Implementing Static and Dynamic Full Adders in Dynamic Body Biasing Technology

Preeti Singh, Shobha Sharma

Abstract: In this paper, we proposed the new technology for good performance and high speed. We used dynamic body biasing implemented static and dynamic full adders. This is very useful for threshold voltage decrease by the dynamic body biasing which has good benefit for decrease delay of the circuits. The proposed method provides less power and delay. In Full Adder implementation CMOS technology at 180 nm is used. Simulation is done by cadence virtuoso tool. New static and dynamic Full Adders have been suggested in this paper. We have implemented 8 bit static and dynamic full adder in 180 nm Dynamic Threshold CMOS technology. The proposed DTMOS circuits are faster than existing Full Adder circuits.

Index Terms: DTMOS, Domino Logic, Full Adder, Delay, Static, Dynamic, Power Delay Product [PDP], and Power

I. INTRODUCTION

Full Adder digital circuits are based on CMOS technology to provide low power consumption. Now a day's main focus in circuit design is on less cost and small area of the circuits. We have used VLSI technology to decrease the power, delay and area. In VLSI design, circuit's works on low power and size is reduced. In this research paper various parameters of the design like power, delay and power delay product are minimized by using dynamic body biasing. This is very effective for the threshold voltage minimization. In this research work, performance of the circuit is improved using dynamic body biasing technique by decreasing the threshold voltage. Dynamic threshold CMOS is very effective technique, which has low delay because threshold voltage is reduced by this technique, in this technique gate and body of MOS is connected and input is given by gate terminal. Full adder using various logic styles in DTMOS are used in arithmetic logic applications. Corresponding

II. VARIOUS LOGIC STYLES USING DTMOS

By logic style using DTMOS is affected various parameters like power dissipation, delay and power delay product of the circuit. Delay of the circuit is based on the no of transistors used and threshold voltage. In Static and dynamic CMOS methods; Static method has 2N no. of transistors and Dynamic method has N+2 no. of transistors. Dynamic method has clock.

A. Static CMOS

In Static CMOS method; there are two pull down and pull up networks. Pull up network connected to VDD and pull down network is connected to GND. In static CMOS method only one network is on other is off. In the output terminal is connected to VDD or GND.

B. Pseudo NMOS method

In Pseudo NMOS method, PMOSs are replaced by one clock which gate is grounded and there is N+1 no. of transistors. Benefits of the pseudo NMOS is less no of transistors are used.

C. Domino logic

In this method we overcome the cascading problem. It is combination of CMOS inverter and dynamic logic. There are two stage of Domino logic: Pre charge stage and Evaluation stage. When clock is zero then this is pre charge stage and output is connected with VDD. So static CMOS inverter has 0 output. When clock is one then this is evaluation stage and output change to zero. So the output of the static CMOS inverter is one.
Implementing Static and Dynamic Full Adders in Dynamic Body Biasing Technology

Fig 3: Domino logic

D. Modified domino logic
This method is very effective for reducing the speed, delay and power consumption are of the Full Adder circuit. When modified domino logic is compared with other method the overall speed and power consumption of the circuit was less.

Fig 4: Modified Domino logic

III. VARIOUS LOGIC STYLES USED IN FULL ADDERS:

Static and Dynamic logics can be used in designing arithmetic circuits. Full adder and comparators are the basic circuits which are used in arithmetic applications. When no of transistors of the circuits are decrease than the power consumption is low and speed is high. Static and dynamic logics such as static, Domino, Pseudo and proposed Domino logics, we have implemented full adders using various logics in dynamic body biasing.

A. Static CMOS full adder in Dynamic body biasing
It is static CMOS Full Adder in Dynamic Body Biasing which is consists 28 no. of transistors.

Fig 5: Static CMOS Full Adder in Dynamic Body Biasing Schematic

B. Pseudo NMOS Full Adder in Dynamic Body Biasing
It has 18 transistors which is implement sum and carry function of full adder and also satisfied the truth table of full adder.

Fig 6: Pseudo NMOS Full Adder in Dynamic Body Biasing Schematic

C. Domino Full Adder in Dynamic Body Biasing:
It has consists 20 transistors which is implemented sum and carry logic of full adder.
Fig 7: Domino Full Adder in Dynamic Body Biasing Schematic

**D. Modified domino full adder in dynamic body biasing (Proposed):**
It consists of 26 transistors and which is satisfied truth table of full adder.

Fig 8: Proposed Domino Full Adder in Dynamic Body Biasing Schematic

**IV. RESULT AND SIMULATION**
In this paper simulated results of existing and proposed Full Adder designs were simulated using 180nm CMOS technology at 1.8 volt using cadence virtuoso tool. The transient responses of the designs are similar as full adder truth table.

A. **Transient Response**

Fig 9: Simulation of static CMOS FA in Dynamic threshold CMOS

Fig 10: Simulated of pseudo NMOS FA in dynamic threshold CMOS

Fig 11: Simulation of domino logic FA in dynamic threshold CMOS

Fig 12: Simulation of proposed domino logic FA in dynamic threshold CMOS
B. Delay calculation by cadence virtuoso

Fig 13: Delay of static CMOS FA in Dynamic threshold CMOS

Fig 14: Delay of pseudo NMOS FA in Dynamic threshold CMOS

Fig 15: Delay of domino logic FA in dynamic threshold CMOS

Fig 16: Delay of proposed domino logic FA in dynamic threshold CMOS

C. Tabulation

D. Table 1: Comparison of delay

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Full Adder</th>
<th>Delay(ns) [Existing]</th>
<th>Delay(ns) [Proposed]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Static CMOS</td>
<td>31.27</td>
<td>20.03</td>
</tr>
<tr>
<td>2</td>
<td>Pseudo NMOS</td>
<td>19.14</td>
<td>16.83</td>
</tr>
<tr>
<td>3</td>
<td>Domino logic</td>
<td>11.278</td>
<td>9.716</td>
</tr>
<tr>
<td>4</td>
<td>Modified Domino logic</td>
<td>7.78</td>
<td>6.93</td>
</tr>
</tbody>
</table>

Table 2: Comparison of power

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Full Adder</th>
<th>Power(µW) [Existing]</th>
<th>Power(µW) [Proposed]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Static CMOS</td>
<td>161.1</td>
<td>234.8</td>
</tr>
<tr>
<td>2</td>
<td>Pseudo NMOS</td>
<td>709.1</td>
<td>700.6</td>
</tr>
<tr>
<td>3</td>
<td>Domino logic</td>
<td>338.8</td>
<td>347.18</td>
</tr>
<tr>
<td>4</td>
<td>Modified Domino logic</td>
<td>213.7</td>
<td>199.2</td>
</tr>
</tbody>
</table>

Table 3: Comparison of PDP

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Full Adder</th>
<th>PDP(E-12) [Existing]</th>
<th>PDP(E-12) [Proposed]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Static CMOS</td>
<td>7.3</td>
<td>4.703</td>
</tr>
<tr>
<td>2</td>
<td>Pseudo NMOS</td>
<td>13.57</td>
<td>11.79</td>
</tr>
<tr>
<td>3</td>
<td>Domino logic</td>
<td>3.81</td>
<td>3.37</td>
</tr>
<tr>
<td>4</td>
<td>Modified Domino logic</td>
<td>1.62</td>
<td>1.33</td>
</tr>
</tbody>
</table>

Fig 17: Comparison of Delay for Gate Driven and DTMOS Adders
This paper dealt with the complete designing of a various logic full adder using dynamic body biasing. It is implemented and characterization is shown in the form of tables and graph for performance parameter like power, delay and power delay product. The design of various logic full adders using dynamic body biasing has been simulated using Cadence virtuoso tool on 180 nm CMOS technology. Figure 17, 18 and 19 shows the proposed design is better than existing design in power consumption, PDP and circuit delay. The delay, power and PDP are decease with the dynamic body biasing technique. All the characteristic plot of the various type full adders is given and calculation of the power, delay and PDP is shown. The results show that various logic full adder using dynamic body biasing has minimized the delay, power and PDP. The graph, table of comparison of various full adders, and transient response show that the proposed design is better than the existing designs.

**FUTURE SCOPE**

The full adder proposed in this paper produced robust result and attained the required design goals. There are always improvements that could be made with any design and so in this. Three areas which need more attention are lower delay, power and PDP. Increasing the speed of the full adder would surely make it a better choice at low power application. The various full adders can be used to design an ALU which could be design several logic functions. The schematic could be design into a layout and further fabricated to real chip for several purposes can be done.

**REFERENCES**


19. Sung no kang, Yusuf labebici,”CMOS Digital interated circuits analysis and design” Third addition.


**AUTHORS PROFILE**

Preeti Singh completed B.Tech in Electronics and communication from UPTU. I have two years industry experience in Central Electronics Limited. Currently pursuing M. Tech in VLSI system from Indira Gandhi Delhi Technical University for women, Delhi, India.