International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-8 Issue-2, July 2019

Deeper Insight of Various Full-Adder Designs with Various Techniques and Technology

Preeti Singh, Shobha Sharma, Ashish Singh

Abstract*: In this paper various type of full adder circuits with high speed operation have been analyzed. Power Consumption, Speed and Area are important factors of the design aspect of full adder circuit. Many researchers have worked on full adder designs using various technologies. Present paper deals with literature analysis based on full adder designs.

Index Term: Power Consumption, Speed, Delay, Full –Adder, Power Delay Products.

I. INTRODUCTION

Full adder is a fundamental unit of any arithmetic operation, can be used in any VLSI system based on the various logic. The Speed, Area, Power Consumption and Power Delay Product (PDP) are the most important design aspects in low power VLSI design. Among these design aspects, power delay product also known as PDP, is used to analyze full adder performance. The overall power consumption of a full adder circuit should be reduced, so that over all consumed power of the chip on board can be reduced. This paper presents a analysis of the work done in different full adder circuits design. Different no of transistors and technology were used by various researchers. Also, we represent the advantages, disadvantages and future scope of the included analysis papers.

II. RELATED WORK

Shahmini Subramanian, Ajay Kumar Singh and Gajula Ramana Murthy, 2018 [1] Proposed a stable 1 Bit Full Adder circuit, which provides better efficiency for power consumption. This paper describes the design of 14 Transistors based full adder stable circuit, which consume less power. Pass transistor logic is used in design. Mentioned Monte Carlo simulation shows that the proposed full adder circuit is more reliable than existing designs. For sum and carry node the proposed circuit was able to attain strong low or high logic. The combinations of 8 logic Output, at SUM and CARRY node is shown in Table1 and Table2.

Table 1: Output Voltage Table at SUM node [1]

Logic Combinations	Output Voltage at Sum node(V)			
	Proposed 14T			
000	0.000	0.000	0.242	0.000
001	0.814	0.681	0.845	0.139
010	0.814	0.716	0.621	0.931
011	0.000	0.000	0.000	0.000
100	0.839	0.716	0.793	0.501
101	0.000	0.000	0.000	0.000
110	0.000	0.000	0.294	0.260
111	0.839	0.690	0.966	0.578

Table 2: Output Voltage at Carry node [1]

Logic Combinations	Output Voltage at Carry node(V)			
	Proposed 14T			
000	0.000	0.000	0.000	0.000
001	0.000	0.000	0.261	0.000
010	0.000	0.000	0.000	0.000
011	0.839	0.750	0.974	0.475
100	0.000	0.000	0.000	0.303
101	0.698	0.725	0.871	0.561
110	0.777	0.518	0.854	0.974
111	0.916	0.535	0.991	0.974

C. M. R. Prabhu, Tan Wee Xin Wilson and Thangavel Bhuvneshvari, 2018 [2] Proposed a novel 11 transistor full adder. In their design 65 NM CMOS Technology were used. They have proposed a power efficient, improved 11 Transistor full adder circuit. In proposed adder circuit, low power consumption is observed. The drawback of the proposed circuit is that it occupies large area on chip since 11 transistors were used. In table 3 shows the comparison of delay and power using different technology.

Table 3: Power and Delay comparison [2]

Technology	65nm	120nm
Power Consumption	0.321 µw	0.731 µw
Size	W:24µm, H:7µm	W:26µm, H:8µm
Delay for Sum	1.30ps	3.00ps
Delay for Cout	1.90ps	3.00ps

Revised Manuscript Received on 30 July 2019.
***** Correspondence Author
Preeti Singh*, Electronics and Communication, Indira Gandhi Delhi Technical University for women, Delhi, India.
Dr Shobha Sharma, (Corresponding Author) Faculty, Electronics and Communication, Indira Gandhi Delhi Technical University for women, Delhi
Ashish Singh Electronics and communication, RJIT, BSF Academy, India.

Harini. V, P. Sasi Seerthi, G. Vishnu Vardhan Rao, 2018 [3] Designed a full adder using domino logic and various other logic styles [like static CMOS, pseudo NMOS etc.]. Proposed circuit consumes low power, high speed and reduces PDP with an alternative logic. All full Adder circuits were designed with CMOS technology of 180 NM. The suggested method provides better power and delay.

Table 4: No of Transistors used and Corresponding Delay [3].

Sr. No.	Full Adder	No of Transistors	Delay
1	Static CMOS	28	31.27 E-9
2	Pseudo NMOS	18	19.14 E-9
3	Domino Logic	20	11.27 8E-9
4	Proposed Domino Logic	26	7.78 E-9

Ramesh Jangir, Ramakant Vyas, 2017 [4] Implemented an area efficient full adder. In it they have used 3 Transistor XNOR using 32 NM CMOS technologies. Also proposed design consumed low power. The proposed design uses 8 CMOS transistors. The reduction in the count of no of CMOS transistor improved area and power performance. In their design Micro wind 3.1 tools at 32 NM technologies has implemented adder cell efficiency for DSP applications. The future work main focus is to minimize the circuit power consumption, area and delay.

Table 5: No of Transistors, power and area comparison [4].

V	power	Area	Transistor count
18TG FA	3.68uw	58.4um2	18
14TG FA	3.68uw	41.2um2	14
10TG XNOR FA	1.534uw	25.5um2	10
10TG XOR FG	0.842uw	25.5um2	10
8T FA (Proposed)	0.813uw	19.4um218	8

Rakesh Chowdary Gutta, UhaNikitha Rachapalli, Piyush Remala, Phaneendra Vale, T V Ramakrishna, (2017) [5] Presented a 1 bit hybrid full adder. Also they have used pass transistor logic in design. The circuit implementation main focus was on performance parameters like delay power and area. In proposed work, they have used 50 NM technologies, which is an improved performance in the context of area, power and delay. Tirumalasetty Venkata Rao, S B Lokesh, K V K V L Pavan Kumar, E Raghu Veera, (2017) [6] Proposed the implementation of 1 bit full adder. They have used voltage bootstrapping in proposed design. Proposed full adder was examined using mentor graphics pyxic schematic composer at a supply voltage of 1.2 volt to 2 volt. In their design, they have used 180 NM technologies. The voltage bootstrapping circuits eliminating the voltage step in the already reported 1 bit full adder design. So the proposed circuit is useful for high performance and complex VLSI design system.

Table 6: No of Transistors, power, delay and PDP comparison [6].

Design	Power (uw)	Delay (ps)	PDP (FJ)	Transistor count
CMOS FA	6.28	304.25	1.9106	28
CPL FA	7.795	194.41	1.5154	32
BBL-PT FA	7.265	290.48	2.1103	23
Current sink FA	7.859	231.56	1.8270	23
Proposed full adder	5.243	213.54	1.1195	25

Pankaj Kumar, Rajender Kumar, (2016) [7] Presented the high performance, low voltage hybrid full adder. In this paper they have reduced the power delay product. Modified NAND and NOR gate were used to represented full adder circuit, which was implemented using cadence virtuoso tool. The design was simulated at UMC 55 NM and 90 NM CMOS technologies. In this paper the full adder implementation was based on power consumption, power delay product and speed, which was compared with conventional CMOS full adder. Table 7 presents the comparison for delay, power delay product and power consumption.

Table 7: Power, Delay, PDP and No of Transistor Comparison

VDD (V)		1	0.4	0.6	0.8
Power (µW)	CMOS	0.574	1.357	2.508	4.152
	HPSC	-	0.65	1.205	1.734
	Hybrid	0.225	0.55	1.036	1.703
	Hybrid CMOS	0.263	0.623	1.154	1.885
	Proposed	0.2713	0.6612	1.274	2.199
Delay(pS)	C-MOS	1071	189.8	85.47	56.41

	HPSC	-	139.4	50.46	45.44
	Hybrid	954.8	179.1	85.07	58.15
	Hybrid CMOS	2718	325.8	120.8	62.28
	Proposed	440.3	79.76	34.63	24.82
Power-Delay Product (aJ)	C-MOS	615.396	257.558	214.358	234.214
	HPSC	-	90.735	60.804	78.792
	Hybrid	215.689	98.522	88.132	99.029
	Hybrid CMOS	716.464	203.103	139.403	117.397
	Proposed	119.453	52.737	44.118	54.579

Raushan Kumar, Sahadev Roy, and C.T. Bhunia, (2016) [8] Implemented the high-speed low power double gate 1-bit full adder. The design was implemented using 16 transistors, which operates at low voltage. In proposed designed, they maintained low output voltage swing, low power consumption and high speed. Circuit was simulated using SPICE simulation tool on 180 NM technologies. In this paper they proposed low voltage swing and low delay because of output voltage degradation. Also they mentioned new MTVL 16Transistor double gate 1bit full adder, leakage current was controlled by proposed designed. Also area and power consumption were reduced by this technique.

Table 8: Power, PDP, Delay, and No of Transistor Comparison in Full Adder [8].

Design	Power (µW)	Delay (ns)	PDP	Transistor Count
CMOS	6.2197	0.2921	1.816	28
CPL	7.7198	0.1839	1.420	32
TFA	8.2491	0.2871	2.368	16
TGA	8.4719	0.2939	2.898	20
14T	12.7217	0.3817	4.855	14
10T	14.3449	0.1325	1.902	10
Majority-based	6.3227	0.1854	1.172	NA
Hybrid	4.1563	0.2240	0.931	16
Proposed FA	4.0513	0.1590	0.644	16

Nishan Singh, MandeepKaur, Amardeep Singh, Punit Jain,(2014) [9]Proposed a Full Adder design, which was implemented using various logic styles like CMOS, Transmission Gate and Pass Transistor logic. Designed full adders were simulated at 180 NM, 90 NM and 45 NM of CMOS technologies. In this paper they have shown the transmission based full adder consumed less power than pass transistor full adder and conventional CMOS based full adder. In this paper they have improved the problem of voltage degradation using transistor sizing. Table 9 presents the comparison of power consumption for different adders.

Table 9: Power Consumption for Various Adders [9].

Sr. No.	Circuit [Full Adder]	Power [on 180nm]	Power[on 90nm]	Power[on 45nm]
1	CMOS FA	3.98 E-6	338.9 E-9	79.1 E-9
2	TG FA	1.52 E-6	181.7 E-9	24.9 E-9
3	Pass Transistor FA	1.82 E-6	252.8 E-9	27.4 E-9

R. Anitha, (2016) [10] Represented a comparative study on transistor based full adder designs. In this paper 1-bit full adder was implemented using Arithmetic logic, which is very useful for achieving fast results. In it they have minimize the area on chip and power consumption, which is very useful for portable applications. Also they have reduced the circuit delay, which leads to fast processing.

Table10: Delay, Power and Power Delay Product Comparison for Various Adders [10].

Adder	No. of Transistors	Power (nW)	Delay (ps)	PDP(E-20)
CMOS	28	54.7	375.3	2054
CPL	32	76.8	462.7	3554
TGA	20	43.0	282.4	1215
TFA	16	41.0	297.3	1219
HPSC	22	38.8	539.6	2096
Hybrid CMOS	24	34.7	372.8	1293
14T	14	45.3	427.5	1937
Proposed 8T	8	5.9	288.3	1691

Zahra Zareei, Keivan Navi&PeimanKeshavarziyan, (2017) [11] Proposed a low power, high-speed 1-bit inexact full adder cell designs. It is very suitable for low-energy image. In this paper they have used the MATLAB tool and HSPICE tool on 32 NM technologies. With the help of HSPICE tool, they studied effect of temperature variation and voltage scaling on the proposed full adder design. Also using MATLAB tool they have performed image processing

Table 11: Characteristics of inexact Full Adder cells [11].

Design	Transistor	Critical path	Full swing	Error distance
AXA1	8	3	YES	4
AXA2	6	3	NO	4
AXA3	8	3	NO	2
InXA1	8	3	NO	2
InXA2	10	4	NO	2
InXA3	8	4	NO	2

simulation, which evaluate the peak SNR of proposed full adder design. Current mode scheme at 32nm carbon nano tube field effect transistor has been used in proposed design.

Table 12: Analysis of different type of Full Adder Design

Sr. No	Title of the Paper	Publisher, Year & Vol.	Indexing	Technology or Tool Used	Conclusion	Advantages	Disadvantages	Future Scope
1	Design of power efficient stable 1-bit full adder circuit	IEICE Electronics Express, 2018, Vol. 15	SCI and Scopus	Monte Carlo Simulation	Proposed 1-bit full adder design control leakage current effectively.	More reliable than existing circuits.	Proposed circuit has design complexity.	Proposed layout can be fabricated to chip for several purposes.
2	Novel 11 T Full Adder in 65 NM CMOS Technology	ARPN Journal of Engineering and Applied Sciences, July 2018, Vol. 13	Scopus	65 nm technology	Proposed 11 T adder design reduced leakage current.	Proposed circuit has the less delay.	Proposed circuit has large chip size.	Proposed layout can be fabricated to chip for several purposes.
3	Comparative Analysis and Design of Full Adder using Domino Logic and Various Logic Styles	International Journal of Pure and Applied Mathematics, 2018, Vol. 119	Scopus	Cadence Virtuoso 180 nm	Proposed full adder has less delay and power delay product.	Proposed circuit has Less PDP and higher speed.	Proposed circuit has more no of transistors.	The proposed schematics further could be converted into layout.
4	An area Efficient 3T XNOR cell based Low Power Full adder using 32nm Technology	International Journal of Engineering Trends and Technology (IJETT), July 2017, Vol. 49	NASA ads	Microwind 3.1 tool 32 nm	Proposed full adder exhibits less area on chip and power consumption .	Proposed circuit has reduced area cell.	Proposed circuit has increased delay.	Further overall circuit delay could be reduced.
5	Design and Analysis of one Bit Hybrid Full Adder Using Pass Transistor	International Journal of Pure and Applied Mathematics , 2017, Vol. 116	Scopus	50 nm technology	Proposed design occupies less area on chip. Also power consumption is less	Proposed full adder uses less no of transistors and minimizes power consumption .	--	Proposed layout can be fabricated to chip for several purposes.
6	Design and Implementation of 1 Bit Full Adder Using Voltage Bootstrapping Circuit	International Journal of Pure and Applied Mathematics , 2017, Vol. 117	Scopus	Mentor graphics 180 nm	In proposed full adder design, used voltage bootstrapping circuits eliminated the voltage step.	Proposed full adder is suitable for high performance and complex VLSI system.	--	Further area on chip can be reduced.

7	Low Voltage High Performance Hybrid Full Adder	Engineering Science and Technology, an International Journal 19, 2016,	ESCI, Scopus (Elsevier)	Tool: Cadence Virtuoso UMC 55 nm and 90 nm	Design has high performance and good power delay product.	Proposed circuit has best PDP.	--	Proposed full adder design could be a good choice at Nano scaling in VLSI system.
8	Low-Power High-Speed Double Gate 1-bit Full Adder Cell	International Journal of Electronics and Telecommunications, Nov 2016, Vol. 62	Scopus (Elsevier)	SPICE simulation tool, 180nm CMOS technology	Proposed full adder design reduced the leakage current and improved the performance.	Proposed circuit controlled leakage current, reduced power consumption, area and PDP.	Complexity of the circuit increases due to many transistors was used to represent the full adder circuit.	Later more leakage current could be controlled.
9	An Efficient Full Adder Design Using Different Logic Styles.	International Journal of Computer Applications , July 2014, Vol. 98	EBSCO, NASA ADS	180 nm, 90nm, 45nm, technologies Cadence virtuoso tool	Proposed full adder provides minimum transistor count as well as load capacitance.	Proposed circuit consumed less power.	Proposed circuit suffers from voltage degradation.	The presented work can be extended to make complete Arithmetic unit, which can be used in many VLSI system.
10	Comparative study on transistor based full adder designs	World scientific news, 2016, Vol-47	EBSCO	HSPICE tool 90 nm CMOS technology	Proposed full adder design improved the power consumption.	Due to less power consumption, proposed full adder circuit is very useful in portable application.	--	--
11	Low-Power , High-Speed 1-Bit Inexact Full Adder Cell Designs Applicable to Low-Energy Image Processing	International Journal of Electronics, July 2017, Vol. 47	SCI, Scopus (Elsevier)	Tool: HSPICE and MATLAB 32 nm CNFET Technology	By proposed full adder design, error distance was minimized as possible.	Proposed circuit has reduced the delay and circuit complexity.	--	--

III. CONCLUSIONS

The Full Adder is an important part in the VLSI designs because full adder performance decides the performance of VLSI designs. Here in this analysis paper, we compare design of full adder based on performance parameters like: delay, area on chip, power consumption, and power delay product.

To achieve the comparison among mentioned performance parameters various technology and tools were used by different researchers. In this paper we have also compare the advantages, disadvantages and future scope of different full adder circuit, which will be very useful for VLSI system design.

REFERENCES

1. ShahminiSubramaniam, Ajay Kumar Singh and GajulaRamana Murthy, 2018: Design of power efficient stable 1-bit full adder circuit, IEICE Electronics Express, Vol. 15.
2. C. M. R. Prabhu, Tan Wee Xin Wilson and ThangavelBhuvneshvari, "Novel 11 T Full Adder in 65 NM CMOS Technology", ARPN Journal of Engineering and Applied Sciences, Vol. 13, No, July 2018.
3. Harini. V, P. SasiSeerthi and G. Vishnu VardhanRao, "Comparative Analysis and Design of Full Adder using Domino Logic and Various Logic Styles", International Journal of Pure and Applied Mathematics, Vol. 119, No, 2018.
4. Ramesh Jangir and RamakantVyas, "An area Efficient 3T XNOR cell based Low Power Full adder using 32nm Technology", International Journal of Engineering Trends and Technology (IJETT), Vol. 49, No, July 2017.
5. RakeshChowdaryGutta, UhaNikithaRachapalli,PiyushRemala, Phaneendra Vale and T V Ramakrishna, "Design and Analysis of one Bit Hybrid Full Adder Using Pass Transistor ", International Journal of Pure and Applied Mathematics, Vol. 116, No, 2017.
6. TirumalasettyVenkataRao, S B Lokesh, K V K V L Pavan Kumar and E Raghu Veera, "Design and Implementation of 1 Bit Full Adder Using Voltage Bootstrapping Circuit", International Journal of Pure and Applied Mathematics, Vol. 117, No, 2017.
7. Pankaj Kumar and Rajender Kumar, "Low Voltage High Performance Hybrid Full Adder", Engineering Science and Technology, an International Journal, Vol. 19, No, 2016.
8. Raushan Kumar, Sahadev Roy, and C.T. Bhunia, "Low-Power High-Speed Double Gate 1-bit Full Adder Cell", International Journal of Electronics and Telecommunications, Vol. 62, No, Nov 2016.
9. Nishan Singh, MandeepKaur, Amardeep Singh and Punit Jain, "An Efficient Full Adder Design Using Different Logic Styles", International Journal of Computer Applications, Vol. 98, No, July 2014.
10. R. Anitha, "Comparative study on transistor based full adder designs", World scientific news,Vol. 47, No. 2016.
11. Zahra Zareei, KeivanNavi&PeimanKeshavarziyan, "Low-Power, High-Speed 1-Bit Inexact Full Adder Cell Designs Applicable to Low-Energy Image Processing", International Journal of Electronics, Vol. 47, No, July 2017.

AUTHORS PROFILE

Preeti Singh, completed B.Tech in Electronics and communication from UPTU. I have two years industry experience in Central Electronics Limited. Currently pursuing M. Tech in VLSI system from Indira Gandhi Delhi Technical University for women, Delhi, India

Ashiah Singh, , completed B.Tech in Electronics and communication from AKTU. M. Tech in Digital communication from RJIT, BSF Academy, India.