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Design and FPGA Implementation of LDPC Decoder Chip for Communication System using VHDL

Aakanksha Devrari, Adesh Kumar, Himanshu Chauhan, Amit Kumar

Abstract*: The paper emphasized on the design and application of LDPC coding system using FPGA. The LDPC decoder is used to decode the information/data received from the channel after correcting channel errors based on parity bits selection of the data bits. In the communication system, when a parity check failure is noticed, the information from the multiple parity bits can be used to recover the original data bit. The LDPC decoder implementation is done using Shift-Register based design to reduce the complexity. The Modified Sum Product (MSP) method is used to decode, the signal. The system performance is also analyzed with hardware chip and timing parameters with FPGA implementation of the same system. The chip design of the LDPC chip is done usingVivado 17.4, programmed with the use of VHDL and hardware performance is estimated on Virtex-5 FPGA.

***Index Terms*: AWGN, BPSK, LDPC codes, VHDL language, MSP, FPGA**

I. INTRODUCTION

The communication system transmits the data form transmitter to receiver through channel using landline or wireless medium. The consistency of the communication system is subjected to the external noise minimization in environment. The noise produces intrusion to the system which introduces the faults in communicated data. The Fig. 1presents a Forward error correction (FEC) communication system diagram which shows transmission of information/data from source to destination. The data from source is provided to the encoder and further processing for modulation using some modulation technique and then transmitted over AWGN channel. The noise is added in the transmission through channel. The output of the channel is given to the demodulator and the data is decoded using error correcting decoder at receiver end. The LDPC coding was first introduced by Gallager [1, 2] in the initial of 1960. The outstanding discovery was overlooked by investigators for almost 20 years, till a scholar named Tanner suggested a new understanding to the LDPC coding in 1981, from graphical viewpoint. The research was directed to find again of Gallager's codes. It was understood that an extensive LDPC codes with iterative translating which was grounded proceeding for thetrust propagation that permits a routine faults improvement with only a segment away of a decibel under the acceptance of Shannon'stheorem [3, 6, 7, 8]. Consequently, this finding completed the LDPC coding is one of the controlling method comparatives to turbo coding, widely used for channel coding [4, 5] and error corrections where high reliability is primary concern.

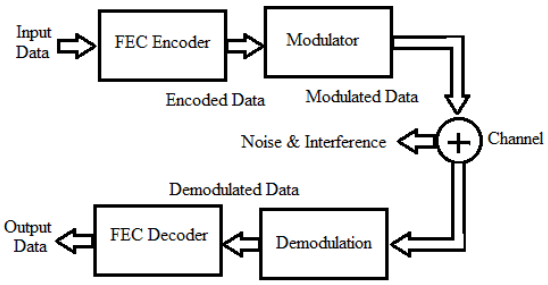

Fig 1 FEC Encoded Communication System

II. LDPC CODING

The LDPC codes are directly referred as linear block codes, designated by (n, k) or (n, w_c, w_r).
Where, n = the length of code word,
k = length of the message bits,
W_c = column coefficients/weight means the count of nonzero essentials present in a column of a parity checker matrix and W_r = row weight means the count of non-zero essentials present in a row of a parity checker matrix.
The LDPC codes are following two main characteristics.
Parity Check: These codes are characterized by a parity checker matrix H, which is formed as a binary matrix and satisfies the condition

$$cH^T = 0 \qquad (1)$$

Where, c is a codeword.
Low Density: H denotes the sparse matrix which means the presence of number of '1' is much less than the presence of '0's. The behavior is referred sparseness of H which assurances the low computing complexity.

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***** Correspondence Author
Aakanksha Devrari*, Research Scholar, Department of Electronics & Communication Engineering, Uttarakhand Technical University, Dehradun, India
Adesh Kumar Department of Electrical & Electronics Engineering, University of Petroleum and Energy Studies, Dehradun, India
Himanshu Chauhan, Department of Electronics & Communication Engineering, College of Engineering (COER), Roorkee India
Amit Kumar Faculty of Technology, Uttarakhand Technical University, Dehradun, India

Tanner Graphs: The Tanner graph [9, 10] is formed by two sets of vertices: variable/inconstant nodes and check nodes. The codeword is denoted by the 'n' vertices, referred as variable nodes, and 'k'vertices grants the parity checking equations denoted by check nodes [11, 12].

The edge associates a variable node with the checker node if that specific bit is comprised in the consistent parity check [1, 13] equivalence. Therefore, the number of count ends in the tanner diagram represents the available number of logic'1's in the parity checker matrix.

Cycle: A cycle or a circle in a Tanner diagram is an order of associated vertices which are starting and ending at the same vertex in the diagram and covers another vertices also, but not more than once. The extent of a cycle is the sum of edges, that it permits. Since the Tanner graphs are bipartite, each cycle is associated with even length.

Girth: The girth presents the minimum extent of the rounds or cycles for the Tanner graph. For an example, let us consider that H denotes the parity checker matrix of an asymmetrical (10, 5) LDPC coding.

$$H = \begin{bmatrix} C_1 \\ C_2 \\ C_3 \\ C_4 \\ C_5 \end{bmatrix} [X_1 \quad X_2 \quad X_3 \quad X_4 \quad X_5 \quad X_6 \quad X_7 \quad X_8 \quad X_9 \quad X_{10}] \quad (2)$$

$$H = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \end{bmatrix}$$

The Fig. 2 presents the Tanner graph corresponding to H matrix . The LDPC codes are based on iterative decoding procedure in which statistical independence is considered for the message conversions between changed nodes. In each cycle, the generated message of each node will be transferred back to the node itself. The assumption is not self-deterministic due to which the decoding accuracy is wedged. Thus, it is required to get the matrices with high girth values.

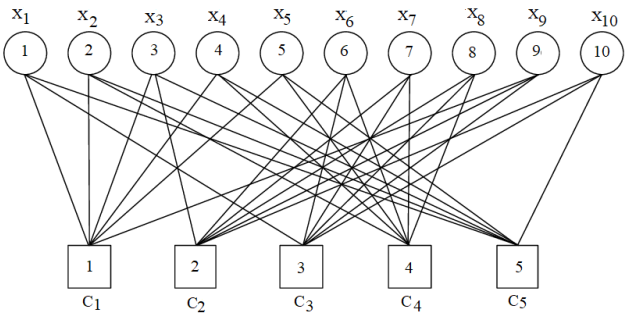

Fig. 2. Tanner graph for the parity check matrix H

LDPC Encoding: The encoding [2, 14] of the LDPC coding process is depending of the length of code word. Irrespective of it, the codes are providing many advantages. The encoding of LDPC codes can provide difficulty for some commercial applications. The codes are having large encoding delay and complexity. The encoding of LDPC codes [15] contains of two tasks

- Formation of a sparse parity checkermatrix.
- Create the code words using thismatrix.

Decoding of LDPC Codes: The iterative algorithms [5, 16] are used for decoding the LDPC codes. Belief Propagation(BP) is widely adopted algorithm used for the decoding of LDPC codes.

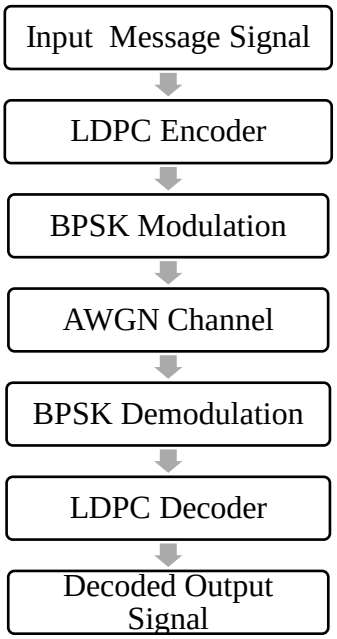

Fig.3. BPSK Modulation and AWGN Channel for LDPC

The hardware implementation for the BP algorithm is adapted using "Min-Sum" approach in which the information of data node is updated first after the checking of the node in each iteration. In the close of the decoding technique a tough decision is taken based on the most probable codeword [10]. The block levelpresentation of the LDPC based communication system is depicted in fig. 3 which is based on BPSK modulation [4, 17] and demodulation at transmitting and receiving end respectively. The block parts ofLDPC based communication system are processed through AWGN channel.The random data is transmitted and modulated with the help of BPSK modulator. LDPC encoder is encoding the transmitted data through the AWGN channel, [8, 18, 19] demodulation is done by BPSK demodulator and LDPC decoder to decode the instantaneously data at the receiving end.

III. LDPC ENCODER AND DECODER

The LDPC codes as cyclic codes are considered as special case used to conceptualize the parity check code.

Matrix for Parity Check: The formation of parity checker matrix is based on block-circulant LDPC code creation for the generation of a parity checker matrix. The main benefit of circulant code is that it provides more accurate error correction performance as well as the structured decoder architecture. The binary matrix is used to present the parity check matrix in which single row is created with the help of the preceding row by a single right cyclic shift. The parity check matrix H with size (rT×nT) is constructed using concatenation of (r×n) light circular of size T×T. The Tanner diagram matching to the matrix is namedas a protograph [7].

The photographs considered in the design are AR3A is shown in in fig. 4 and AR4A codes with a rate of ½ depicted in fig. 5.The squares present the parity checker nodes and circles are denoting the variable nodes. The hard circles are representing the communicated symbolic codes and the open ones are penetrated. The design is based on 3 level decoding: accumulate to decode, repeat-by-3 (or 4), and accumulate further to decode [8]. The photographs presented a block circular parity checker matrix (3 × 5) in which the number of parallel ends denotes the grade of the consistent circulant. The protograp [20] would not be straight extended without familiarizing less weight codewords, irrespective of the selection of circulars. That's what protograph can be extended twice with small variation matrices, with size 8 × 8 and 4 × 4.

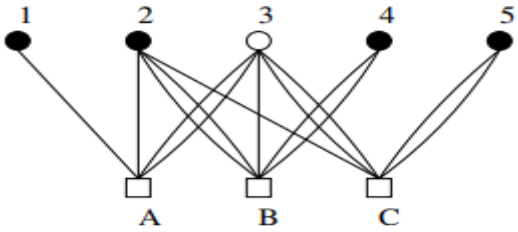

Fig.4 AR3A Protograph

These circulants are used to form the complete code. The obtained matrix is a resultant of parity checker matrix such as depicted in fig. 5 for a minor AR4A code. The nonzero entries of a matrix are presented by a dot. The protograph is created by putting checker nodes in the sequence of (A, B, C) and variable nodes in the order of (4, 2, 1, 5, 3) for AR4A and drawn with the help of solid lines, first growing with 4 × 4 variations, and then increasing with 16×16 circulars. The resultant 12 × 20 group-circular formation is highlighted by dottedlines.

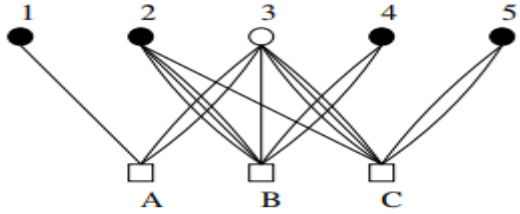

Fig. 5 AR4A protograph.

The idea is illuistrated with the help of AR3A diagram and AR4A diagram and codingsamples. In case of reordering the rows selection and columns selections of AR4A, the base matrix is presented as (B, A, C) and sequence will be (4, 2, 3, 1, 5). The base matrix is given as

$$H = \begin{bmatrix} 2 & 3 & 1 & 0 & 0 \\ 0 & 0 & 2 & 1 & 0 \\ 0 & 1 & 3 & 0 & 2 \end{bmatrix}$$

Encoder Hardware

The hardware implementation of the encoder depends on the block-circulant matrix generated by the contents of the shift registers and cyclic shift taken row wise after row wise sequentially. It is a group of (n-k) encoders bits working with the concept of recursive convolutional codes. Each encoder is having limited length 'T'. The fig. 6 presents the feeding method with 'k' message bits given to encoder sequentially, and then registers are updating their values with shift operation taken once per bit. The contents are stored in the register. The switches are then altered, and contents of these registers are readout in sequential wayalong with the parity bits of each codeword.

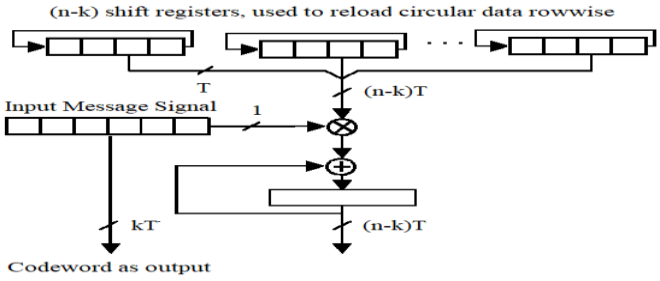

Fig. 6 The (n-k) soft operations with circular data processing row wis

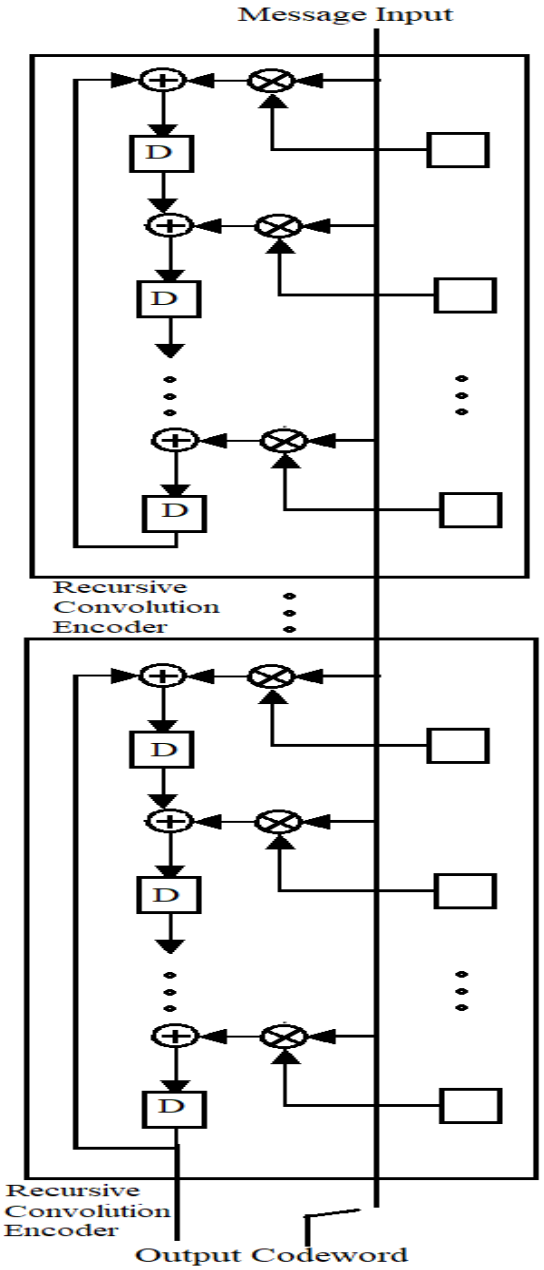

Fig. 7 Encoder structure with circular operation

IV. IMPLEMENTATION OF LDPC

The LDPC encode output is taken based on the multiplication operation of input message matrix with the generator matrix. For the large message, it becomes very difficult to implement a LDPC encoder with a complex matrix. The following steps are involved in encoding process

Step-1: Calculate parity check matrix H

$$H = [-P^T : I_{n-k}] \quad (3)$$

Step-2:Calculate Generator matrix (G)

$$G = [\mathrm{I_k} : \mathrm{P}] \quad (4)$$

Step-3: Calculate the transmitted code word(c) will be

$$c = m.G \quad (5)$$

The parity matrix (H) is designated from the circulant data encoding. H denotes the sparse matrix with rate (1/2). In the general way, the H matrix is of the form 2048 x 4096. The generator matrix G is also in the form 2048 x 4096, but real time design and implementation of such a big data is a challenging task since as the contents are written for each link i.eamong checker nodes and variable nodes. For the implementation point of view, the matrix (32 x 64) can be repeated to implement a big matrix of larger size. The H matrix and G matrix for the VHDL design implementation used is given in fig.8 and fig.9 respectively.

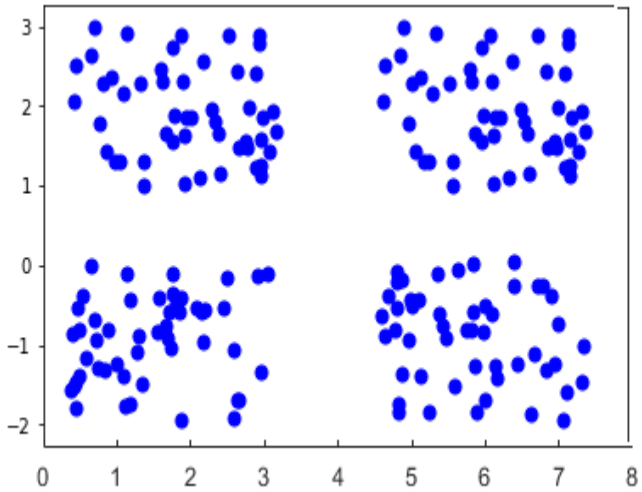

Fig. 8 H Matrix for VHDL implementation

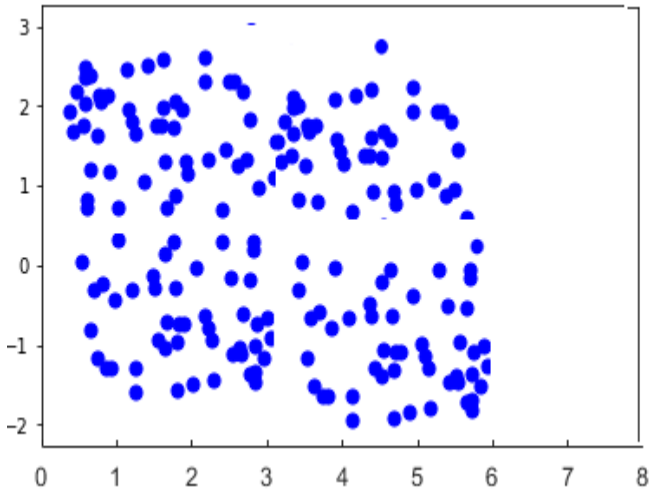

Fig. 9 G Matrix for VHDLimplementation

V. RESULTS & DISCUSSIONS

The VHDL design and implementation of the system includes the multiplication function of the input message matrix along with generator matrix (G).The size of generator matrix is of order 16 x 32, means that the input message size is 16-bit and output is of 32-bit. The matrix multiplication concept is used in between message stream and generator matrix. The VHDL programming is used for the chip synthesis on virtex-5 FPGA for target device xc5vlx20t-2-ff32.

Step 1: The contents of the generator matrix is stored in registers. The encoder will require 16 no. of 32-bit registers to store the contents of 16 x 32matrix.

Step 2: Matrix multiplication between message matrix (1 x 16) and generator matrix is written with a combination of AND logic & OR logic.

Step 3: The VHDL test bench is used to check the functionality of the design.

Step 4: The output of the encoder is tested through the AWGN channel.

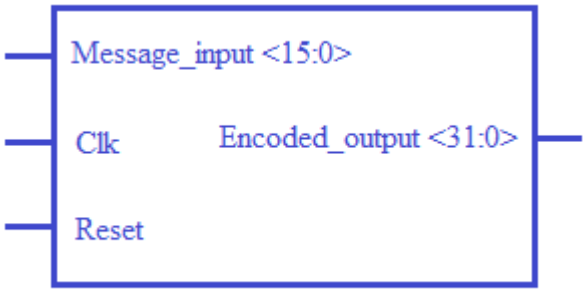

Fig. 10 RTL View of Encoder

The fig. 10 presents the RTL view of encoder chip. The detail of the pins is given in table 1.

Table 1 RTL Pin detail of encoder chip

Pins	Description
Clk	Clk is the input clock signal used to run the clock with 50 % duty cycle on rising edge.
Reset	Input signal to reset the register contents. When reset = '1' then the contents of encoderis zero, When, reset = '0', the contents of encoder is processed
Message_input<15:0>	It is the 16-bit input message given at the input of the transmitter

Encoded_output<31:0 >	**It is the 32-bit output of the AWGN channel considered as the output of the encoder**

LDPC decoder is implemented using a Modified Sum Product Algorithm (MPSA) [20], which is an approximation algorithm in perspective with normal SPA algorithm. A modified SPA is used for implementation ease of thisdecoder. The fig. 11 presents the RTL view of decoder chip. The detail of the pins for decoder chip is given in table 2.

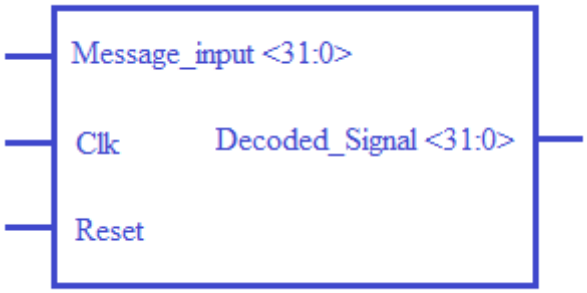

Fig. 11 Decoder RTL view

Table 2 RTL pin detail of decoder chip

Pins	Description
Clk	Clk is the input clock signal used to run the clock with 50 % duty cycle on rising edge.
Reset	Input signal to reset the register contents. When reset = '1' then the contents of decoderis zero, When, reset = '0', the contents of decoder is processed
Message_input<31:0>	It is the 32-bit input message given at the input of the receiver end
Decoded_signal<31:0>	It is the 32 -bit output of the receiver as the decoded signal

The detail of the hardware resources utilization is shown in table 3. It delivers the information of no. of slices, flipflops, LUTs and IoBs. The table 4 gives the information of chip timingrealted parameters such as minimum **p**eriod (ns), maximum timeline after clk (ns), minimum timeline before clk (ns), and combinational path delay.

Table 3 Hardware resources utilization

Hardware	Encoder	Decoder
Slices	32/12480	100/12480
Slice Flip-Flops	41/12480	48/12480
LUTs	55/330	68/330
IOBs Bounded	49/172	65/172
GCLKs	1/32	1/32

Table 4 Timing parameters summary

Timing Parameter	Encoder	Decoder
Max Frequency (MHz)	355.0	355.0
Minimum period (ns)	1.056	1.275
Timeline before clk (minimum) (ns)	1.820	2.019
Timeline after clock (maximum) (ns)	2.420	2.154
Combinational path delay (ns)	6.152	7.504
Speed Grade	-5	-5

The fig 12 presents the simulation results of the LDPC encoder and decoder.

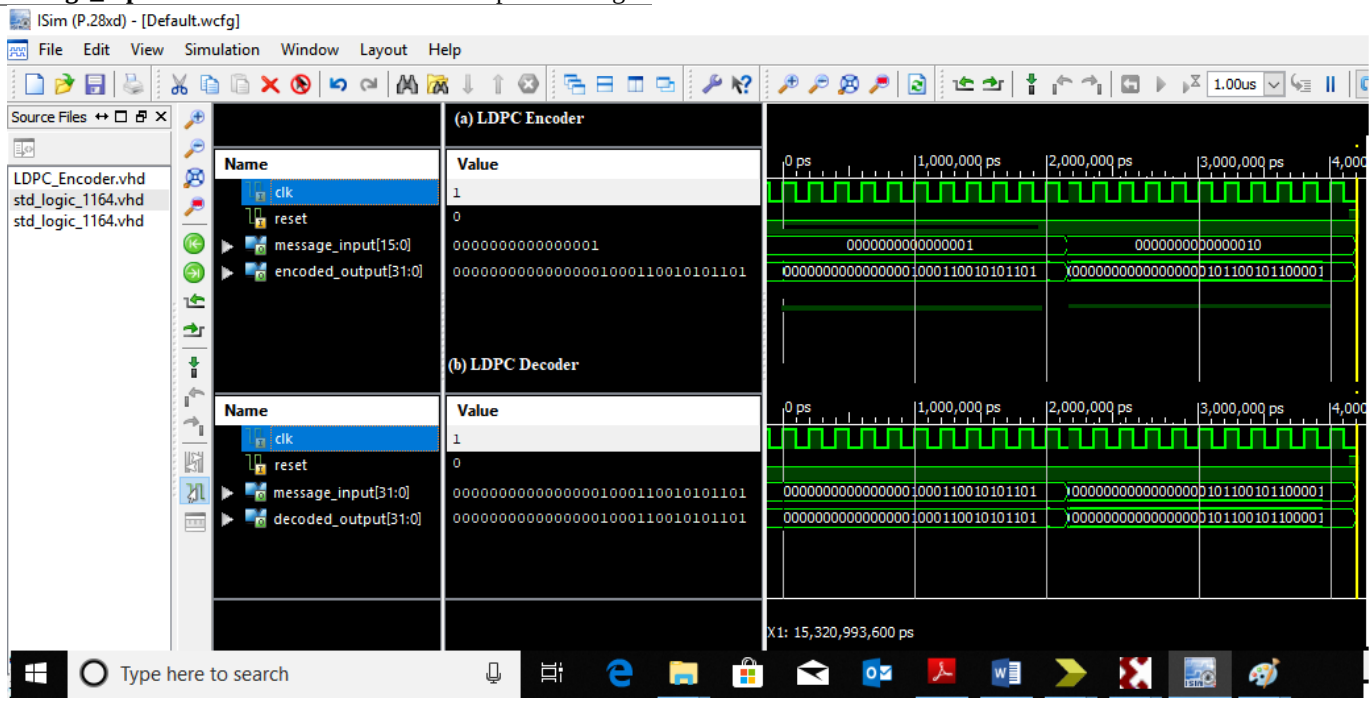

Fig. 12 Simulation of LDPC decoder and encoder

The following test cases are used to check the functionality of the design.

Test-1: Clk = Clock signal, Reset = 0, message_input [15:0] = "0000000000000001" then the encoded_output = "00000000000000001011001011000001".

Test-2: Clk = Clock signal, Reset = 0, message_input [15:0] = "0000000000000010" then the encoded_output = "00000000000000001001110010101101".

Test-3: Clk = Clock signal, Reset = 0, message_input [31:0] ="00000000000000001011001011000001".thenthe decoded_output ="00000000000000001011001011000001".

Test-4: Clk = Clock signal, Reset = 0, message_input [31:0] ="00000000000000001001110010101101".then thedecoded_output="00000000000000001001110010101101".

VI. CONCLUSIONS

LDPC Codes are the linear error improvement codes for the error correctness, a technique of transmitting the messages over the noisy channel. With lieu - Shannon's controlled implementation & typically parallel execution of plan, low-density parity check codes are mainly executed at enquire & well-designed area of applications. The FPGA Implementation of LDPC codes using matrix method and Modified Sum Product (MSP) Algorithm have been achieved. The complexity [21] of the LDPC decoder implementation is reduced using Shift-Register method. The chip design of LDPC decoder is done in Vivado 17.4 using VHDL and Virtex-5 FPGA is used for synthesis for target device xc5vlx20t-2-ff32. The hardware parameters such as slices, flipflops, IoBs, LUTs, GClk and timing results for the same are extracted successfully from Xilinx VivadoSoftware. The LDPC codes will be possible to decode by the low power microprocessor with the help of FPGA look up tables. The designed encoder chip is advantageous for error correction in scalable communication system

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AUTHORS PROFILE

Ms. AakankshaDevrariis Research Scholar in Electronics & Communication Engg. Department at Uttarakhand Technical University, Dehradun India. She is B.Tech in Electronics & Communication Engineering from Uttaranchal Institute of Technology, Dehradun, affiliated to Uttarakhand Technical University Dehradun in 2011. M.Tech(Hons.) in VLSI Design, from Faculty of Technology, VLSI Department, Uttarakhand Technical University (UKTU) in 2013.. Her areas of interest are Digital Communication, Digital Signal Processing, Antenna Wave Propagation & Mobile Computing. She has published more than 20 research papers in international journals and conferences.

Dr. Adesh Kumar is currently working as Assistant Professor (Selection Grade) with the department of Electrical &Electronics Engineering, University of Petroleum and Energy Studies (UPES), Dehradun India. He is B.Tech in Electronics & Communication Engineering from Uttar Pradesh Technical University (UPTU), Lucknow India in 2006. M.Tech (Hons) in Embedded Systems Technology, from SRM University, Chennai in 2008. Ph.D (Electronics Engineering) form University of Petroleum and Energy Studies (UPES), Dehradun India in 2014. He has employed in TATA ELXSI LIMITED Bangalore as Senior Engineer and faculty member in ICFAI University, Dehradun. His areas of interest are VLSI Design, Embedded Systems Design, Network on Chip, Digital Image Analysis.

He has published more than 50 research papers in international peer reviewed journals and conferences. He has contributed as Conference secretary in ICICCD-2016, ICICCD-2107 and editor in ICICCD 2018. He is the reviewer of many SCI and SCIE journals such as Wireless Personal Communications, Microsystem, Technologies, 3D research, Springer, Journal of Visual Languages and Computing, Elsevier, etc are few of them.

Dr. Himanshu Chauhan is currently working as Head of Department, Associate Professor in Computer Science Department, College of Engineering Roorkee(COER) Roorkee, Affiliated to Uttarakhand Technical University, Dehradun India. He is B.Tech in Electronics & Communication Engineering from MPJ Rohailkhand University, Bareilly, India in 2001. M.Tech in Computer Science Engg. from JRM Vidyapeeth University, Udaipur, Rajasthan in 2007. Ph.D (Computer Science Engineering) from ChandraMohan Jha University, Meghalya,India in 2012. His areas of interest are Cloud Computing, Image Processing, Cyber Security, Embedded Systems. He has published more than 45 research papers in international peer reviewed journals and conferences.

Mr. Amit Kumar is currently working as an Assistant Professor, in Faculty of Technology VLSI Department, Uttarakhand Technical University, Dehradun India. He is B.Tech in Electronics & Communication Engineering from Gurukul Kangri University, Haridwar, Uttarakhand in 2009. M.Tech in VLSI Design, from Faculty of Technology, VLSI Department, Uttarakhand Technical University in 2013. Pursuing Ph.D (Electronics & Communication Engineering) from Uttarakhand Technical University, Uttarakhand, India. His areas of interest are VLSI Technology, Digital Image Processing, Control Systems. He has published more than 20 research papers in international journals and conferences.