International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-8 Issue-2, July 2019

Design and Analysis of Power Efficient 64-Bit ALCCU

Dharmavaram Asha Devi, Muchukota Suresh Babu

Abstract*: Speed of any system depends on mainly two factors known as frequency and parllel processing. Such high speed processing systems are required in real time embedded systems. The existed systems are operated with maximum of 2 to 3 GHz. The proposed 64-bit ALCCU is a high-speed processing system that will perform arithmetic, logical and code conversion operations. It is implemented in structural style with Verilog Hardware Description Language. This design is a high speed, low powered and will perform 32 operations. Its data size is 64_bit, implemented on xc7a100tcsg324-1 which is an Artix 7, 100K gate technology FPGA with a CSG 324 package. Satisfactory low power (less than 1W) has been observed with varying clock rates of ranging from 10 MHz to 20 GHz. The analysis is done with Low Voltage CMOS I/O standards from 1.2 to 3.3V range. The application of the proposed design can be used as an IP in high speed processors and controllers.

***Index Terms*: Arithmetical, Logical and Code-Conversion Unit (ALCCU), Field Programmable Gate Array, Hardware Description Language, Low Voltage CMOS.**

I. INTRODUCTION

For the past five decades, various processors and controllers were developed and are used in multiple applications. The aim of VLSI Design Engineer is to reduce power consumption, improving the performance and reducing the area. In the present scenario, there is a requirement of power efficient 64-bit processors in which 64-bit ALUs plays a vital role. With this motivation, high speed, power efficient ALCCU with 64-bit design is implemented. The operating frequency of the proposed design is up to 20 GHz and power consumption is less than 0.5W.

A. *Literature survey*

ALUs are designed with 8-bit to 64-bit with an operating frequency of up to 5GHz. The proposed design is power efficient than existed and can operate up to 20GHZ operating clock speed.

B. *Problem Statement*

When Design of power efficient, high speed, multi-functional 64_bit processing unit known as ALCCU. This can be verified, synthesized and implemented using CAD tool and FPGA.

II. DESIGN ANALYSIS

The design of 64-bit ALCCU is divided into 5 modules named as AU1, AU2, LU1, LU2, and 4-input signal selector to select one out of four functional module outputs. This design is able to implement 32 operations and hence total five select signals are used that are S0-S4. Each functional module will perform eight different operations. Therefore, three select signals S0_S2 are used to select one among them with S2 as MSB and S0 as LSB. These three select signals are connected concurrently to all four functional modules. The outputs of four individual functional units hold the results of four different operations according to their select signals combination. Now, the selection signals S3 to S4 are used for the selection of one output among four functional unit's outputs. It is a sequential design. In order to synchronise the design, global clock is given to all four functional units. Bottom up approach is used in this design.

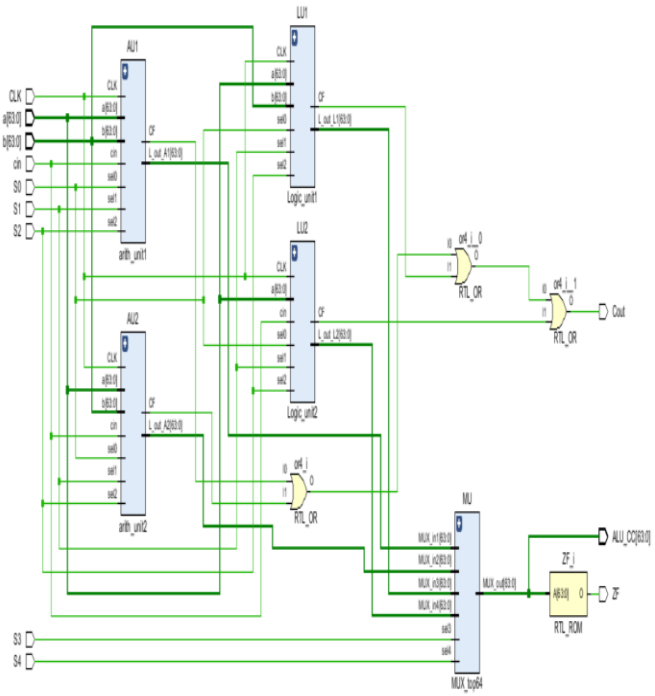

Fig. 1. RTL Design of 64_bit ALCCU

Table. I illustrates the functions implemented in the proposed system. Hierarchical model of ALCCU consists of five sub modules, four functional modules and one multiplexer module as shown in Fig.1.

Revised Manuscript Received on 30 July 2019.
***** Correspondence Author
Dharmavaram Asha Devi*, Department of Electronics & Communication Engineering, Sreenidhi Institute of Science and Technology, Hyderabad, India.
Dr. M. Suresh Babu, Department Computer Science Engineering, Sri Krishnadevaraya University, Anantapur (A.P), India.

The first arithmetic unit performs eight operations with 64-bit data size that are: i) addition of two numbers without carry, ii) addition with carry, iii) subtraction, iv) subtraction with borrow, v) multiplication of two numbers (16_bit numbers with 32-bit product), vi) division operation, vii) increment operation, and viii) decrement operations respectively. The corresponding select signals S0 to S4 values are 0 to 7, with S4 as most significant bit and S0 as least significant bit. The logic of the design is implemented in behavioural model using switch type logic to select one among eight operations.The second functional unit performs another set of eight operations: i) negation operation (1's complement), ii) 2's complement, iii) modulus, iv) percentile, v) even parity generation, vi) odd parity generation, vii) binary to gray conversion and viii) gray to binary conversion operations. The select signal values are 01000 to 01111 as shown in Table I. The second functional unit is further sub divided in to three sub modules: i) parity generation, ii) gray code conversion from binary and iii) binary conversion from gray code. This arithmetic unit2 is more complicated than arithmetic uint1 as it consists of parity generation and two code conversions, binary to gray and gray to binary. These three sub modules are implemented in gate level model and instantiated in arithmetic unit2. The eight functions come under this will be selected using case statement.The third functional module is LU1 which performs: i) Transfer Operation, ii) Inversion Operation, iii) AND, iv) OR, v) NAND, vi) NOR, vii) XOR and viii) XNOR operations. All these operations are bit wise logic operations. The corresponding select-signal values are from 16 to 23 as illustrated in Table 1. The logic of the logic unit1(LU1) is implemented with non-blocking assignments, to provide concurrent execution of all the logical operations specified under this module.The fourth functional unit, LU2 performs other eight logical operations: i) Logical-Shift-Left, ii) Logical-Shift-Right, iii) Rotate-Left, iv) Rotate-Right, v) Rotate-Left with Carry, vi) Rotate-Right with Carry, vii) Arithmetic-Shift-Left and viii) Arithmetic-Shift-Right respectively. The corresponding select signal values are from 24 to 31 as illustrated in Table 1. The logic of this module, LU2 is implemented in behavioural model with logical operators and selection of the operation with a case statement. In this way, coding techniques are used in individual modules to consume less power. The overall design, the top module is implemented in structural model as specified in Fig.1The specifications of the design, the data size is 64-bit, number of control signals: five S4 to S0, number of operations: 32, status of the result: Cout and ZF are the flag indicators to represent carry out and zero flag as shown in Fig. 1.

Table I: List of ALCCU operations and it's select-signal values

Operation Number	Select Signals {S4,S3,S2,S1,S0} =	Operation Name	Operation Number	Select Signals {S4,S3,S2,S1,S0} =	Operation Name
0	00000	Addition	16	10000	Transfer/buffer
1	00001	Addition with carry	17	10001	Inversion
2	00010	Subtraction	18	10010	AND
3	00011	Subtract with barrow	19	10011	OR
4	00100	Multiplication	20	10100	NAND
5	00101	Division	21	10101	NOR
6	00110	increment	22	10110	XOR
7	00111	decrement	23	10111	XNOR
8	01000	Complement	24	11000	Logical Shift Left
9	01001	2's Complement	25	11001	Logical Shift Right
10	01010	Modulus	26	11010	Rotate Left
11	01011	Percentile	27	11011	Rotate Right
12	01100	Even Parity Generator	28	11100	Rotate Left with Carry
13	01101	Odd Parity Generator	29	11101	Rotate Right with Carry
14	01110	Binary to Gray	30	11110	Arithmetic Shift Left
15	01111	Gray to Binary	31	11111	Arithmetic Shift Right

III. FUNCTIONAL VERIFICATION

After the design of ALCCU, testbench module is created. In testbench module, ALCCU is instantiated as a module under test. The testbench applies data to it, and monitors its output using Xsim simulator tool. The advantage of the testbench is used to reduce the testing time and also, the same testbench can be used before and after the synthesis. Specific Test vectors are driven by the test-bench module to the design, to observe the functional behaviour of the ALCCU through waveform result. One sample of simulation result for binary to gray code is shown in Fig. 2.

Fig. 2. Simulated output when S = 14 (gray code conversion from binary)

The simulated results shown in Fig. 2 is gray code after conversion from binary. Here, the given test vector is given to 'a'. The select signal value {S4, S3, S2, S1, S0} = 01110_2=14_d which represents gray code converted from binary (Table. I).

Interpretation of the results shown in Fig. 2:

a = 1111000010101011_H

= 0001 0001 0001 0001 0000 0000 0000 0000 0001 0000 0001 0000 0001 0000 0001 0001_2

= 0001 1001 1001 1001 1000 0000 0000 0000 0001 1000 0001 1000 0001 1000 0001 1001_G

= 1999800018181819 Gray code in Hexadecimal representation

IV. SYNTHESIS ANALYSIS

In synthesis process, the elaborated RTL_design was converted in to logic gate level netlist file [11-12]. In this process, synthesis tool accepts a standard cell library, design constraints file and the RTL design as inputs and generates a gate-level netlist file [11]. The resource utilization of the ALCCU design using Artix 7 FPGA is 22.56% of LUT, 0.93% of Flip Flops, and4.17% of DSPs as illustrated in Table. II.The power analysis of ALCCU is performed with LVCMOS12 is illustrated in Fig. 3. This report is generated on the basis of implemented netlist, constraint files and simulation files. The dynamic power observed for this is 0.003W and static power of the device is 0.111W. As illustrated in Fig. 3, 0.113W of total power on chip has been observed with a clock constraint of 100MHz.

Table II: Utilization Report of ALCCU

Resource	Utilization	Available	Utilization %
LUT	14306	63400	22.56
FF	1177	126800	0.93
DSP	10	240	4.17

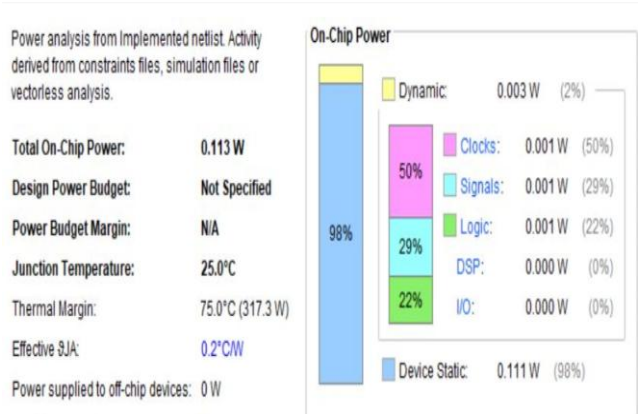

Fig. 3 Power report of ALCCU with 100MHz Clock for LVCMOS12

The total power on chip for various clock constraints range, 10MHz to 20GHz for different input/output standards: LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15 and LVCMOS12 are shown in Figure 4. Similarly, the total on chip power with different clock constraints for LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25 and LVCMOS33 are illustrated in Table.III and Fig. 4.

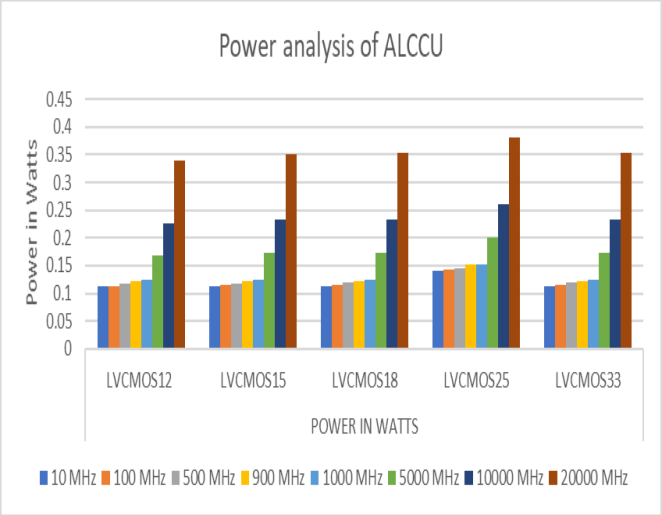

Fig. 4. Power analysis of 64-bit ALCCU with different I/O standards with clock frequencies ranging from 10 MHz to 20000 MHz.

Table III: Power Analysis for different clocks for different I/O standards of LVCMOS

S.No.	Frequency (MHz)	3.3 Power (W)	25 Power (W)	18 Power (W)	15 Power (W)	12 Power (W)
1	10	0.113	0.141	0.113	0.113	0.112
2	100	0.114	0.142	0.114	0.114	0.113
3	500	0.119	0.146	0.119	0.118	0.118
4	900	0.123	0.151	0.123	0.123	0.122
5	1000	0.125	0.152	0.125	0.124	0.124
6	5000	0.173	0.201	0.173	0.172	0.169
7	10000	0.233	0.261	0.233	0.232	0.226
8	20000	0.353	0.382	0.353	0.352	0.339

Table IV: Timing report of the 64_bit ALCCU

Setup time	Hold time	Pulse Width
Worst Negative Slack = 25.175ns	Worst Hold Stack = 0.005ns	Worst Pulse Width Stack =15.250ns

The worst negative slack of setup time is 25.175ns, the worst hold stack of hold time is 0.005ns and worst pulse width stack of 15.250ns of timing report is shown in Table IV.

V. RESULTS AND DISCUSSION

The ALCCU consists of two 64-bit inputs: a and b, seven scalar inputs: clk, cin, S0, S1, S2, S3, S4 and one 64-bit output: ALU_CC, two scalar outputs: Cout and ZF. The total number of inputs and outputs together are 201. Therefore, virtual input and output core which is used to monitor and drives FPGA internal signals in the real time [1].

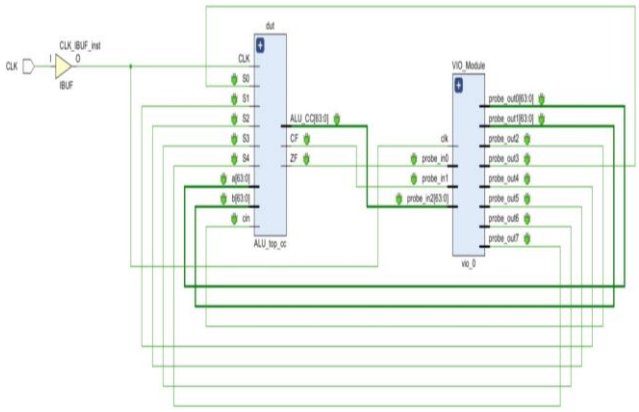

Fig. 5. Interfacing of VIO and ALCCU(DUT)

Here, the two data inputs, a and b are of 64-Bit length and select signals: S4, S3, S2, S1 and S0 are the outputs of virtual I/O Block (actually, these signals are actual inputs to ALCCU). The outputs of ALCCU, ALU_CC, Cout and ZF are given as inputs of the virtual I/O block. The design module and VIO block are used as sub components in top module as shown in Fig. 5. To maintain synchronism, common clock is given to both VIO and design modules.

Name	Value	Activity	Direction	VIO
a[63:0]	[H] 1111_0000_1010_1011		Output	hw_vio_1
b[63:0]	[H] 1010_1010_1010_1010		Output	hw_vio_1
ALU_CC[63:0]	[H] 1E1E_0000_1FE0_1FE1		Input	hw_vio_1
S4	[B] 0		Output	hw_vio_1
S3	[B] 1		Output	hw_vio_1
S2	[B] 1		Output	hw_vio_1
S1	[B] 1		Output	hw_vio_1
S0	[B] 1		Output	hw_vio_1
cin	[B] 0		Output	hw_vio_1
CF	[B] 1		Input	hw_vio_1
ZF	[B] 0		Input	hw_vio_1

Fig. 6. Gray to Binary Operation for S=15 observed at Hardware VIO Window

The output results of Gray to Binary operation with a select signal value S=15 obtained at the Hardware VIO Window, is illustrated in Fig. 6.

Table V: Comparison of proposed work with existed work.

Parameter	References [4,5,6]	Reference [7]	Proposed work
Technology	28 nm CMOS	28 nm CMOS	28 nm CMOS
Data Size	32-bit	32-bit	64-bit
Number of Operations	32	32	32
Clock Frequency	10 MHz	Up to 5000MHz	Up to 20000MHz
Total on Chip Power	0.123W	0.095W	0.353W

VI. CONCLUSION

The proposed 64_Bit ALCCU is successfully designed, verified and implemented with low power. This design is implemented with functional distributed modules in structural model and efficient RTL coding in each sub module of the design to obtain low power. Satisfactory low power is observed for clock frequencies: 10, 100, 500, 900, 1000, 5000, 10000 and 20000 MHz. All these clock constraints are applied on different input/output standards: LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15 and LVCMOS12 are as shown in Fig. 4. The proposed work can be extended to 128_bit and beyond 128-bit.

REFERENCES

1. Xilinx, Virtual Input/Output v3.0 LogiCORE IP Product Guide (PG159), Vivado Design Suite, PG159 October 4, 2017.
2. Vivado Design Suite User Guide: Getting Started, UG910 (v2017.1) April 5, 2017.
3. Hui zhang, Zhi-Qiang Wang, Wei Liu and Zheng Tan, "The Design of Arithmetic Logic Unit Based on ALM", 2012 International Workshop on Information and Electronics Engineering (IWI-EE), http: www.elesevier.com/locate/procedia.
4. N. Gaur, A. Mehra, D. Kamboj and D. Tyagi, "A novel implementation of 32 bit extended ALU Architecture at 28nm FPGA"International Conference on Emerging Trends in Communication Technologies (ETCT), Dehradun, pp. 1-4, 2016. doi: 10.1109/ETCT.2016.7882932.
5. Dharmavaram Asha Devi and Sai Sugun L, "Design, Implementation and Verification of 32-Bit ALU with VIO" IEEE International Conference on Inventive Systems and Control (ICISC), Coimbatore 2018.
6. B. Pandey, J. Yadav and M. Pattanaik, "IO standard based energy efficient ALU design and implementation on 28nm FPGA," 2013 Annual IEEE India Conference (INDICON), Mumbai, pp. 1-5, 2013. doi: 10.1109/INDCON.2013.6725996.
7. Dharmavaram Asha Devi, Sandeep Chintala, Sai Sugun L, "Design of Power Efficient 32-Bit Processing Unit", International Journal of Engineering & Technology, 7 (2.16) (2018) 52-56.
8. Rakhi Nangia, Neeraj Kr. Shukla "Resource Utilization Optimization with Design Alternatives in FPGA based Arithmetic Logic Unit Architectures", International Conference on Computational Intelligence and Data Science ICCIDS 2018 published in Procedia Computer Science 132 (2018) 843-848.

9. Dharmavaram Asha Devi, FPGA Design Flow for 8-bit ALU using Xilinx ISE, International Journal of Modren Electronics and Communication Engineering, ISSN:2321-2152, Volume.No.4, Issue.No.2, March 2016.
10. http://anysilicon.com/vlsi-design-flow-overview/
11. Pong P Chu "FPGA Prototyping By Verilog Exampes" A John Wiley & Sons, Inc, 2008.
12. Samir Palnitkar, Verilog HDL A Guide to Digital Design and Synthesis, Second Edition, IEEE 1364-2001 Compliant, Pearson Publications.
13. Vivado Design suite User Guide, Power Analysis and Optimization, UG907 (v2017.3) October 4, 2017.

AUTHORS PROFILE

Dharmavaram Asha Devi, Member IEEE, Fellow IETE. The Author is working as a Professor in the Department of Electronics & Communication Engineering, SNIST, Hyderabad. She became an Associate Member of IETE in Dec-2000 from the Institute of Electronics and Telecommunication Engineering, New Delhi, India. She awarded M.Tech. Degree in Digital Systems and Computer Electronics from JNTU Anantapur in 2005. She achieved a Doctorate Degree from Sri Krishnadevaraya University, Anantapur in Dec 2011, for her research contribution in Embedded System based Soil Analysis under the supervision of Prof. K. Malakondaiah, from SKU, Anantapur. She had 16 years of academic, including 8 Years of R & D Experience. She has published more than 25 papers in International Journals and presented 40+ research papers in National and International level conferences on behalf of her research work done in Embedded Systems and VLSI Designs.

Dr. M. Suresh Babu, has 22 years of teaching experience in MCA and Computer Science Engineering departments. He awarded PhD degree in Computer Science from Sri Krishnadevaraya University, Anantapur, for his contribution on "A study on forecasting stock market index value using data mining techniques" in 2012. He achieved M.Phil (Computer Science) from Bharthiar University in 2007 and Master of Computer Applications from Osmania University,Hyderabad in 1997. He published papers around 90+ in various National and International level Journals and conferences. His area of research interest is data where house, DBMS & RDBMS and Ubiquitous computing.