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A New Topology on Twenty one level Inverter with Reduced Number of Switches

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Abstract: ***The Multilevel inverters are known for their high power capability and reliability. They produce the output in the form of staircase waveform. If the number of level increases then almost perfect sine wave can be attained at the output. The increase in number of levels improves the power quality but it also increases the complexity in control and cost, which will increase the switching losses also. Hence there is a need for research in the multilevel inverter topology to have reduced number of switches for increased levels than the conventional and pre-proposed topologies. The purpose of this paper is to design the new topology on multilevel inverter with reduced switching devices.***

Index Terms: ***Multilevel inverter (MLI) topology, power electronic switches, Reduced THD***

I. INTRODUCTION

The multilevel inverter is the converter which converts the dc input to ac output. The output of multilevel inverter is in staircase formin order to get closer to sinusoidal waveform. The perfection can be improved with increased number of levels and angle optimization of gate signals.The multilevel inverters start from three levels. As the number of levels reach infinity, the output THD approaches zero Because of its low maintenance cost and high power rating, Multilevel inverter are most suitable in Renewable energy sources where they can be easily connected to the photovoltaic cells, fuel cells, etc.

Multilevel inverter are classified into three different topologies namely (a) Diode clamped /Neutral clamped Multilevel Inverter (b)Flying capacitors /Capacitor clamped Multilevel Inverter (c) Cascaded H-bridge Multilevel Inverter.

Among these topologies Cascaded H-Bridge is mostly preferred which can be both series and parallel connected. In Diode Clamped topology more number of diodes have to be used. Similarly in Flying capacitor topology more number of capacitors are to be used which will increase the capacitor voltage balancing problem and cost.

II. PROPOSED TOPOLOGY ON MULTILEVEL INVERTER

The proposed topology is modeled in order to overcome the limitations discussed above. In proposed topology the number of switching devices and dc sources are reduced when compared to pre-proposed topologies. Here the Twenty one level inverter with asymmetric dc sources is modeled to verify its efficiency and working.

The proposed model for Twenty one level inverter consists of ten switches and fourasymmetricdc sources. The switches from Sw1 to Sw6 are Main circuit switches which contributes towards the level increment whereas the switches from Sw7 to Sw10 are Auxiliary switches which aids in achieving positive and negative halves. Resistive load is used in the model. The new topology on 21 level inverter is shown below in Fig.1.

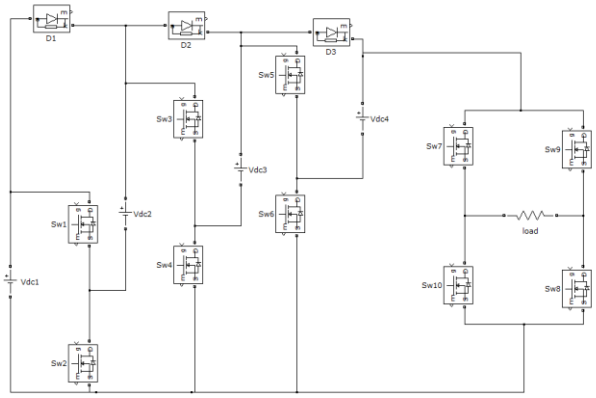

Fig.1 Twenty One Level Inverter Topology

III. MODES OF OPERATION

MODE 1:

In mode1 the switches Sw7 and Sw8 areswitched into on mode which will give outputvoltage Vdc1across the load.
The output voltage level V1=Vdc1.
Diodes D1, D2 and D3 are forward biased in this mode. Switches Sw7 and Sw8 are turned on to produce positive half levels. Similarly switches Sw9 and Sw10 are switched on to give negative half levels at the output.

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Fig.2 Mode1

MODE 2:

In mode2 the switch Sw2 is made on to givevoltage Vdc2 across resistive load. The output voltage level V2=Vdc2. Diodes D2 and D3 are forward biased in this mode.

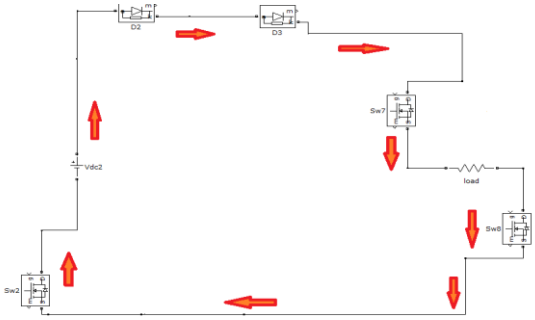

Fig.3 Mode2

MODE 3:

In mode3 the switch Sw2 is made off and switch Sw4 is turned on to give voltageVdc3 at the load. In mode3 the output voltage level V3=Vdc3. Diode D3 is forward biased in this mode. The current flow in the circuit is shown below in Fig.4.

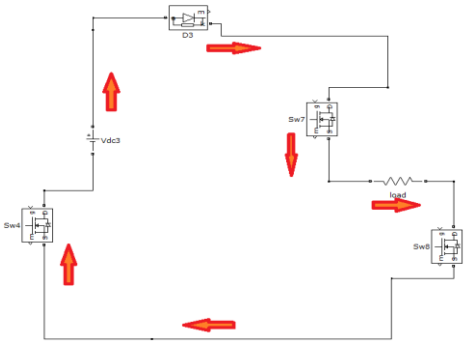

Fig.4 Mode3

MODE 4:

In mode4 the switch Sw3 is off and switch Sw6 is turned on to produce Vdc4 voltage across the load. The output voltage level V4=Vdc4. No Diode conducts in this mode.

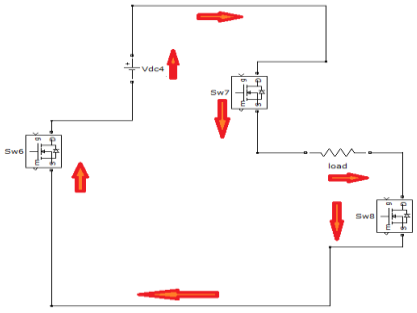

Fig.5 Mode4

MODE 5:

In mode5 the switch Sw6 comes to off state and switch Sw5 is turned on to produce voltage (Vdc1+Vdc4) across the load.

The output voltage level is V5=Vdc1+Vdc4. Diodes D2 and D3 are forward biased in this mode.

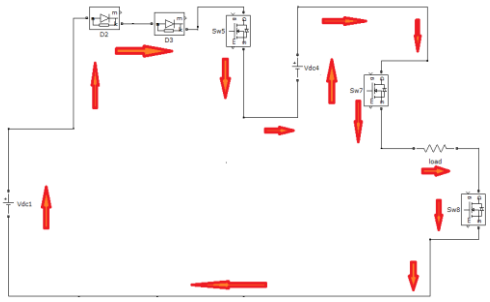

Fig.6 Mode5

MODE 6:

In mode6 the switch Sw6 is turned off and switches Sw2 and Sw5 are switched on to provide Vdc2+Vdc4 voltage across the load. The output voltage level V6=Vdc2+Vdc4. Diode D3 is forward biased in this mode.

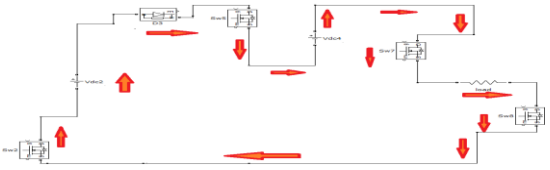

Fig.7 Mode6

MODE 7:

In mode7 the switches Sw4 and Sw5 are switched on to give Vdc3+Vdc4 voltage at the load. The output voltage level V7=Vdc3+Vdc4. No Diode conducts in this mode.

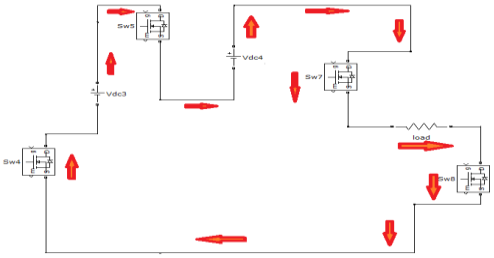

Fig.8 Mode7

MODE 8:

In mode8 the switches Sw3 and Sw5 are switched on to provide Vdc1+Vdc3+Vdc4 voltage across the load.

The output voltage level V8=Vdc1+Vdc3+Vdc4. Diode D2 is forward biased in this mode.

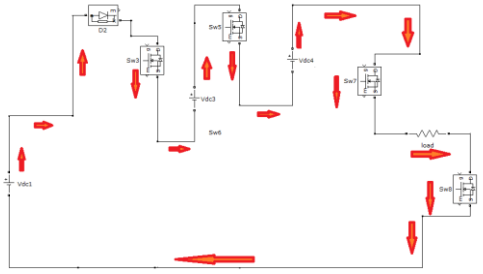

Fig.9 Mode8

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MODE 9:

In mode9 the switches Sw2, Sw3 and Sw5 are turned on to produce Vdc2+Vdc3+Vdc4 voltage across the load. The output voltage level V9=Vdc2+Vdc3+Vdc4. No Diode conducts in this mode.

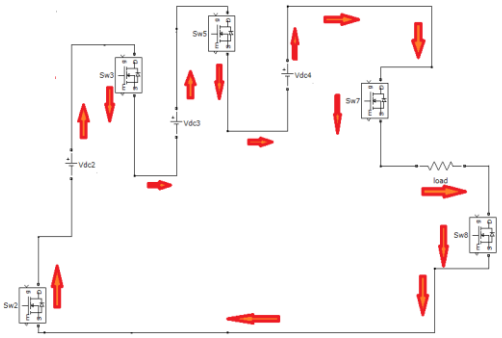

Fig.10 Mode9

Mode 10:

In mode10 the switches Sw1, Sw3 and Sw5 are turned on to produce Vdc1+Vdc2+Vdc3+Vdc4 voltage across the load. The output voltage level V10=Vdc1+Vdc2+Vdc3+Vdc4.

No Diode conducts in this mode.

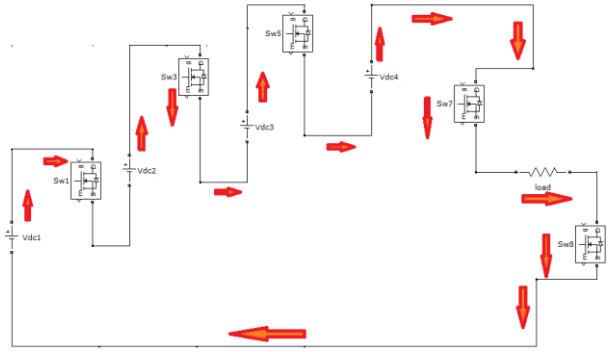

Fig.11 Mode10

IV. SWITCHING TABLE

The switching sequence for the proposed model is shown in the below Table.1.

Whereas S1, S2,…….S10 represents the Switches 1 to 10 respectively.

Output Voltage levels are represented by V1, V2, ……V10. The Voltage levels are V0=0V, V1=Vdc1, V2=Vdc2, V3=Vdc3, V4=Vdc4, V5=Vdc1+Vdc4, V6=Vdc2+Vdc4, V7=Vdc3+Vdc4, V8=Vdc1+Vdc3+Vdc4, V9=Vdc2+Vdc3+Vdc4, V10=Vdc1+Vdc2+Vdc3+Vdc4.

Thus the above said levels are given positive and negative signs with the help of Auxiliary switches S7, S8, S9, S10. Switches S7 and S8 are turned on for positive half cycle and Switches S9 and S10 are turned on for Negative half cycle.

I. SWITCHING TABLE FOR POSITIVE HALF CYCLE

Output voltage levels	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
V0	0	0	0	0	0	0	0	0	0	0
V1	0	0	0	0	0	0	1	1	0	0
V2	0	1	0	0	0	0	1	1	0	0
V3	0	0	0	1	0	0	1	1	0	0
V4	0	0	0	0	0	1	1	1	0	0
V5	0	0	0	0	1	0	1	1	0	0
V6	0	1	0	0	1	0	1	1	0	0
V7	0	0	0	1	1	0	1	1	0	0
V8	0	0	1	0	1	0	1	1	0	0
V9	0	1	0	0	1	0	1	1	0	0
V10	1	0	1	0	1	0	1	1	0	0

The Switches Sw9 and Sw10 conducts for negative half cycle for the same above mentioned voltage levels. Thus 21 levels of output voltage is obtained. (Say +V1, +V2, +V3, +V4, +V5, +V6, +V7, +V8, +V9, +V10, 0V, -V1, -V2, -V3, -V4, -V5, -V6, -V7, -V8, -V9, -V10 levels).

V. SIMULATION RESULTS

The simulation of the proposed Twenty one level Inverter is simulated using MATLAB Simulink software. The MATLAB Simulink diagram of the proposed model is shown in figure Fig.12 below.

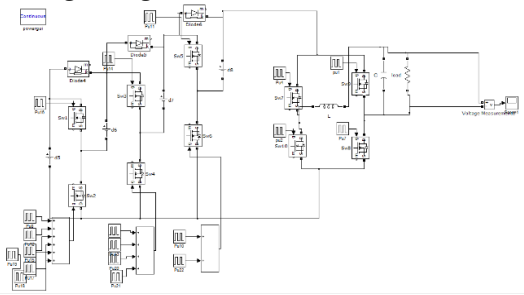

Fig.12 Simulation Circuit Diagram (With Filter Design)

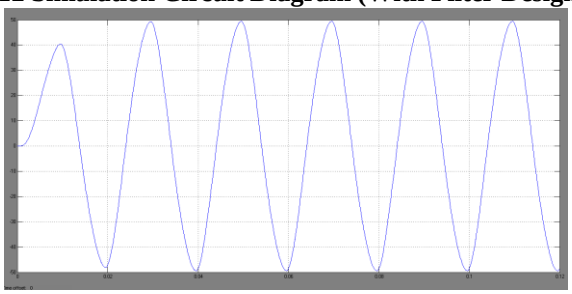

Fig.13 Output Voltage Waveform with filter circuit.

The FFT Analysis of the proposed model with filter design is shown below. The Reduced THD thus obtained adds the advantage to the model.

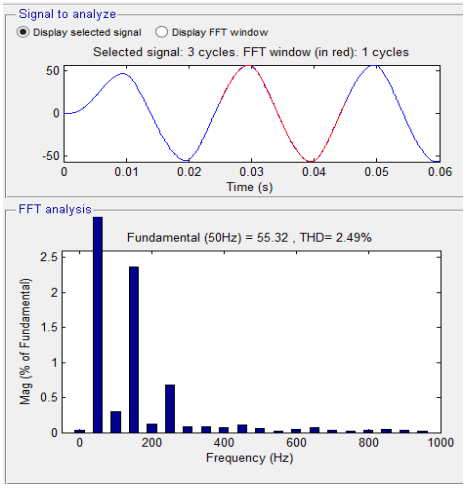

Fig.14 FFT Analysis of proposed twenty one level inverter(with filter).

The following figure shows the output of 21 level inverter without filter model.

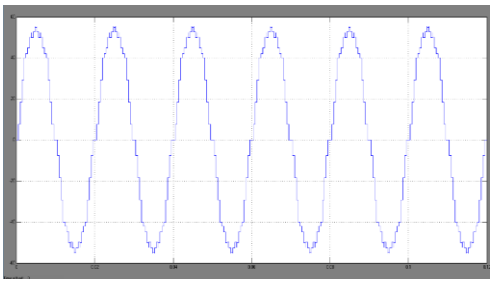

Fig.15 Output voltage of 21 level inverter without filter model.

II.COMPARISON OF NUMBER OF PARAMETERS AMONG VARIOUS TOPOLOGIES OF TWENTY ONE LEVEL INVERTER

Parameters	Diode clamped	Capacitor clamped	Cascaded H- Bridge	Proposed model
Switches	**40**	**40**	**40**	**10**
Clamping diodes	**380**	**0**	**0**	**3**
Balancing capacitors	**0**	**190**	**0**	**0**

The Comparative details of the switches and diodes used in conventional topologies and the proposed model is shown in above table. Thus the objective of the paper is satisfied.

VI. HARDWARE IMPLEMENTION ON PROPOSED MODEL

The hardware circuit for the proposed model is designed and its working is verified for its given objectives. The hardware circuit and output waveform is shown below in consecutive figures respectively.

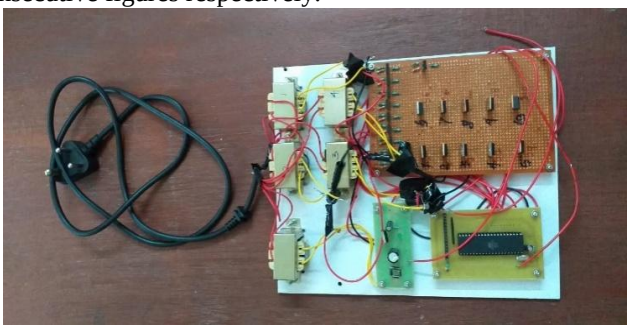

Fig.15 Hardware circuit of proposed model

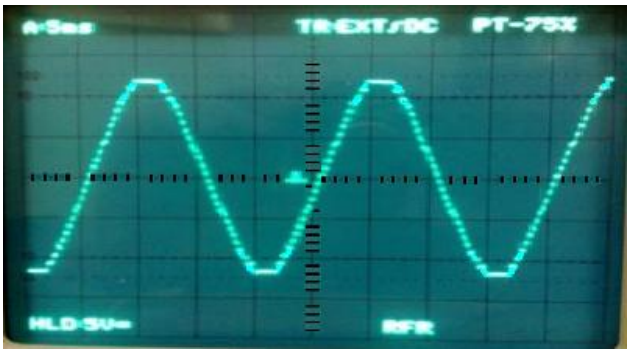

Fig.16 Output voltage

VII. CONCLUSION

The new proposed model of the multilevel inverter is modeled and its working is analyzed. The topology proposed in this paper is also compared with the conventional topologies and the objective of the paper is obtained. Thus the switching devices count is reduced to about four times than the conventional topologies.The MATLAB Simulink simulation software is used to verify the working of the proposed model and hardware is also designed for the new topology. The simulation results are also showcased to prove the success of the proposed model. The FFT Analysis provides the additional advantage to the paper with reduced Total Harmonic Distortion (THD) of **2.49%.** To obtain this value of THD, no any optimization algorithm or closed loop control is used. Hence the circuit complexity is reduced and efficiency of the system is also improved.

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