

High-Precision Current Conveyor Based on BDQFG Miller Ota



Narsaiah Domala, G. Sasikala

Abstract: The paper presents a sub-volt design of highly precise second-generation current conveyor ($CCII \pm$) using Miller compensated Operational Transconductance Amplifier (OTA) designed using bulk driven quasi-floating gate (BDQFG) MOSFET. The bulk-driven approach help in working of proposed $CCII \pm$ at low supply voltage. Moreover, followed BDQFG technique results in improves the transconductance and frequency response of the circuit over standalone bulk-driven technique. The proposed $CCII \pm$ operates at $\pm 0.4V$. Other performances which encourage its wide applicability are in terms of high current range and high bandwidth. The analysis of proposed current conveyor is carried in $0.18 \mu m$ twin-well CMOS technology using HSpice.

Index Terms: Bulk Driven Quasi-floating gate MOSFET, Current conveyor, Bandwidth, supply, Power.

I. INTRODUCTION

Low power, low cost portable handheld devices demand has been a continuous motivation factors for IC industries. However, the trend of device shrinkage and low supply usage has puts a stress mark on the analog designers due to various factors among which the threshold voltage of MOSFET is the main cause. The problem arises when the threshold of MOSFET is higher than the supply voltage. Among solutions to the aforementioned problem the most likely used approaches are subthreshold operation, forward bias bulk source potential etc. However using the low threshold MOST devices these issues can be overcome but at the same time the approach may not be cost effective. Alternative solution can be use of non-conventional structures of MOSFET, i.e. other than gate driven MOSFET, namely: floating gate (FG) MOSFET, quasi floating gate (QFG) MOSFET, bulk-driven (BD) MOSFET and bulk-driven floating gate (BDFG) and quasi-floating gate (BDQFG) MOSFETs [1]. The QFG MOS transistors are wide-band ac coupled circuits and offer better linearity at low voltage. A number of low voltage designs

achieved using QFG MOSFET can be found in literature for example- a linear programmable CMOS OTA, MOS resistor, GM-C filter, current mirror etc. Alternate to QFG, the widely adopted technique for low power circuits design is the BD MOSFET. The BD MOSFET being simple in realization have been extensively used in the design of various circuits [1]. But these MOSFET suffers from low gain due to poor body transconductance and sensitivity to device mismatch and process variations. Various efforts have been exerted to overcome these issues but at the cost of increased circuit complexity and the power. However, with the advent of BDQFG approach [2] the BD drawbacks were overcome. The BDQFG MOSFET is basically operating a BD MOSFET in QFG mode due to which the transconductance of MOSFET gets increased, i.e. effective transconductance becomes the sum of body transconductance and QFG transconductance. A number of articles has been published based on BDQFG approach out which few recently reported are in design of transconductor, current conveyor, differential difference amplifier, low voltage current mirrors etc. To briefly outline the advantage of BDQFG technique, in this paper a low voltage (LV) low power (LP) dual polarity second generation current conveyor ($CCII \pm$) based on two-stage Miller compensated OTA is presented. The simulation results achieved indicates the proposed $CCII \pm$ to be best suited for high frequency low power applications. The paper is organized as follows: section 2 outlines a short discussion on BDQFG MOSFET followed by the design of highly precise $CCII \pm$ in section 3. The simulations are shown in section 4 followed by conclusion in section 5.

II. BDQFG MOSFET

The MOSFET in general is said to be a four terminal device whose fourth terminal known as bulk; is usually connected to the supply rails, i.e. negative/positive supply rail for N-channel/P-channel MOSFET respectively. However, the bulk instead can be used as a secondary gate which can offer threshold free path to input signal. In bulk driven, the input signal given at bulk thus modulates the drain-to-source current which can be done even with very small amplitude of input signal. However, the main drawback with BD MOS transistor is its small body transconductance (g_{mb}) and degraded frequency response. The BDQFG technique overcomes the issues of BD in terms of transconductance and bandwidth by using QFG MOSFET in BD mode. The effective transconductance for BDQFG is given by

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$$g_{m,BDQFG} = g_{m,qfg} + g_{m,BD} = \frac{(C_{in} + C_{qf gb})}{C_{T,qfg}} g_m + g_{mb} \quad (1)$$

where $C_{T,qfg} = C_{in} + C_{qf gb} + C_{gd,MP} + C_{qf gd} + C_{qf gs}$ is the sum total capacitance. As observed the effective transconductance of BDQFG is greater than the body transconductance (g_{mb}) by $g_{m,qfg}$. The schematic of BDQFG MOSFET is shown in Fig. 1 where the bulk is tied to the gate input terminal of QFG MOS transistor M1.

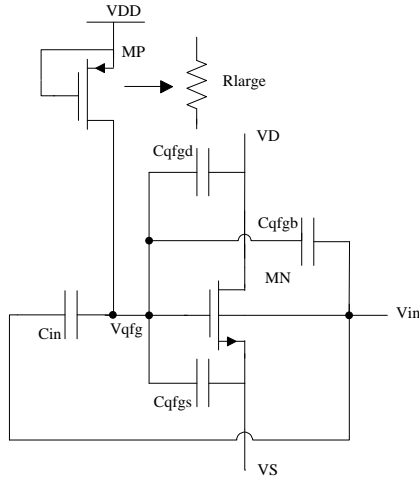


Fig. 1. N-Channel BDQFG NMOS transistor

Under AC, the BDQFG structure combines the features of BD and QFG MOSFET whereas for DC it works as simple bulk driven MOSFET.

III. PROPOSED HIGH PRECISION CCII

The second-generation current conveyor is a 3-port device is defined by

$$V_X = V_Y \quad (2)$$

$$I_{Z\pm} = \pm I_X \quad (3)$$

where X and Y are the input terminals and $Z+$ and $Z-$ are the output nodes. The matrix representation of $CCII \pm$ is given by

$$\begin{bmatrix} V_X \\ I_{Z\pm} \\ I_Y \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \pm 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{Z\pm} \end{bmatrix} \quad (4)$$

From (1), the ideal condition of impedance at various nodes can be observed, i.e. the X terminal should be at low impedance node whereas Y , $Z+$ and $Z-$ should be at high impedance node. Related work in design of low voltage low power second generation current conveyor ($CCII$) can be observed in [2-6]. In this paper, to design of highly precise $CCII \pm$, the topology uses one dual output $CCII+$ and one single output $CCII+$. The architecture of highly precise $CCII \pm$ is shown in Fig. 2 which uses one Dual output BDQFG $CCII+$ and one single output BDQFG $CCII+$.

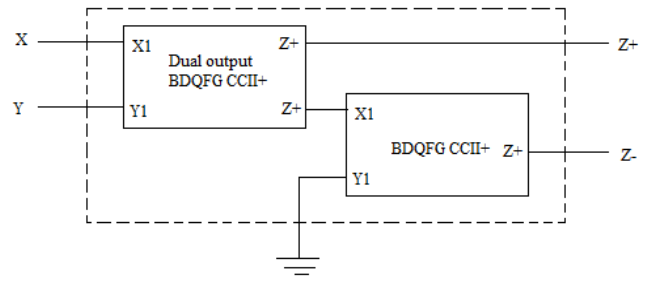


Fig. 2. Highly-precise $CCII \pm$ based on BDQFG Miller OTA

In order to design the positive type $CCII$, BDQFG based Miller OTA is assumed. The structure of proposed LV LP positive type second generation current conveyor based on Miller BDQFG OTA is shown in Fig. 3.

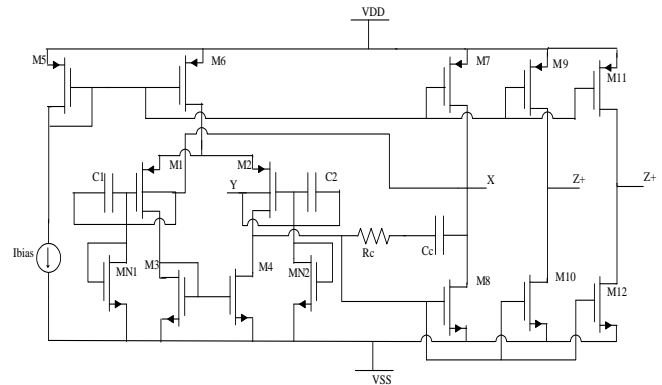


Fig. 3. Dual Output $CCII$ based on BDQFG Miller OTA

The proposed $CCII$ consists of Miller BDQFG OTA (M1-M8) realized in a unity gain buffer mode, done by sorting the output to the negative input terminal of OTA. The positive input terminal is assumed as Y terminal while the negative terminal is labelled as X terminal. The rest pair of MOS transistors (M9, M10) is used for producing positive Z terminal. The MOSFET (M3, M4) and (M5, M6, M7) combinations are simple current mirror realizations. The biasing current (I_{bias}) is used to bias the amplifier. The capacitor C_c is used as miller compensation which improves the phase response of OTA. The rest pair of MOS transistors (M9, M10) is used for producing $Z+$ terminal and (M11, M12) replica the $Z+$ terminal. In literature design of accurate $CCII+$ has been reported frequently. However, for obtaining I_{z-} the general approach followed is using cross-coupled current mirror. Though the technique is simple but as the current path through $Z+$ and $Z-$ is not symmetrical which leads mismatch in outputs of Z terminal. Following the approach of Fig. 2, results in very high symmetry of the $CCII \pm$ thereby resulting in precise output terminal currents, i.e. at $Z+$ and $Z-$ terminal.

IV. SIMULATION RESULTS

The proposed LV LP $CCII \pm$ is simulated on $0.18 \mu m$ twin-well CMOS technology of UMC with the help of HSpice simulator.

The dimensions of MOSFET used in design CCII± is shown in Table 2. The values of other parameters assumed for CCII± are $R_c=10K$, $C_c = C_1 = C_2=1pf$ and a bias current I_{bias} of $10 \mu A$. The simulation results of the proposed LV LP CCII are shown in Fig. 4 to Fig. 9.

Table 1. Dimension of MOSFET used in CCII±

MOSFETs	W (μm)	L (μm)
M1-M4	12	0.6
M5	4	0.6
M6	9	0.6
M7, M9, M11, M12	8	0.6
M8, M10	23.9	0.6
MN1, MN2	0.36	0.36

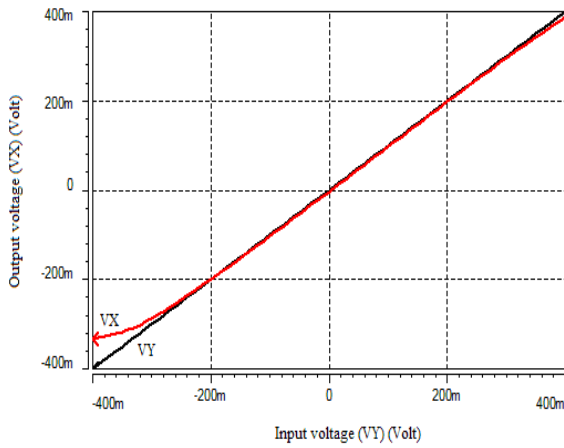


Fig. 4. DC curve of V_x versus V_y .

The fig. 4 shows the DC transfer characteristic, i.e. V_x versus V_y where V_x shows signal swing form $-0.3V$ to $+0.3V$ with minimal offset. The current transfer curve for I_{Z+} and I_{Z-} is shown in Fig. 5 where linearity in the range from $-20 \mu A$ to $+20 \mu A$ with the minimal error is observed. The DC range of linear operation is suitable for various low power applications. The frequency response of V_x/V_y is shown in Fig. 6 which shows a bandwidth of $17MHz$.

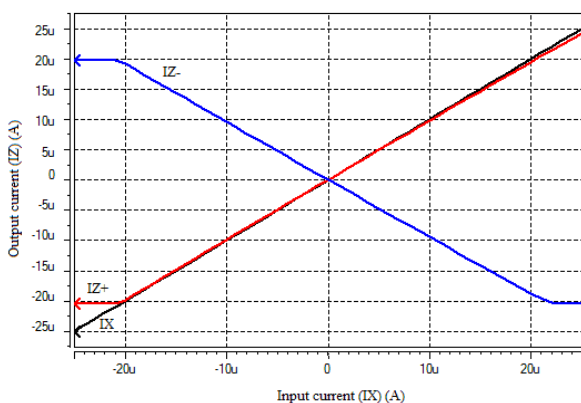


Fig. 5. DC curves of I_{Z+} and I_{Z-} with respect to I_x .

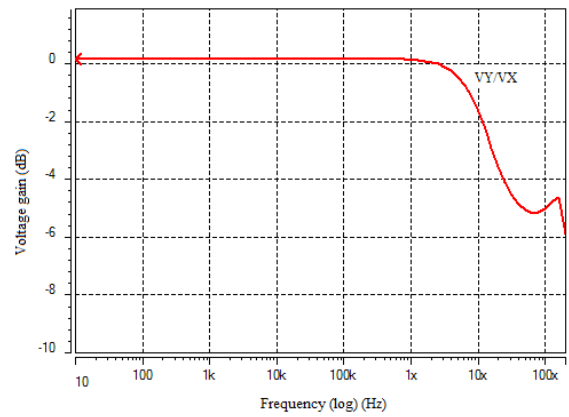


Fig. 6. Frequency responses of voltage gain (V_x/V_y)

The bandwidth response of I_{Z+}/I_x and I_{Z-}/I_x is shown in Fig. 7. The observed bandwidth of I_{Z+}/I_x is $326MHz$ and for I_{Z-}/I_x is $302MHz$. Such high bandwidth suits the proposed architecture for high speed applications.

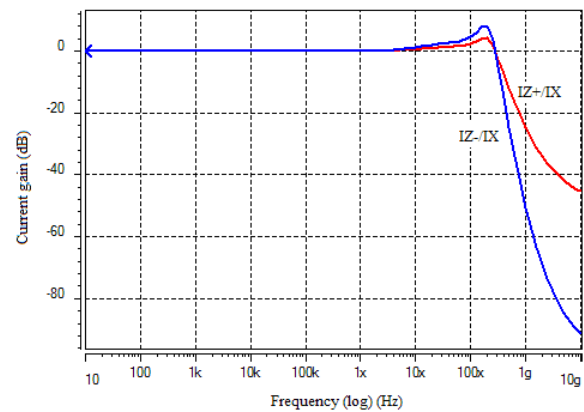


Fig. 7. Frequency responses of current gain (I_{Z+}/I_x and I_{Z-}/I_x)

In fig. 8 and 9, the frequency dependence of the parasitic impedances of X and $Z+$ & $Z-$ terminals is shown respectively. At low frequency impedance at X is 444 ohm and at $Z+$ and $Z-$ the impedance is $110 K\Omega$ and $117 K\Omega$ respectively.

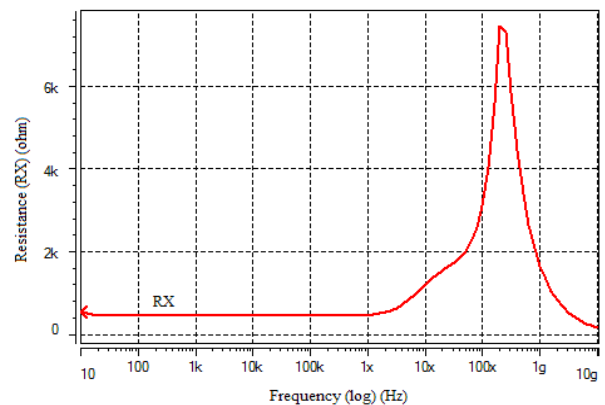


Fig. 8. Parasitic impedance of X terminal

Table 2. Comparison of Proposed CCII± with prior CCII+ & CCII±

Parameters	[2]	[3]	[4]	[5]	[6]	Proposed CCII±
DC range (Volt)	-0.4 to +0.4	-0.38 to +0.38	-0.5 to 0.5	-0.65 to +0.65	-0.63 to +0.25	-0.3 to 0.3
V_X/V_Y (Hz)	18M	14M	4.8M	10.5M	1.05G	17M
Current gain	1	1	1	0.995	1.006	1
I_{Z+}, I_{Z-} (mA)	-0.09 to +0.09	-0.007 to +0.007	-0.03 to +0.03	-0.1 to +0.1	-0.1 to +0.1	-0.02 to +0.02
I_{Z+}/I_X (Hz)	19M	13M	82M	62M	32M	326M
I_{Z-}/I_X (Hz)	----	12.5M	----	----	----	302M
R_X (ohm)	10.3	27	42	6	15	444
R_{Z+} (ohm)	6.28M	0.89K	53M	----	----	110K
R_{Z-} (ohm)	----	0.89K	----	----	----	117K
Power Supply (Volt)	10 ± 0.4	64 ± 0.4	10 ± 0.5	123 ± 0.75	234 ± 1.5	131 ± 0.4
Technology	0.18 μm	TSMC 0.18 μm	0.18 μm	0.35 μm	0.5 μm	UMC 0.18 μm

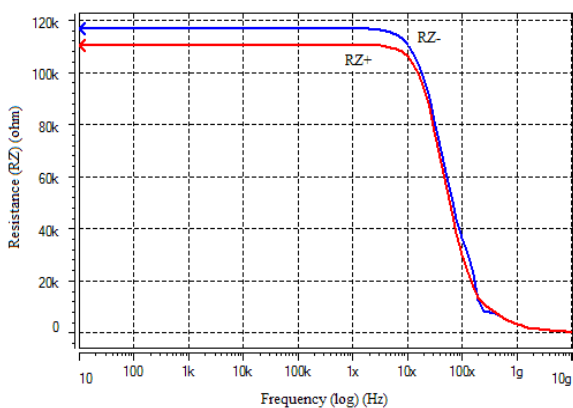


Fig. 9. Parasitic impedance of Z+ and Z- terminal

The complete simulation results are summarized in Table 2. Also the comparison of proposed CCII± with existing CCII+/CCII± reported in literature is shown in Table 2.

V. CONCLUSION

Among the various LV LP techniques have been reported in literature, BD MOSFET is considered as more suitable for its simple configuration but due its sensitivity to device mismatch, poor gain and frequency performances, the structure has its adaptability only to low gain and low frequency applications. Using BDQFG in place of BD improves the performances. Based on BDQFG the paper presents a CCII± based on Miller OTA. Simulations in HSpice using industry provided technology UMC 0.18 μm encourages its applicability to real environment.

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