

# Low Power High Speed Arithmetic Circuits



Kiran Kumar V G, C Shantharama Rai

**Abstract:** In the Design of arithmetic circuits reducing area, high speed and power are the major areas in VLSI system design. In this paper parallel prefix adders like Kogge-stone adder, Brent-Kung adder, Ladner-Fischer adder is designed. Radix-4 Booth multiplier is designed by using Kogge-Stone adder. 16 bit Vedic multiplier is done by using Urdhwa Triyambaka sutra. 8bit Vedic division is implemented by using Crumbs method so as to reduce the area, LUT tables and increase the speed as well as to reduce the Power dissipation. The design is synthesized using Xilinx ISE 14.1 design suite.

**Index Terms:** Kogge-stone adder, Brent-Kung adder, Ladner-Fischer adder. Radix-4 Booth multiplier.

## I. INTRODUCTION

Arithmetic circuits uncover abundant applications in processing architectures. As the complication of DSP architectures is relatively higher, low power design techniques are now very promising. In the era of Internet of Things, Artificial Intelligence and Machine learning, there has been a tremendous research in the area of resource constrained devices, hence the tremendous growth research in low power VLSI system design arises from two main facts, one, as the operating frequency and processing capacity of the chip increases hence the currents to be delivered and heat dissipated increases thus proper cooling techniques has to be provided. Secondly the battery life of such resource constrained devices can be increased resulting in extended operating time. Pervasive work is performed on low-power multipliers at physical, circuit and logical levels, resulting in the design of several parallel multipliers with different area, power and speed constraints.

In this paper, the basic arithmetic operations in like addition, subtraction, multiplication and division are implemented. In the digital system design the most commonly performed arithmetic operation is addition, in this paper three different adders have been implemented. Adder is a digital circuit which performs addition of two n-bit elements and generates (n+1) bits as a sum and carry. An adder can be converted into

subtractor. For subtraction, two elements are considered from which one element is unsigned and another is signed number. A signed number is then converted into unsigned number using two's complement criteria. Both the unsigned and the result of two's complement are added and results are obtained as difference and borrow.

This paper also deals with multiplication; the two numbers are multiplied using the Vedic technique. The term 'veda' denotes storehouse of knowledge. In Vedic multiplier there are 16 sutras but the best among all is Urdhva Tiryakbhyam. In today's world, multipliers play an important role in many high-performance systems such as, Digital Signal Processors, Microprocessors, ALU etc.

The performance of a system is generally examined by the multiplier's performance, as the multiplier is generally the slowest element in the system and usually consumes more space and power and long latency. Therefore, low-power with high speed multiplier design has been an important part in low-power VLSI system design. The divider circuit deals with the design of signed division which divides a number by another number with the signed bit and output are obtained as quotient and remainder.

## II. LITREATURE REVIEW

### A. Review Stage

In paper [1], the comparisons between several kinds of adder are made. The design of various adders such as Ripple carry adder Carry look ahead adder, Carry save adder, Carry select adder, Carry skip adder, Carry increment adder, and Carry bypass adder are discussed. On the basis of their performance parameter each of these adders are compared such as area, power and delay. In [2] the 4-bit, 8bit, 16bit and 32bit Brent Kung Adders have been implemented and simulated using CMOS logic- 45nm Technology. The results have been compared with Ripple Carry adder and Carry Look-ahead adders, a comparative study was conducted. Booth multiplier was implemented by using similar type of adders like CSA Ripple carry adder and so on. Booth multiplier was implemented by using CSA. In CSA area, delay was increased so Kogge-stone is used by which Modified Booth multiplier can be implemented which is explained in the paper [3]. In paper [4], two techniques based upon Vedic maths to improve processor speed have been implemented. There are at total 16 sutras in Vedic mathematic from which two are for multiplication application. The two methods discussed here in the paper are firstly Urdhava Triyakbhyam technique or sutra is similar to array multiplication. The gate delay, number of bit and area is increased slowly when comparison is made with other multipliers.

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And so the second and the advanced technique called NIKHILAM sutra is discussed. Faster mental calculation could be achieved from these sutras. This paper compares the two techniques and finds that NIKHILAM is the best. Here for the processor speed to be increased, this paper discusses techniques for modification of architecture of vedic multiplier. In paper [5] Parvartya yojayet algorithm is been implemented. High performance divider could be developed from this divider algorithm. To the Vedic divider and the conventional divider, static timing analysis is done here.

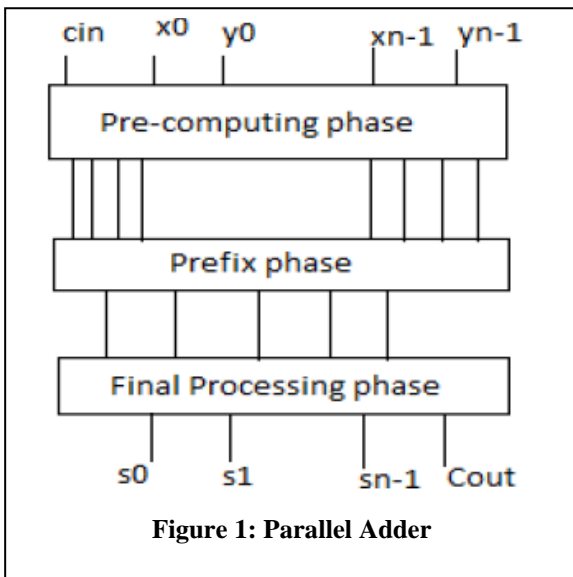
**III. PROPOSED LOW POWER HIGH SPEED ARITHMETIC CIRCUITS**

**A. Parallel Adders**

Parallel adder [6] is very important in the leading technology for the implementation of the VLSI chips. In parallel structure calculation is computed synchronously in parallel way. It is one among the fastest and wider adder. It is mainly focused on better improvement of delay enhancement of the adder. Parallel adder is classified into three phases:

- Pre-computing phase
- Prefix phase
- Final processing phase

The description of parallel adder is given in figure 1.



**Figure 1: Parallel Adder**

In Pre-computing phase propagate and generate signal is generated

$$P_i = A_i \oplus B_i$$

$$G_i = A_i \text{ and } B_i$$

In Prefix phase generate or propagate bit is generated.

Black bit generates ordered bit and grey cell generates left bit.

$$\text{Black cell: } G_i = G_i \text{ xor } (P_i \text{ and } G_j)$$

$$P_{ij} = P_i \text{ and } P_j$$

$$\text{Grey Cell : } G_{ij} = G_i \text{ xor } (P_i \text{ and } G_j)$$

In final stage sum and carryout is obtained

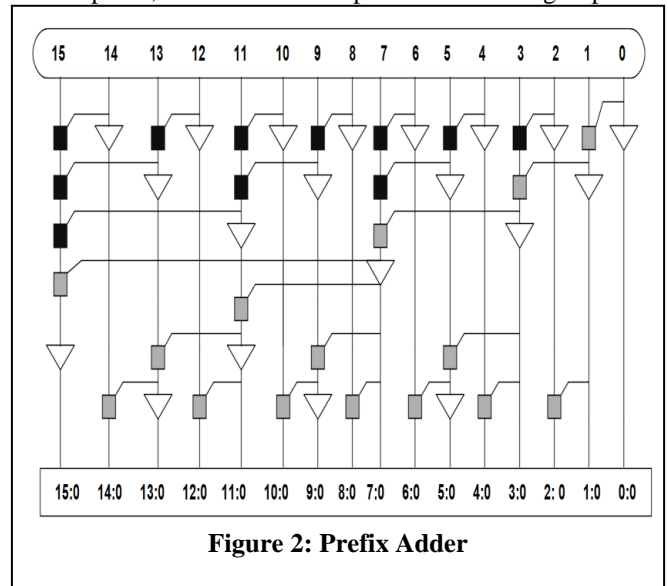
$$C_i = G_i$$

$$S_i = P_i \text{ xor } C_{i-1}$$

**B. Brent-Kung Adder/Subtractor.**

The Brent–Kung adder is a parallel prefix adder (PPA) form of carry look-ahead adder (CLA). Compared to the

Kogge stone adder (KSA), it introduces higher regularity in the adder structure and has less wiring congestion resulting in better performance and less chip area to implement stone adder (KSA). It's better than ripple carry adder as well. The Ripple-carry adders were the starting multi-bit adders that were set up in the early days and got their name from the ripple effect that the carry made while propagating from right to left. The time taken for addition was directly proportional to the length of the added bit. This is opposite in Brent–Kung adders where the carry is calculated in parallel and thus reducing the addition time drastically. Furthermore, to suit low power VLSI design Brent Kung Adders and other Parallel adders are designed to reduce chip area, power consumption and increase speed. Brent-Kung adder has increased performance due to the nature of tree structure of propagating carry which also leads to low power consumption as carry bit has to travel through fewer stages and hence there is minimum switching of transistor. The Brent-Kung adder computes the prefixes for 2-bit groups and using these prefixes 4-bit groups are computed, which in turn the prefixes for 8-bit groups are



**Figure 2: Prefix Adder**

calculated and so on. The carry out of each stage is calculated using these prefixes. These carries with group propagate of next stage will be added to compute the sum bit of that stage. Figure 2 shows the carry generation and carry propagation in parallel prefix adder

$$g_i = a_i + b_i$$

$$p_i = a_i \oplus b_i$$

The carry and sum in terms of  $p_i$  and  $g_i$  is expressed as

$$c_i = p_i + g_i \cdot c_{i-1}$$

$$s_i = p_i \oplus c_{i-1}$$

**C. Kogge Stone adder**

KSA is one type of carry tree adder which is similar to the CLAA. It is one of the fastest adder because it has less logic depth. It is widely used in design of VLSI chips. Kogge stone adder is the best adder because of its structural layout. It has efficient logic depth when compared to other structures of adder. It is one of the widely used adders because of its efficient performance in industry.



It depends on generate and propagate signal. Hence the performance of the adder depends on logic depth and delay. Various components are used in this adder such as black cell, grey cell, generate and propagate block, buffer. Black cell is used for computing propagate and generate signal. Grey cell is used for computing generate signal. Buffer is used for loading the effect. Delay is obtained by  $\log 2^N$  where N is derived as input. Area is obtained by  $(n \log 2^n - n + 1)$  - where 'n' is the input. Kogge Stone adder has 34 black cell and

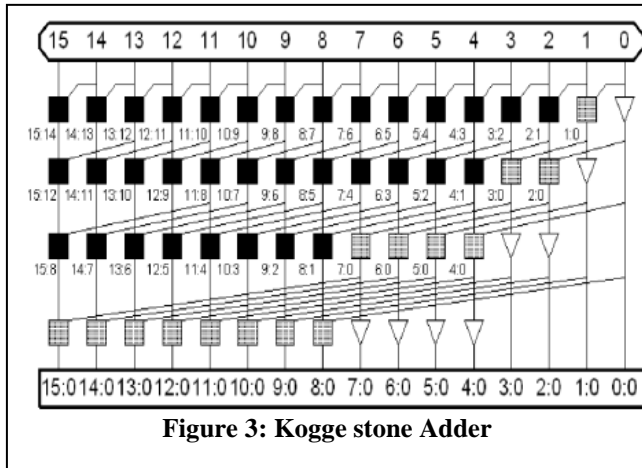


Figure 3: Kogge stone Adder

15 grey cell The 16-bit KSA block diagram of is shown in figure 3

**D. Ladner Fischer adder**

LFA is one more type of carry tree adder. Ladner Fischer adder minimum delay and has maximum fan-out similar to BKA. To generate carry signal  $O(\log n)$  time is required. it is also one among the fastest adder. The performance of this adder depends on minimum delay and high fan-out. Ladner

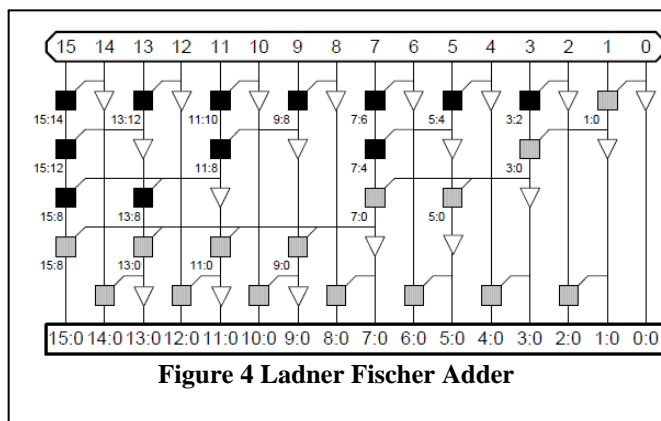


Figure 4: Ladner Fischer Adder

Fischer adder has large area when compared to Brent Kung adder. The 16-bit LFA block diagram of is shown in Figure 4.

**E. Vedic Multiplier**

Among those 16 Sutra one of the sutra which is used for perform Vedic Multiplication operation [7]-[10] is Urdhwa Tiryakbhyam. Urdhwa Tiryakbhyam means column and cross way. The main advantage of this multiplier is all the operation is done simultaneously and also to minimize the delay. It is used in many areas like medical, x-ray field, video compression, and also in fields of electronics. Figure 5 shows

how multiplication is done. This method can also be extended for any no. of digit. The multiplier with urdhva tiryakbhyam technique has added advantage that is, the gate delay and area increases very slowly compared to other conventional multipliers as the number of bits increases. The figure 5

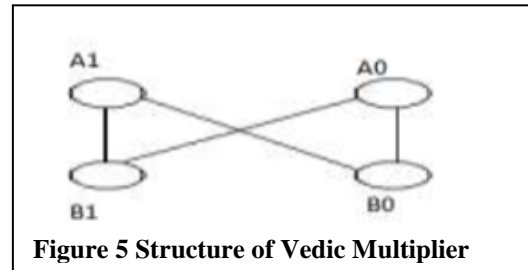


Figure 5: Structure of Vedic Multiplier

shows the flow of 4-bit numbers get multiplied using urdhva

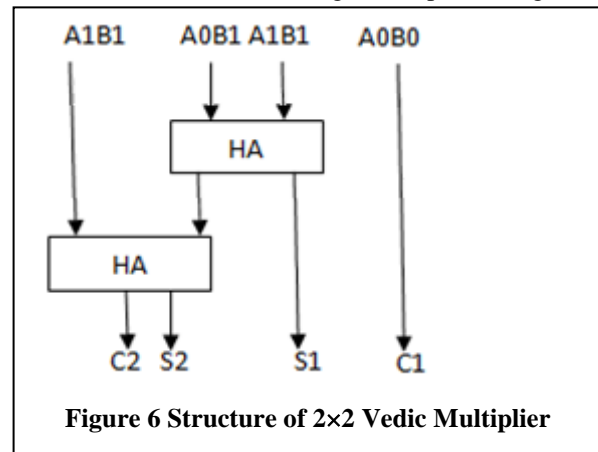


Figure 6: Structure of 2x2 Vedic Multiplier

tiryakbhyam technique.

**F. Urdhwa triyambaka multiplier**

The 2x2 method is done by 2 bit number  $A=A1A0, B=B1B0$ . The design is done by AND gate and half adder. The structure of is similar to Array multiplier. The Structure of 2x2 Vedic Multiplier is shown in figure 6.

**G. 4x4 Urdhwa triyambaka multiplier**

4x4 multiplier consist of 4 bit number  $A=a3a2a1a0, B=b3b2b1b0$ . 4x4 Method designed by 4 2x2 Vedic multiplier and 3 adders are used. 2x2 multiplier is done using 2 half adder and 4 gates. By using 4 bit input 8 bit product is obtained. The structure of 8x8 urdhwa triyambaka method is given in Figure 7.

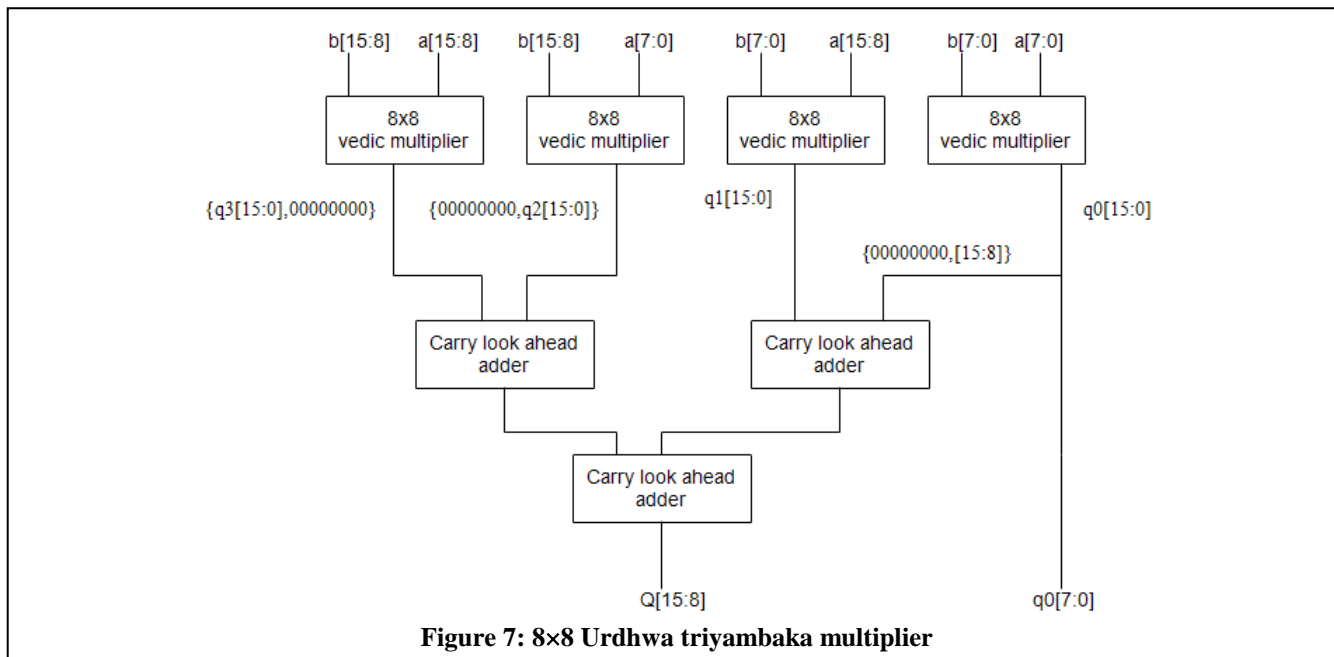


Figure 7: 8x8 Urdhwa triyambaka multiplier

**H. Analysis of division method**

In this sutra first only compliment of the divisor is taken leaving the MSB bit. The number of which the compliment is taken is multiplied with the sum of each number of the dividend and is carried out by addition in order to obtain the quotient and remainder Consider an example where dividend is 13650 and divisor is 123. So using this methodology iteration is reduced to 8. Figure 8 shows an example for division of two numbers.

Divisor	Dividend
1 1 3	1 3 5 9 0
-1 -3	-1 -3
	-2 -6
	0 0
-	1 2 0   3 0
	Q=120   R=30

Figure 8: Vedic division of two numbers

**I. Division by binary number**

Division by binary number [11], [12] is also done in the same way as the division of decimal number is done. To carry out the division 3 complimented bit are required they are -1, 0 and 1 respectively. An example of binary number is illustrated in Figure 8: Dividend=13590, Divisor=113

**Crumb method**

Crumb encoding requires two bits to describe single bit. They are signed bit and value bit. If signed bit is 0 then it is assumed as positive or negative. In Table 1 signed and valued bit is shown: Finally, the Modified method of Pragyatra Yojayet of eight-bit Dividend and four bit divisor is done by using

Crumb method in Figure 9. In this example LSB of the divisor crumb is complemented and then it is partially multiplied with dividend. Quotient is obtained by most significant bit (MSB) and the Remainder is obtained from remaining 3 bit from last result. Modified Vedic division is shown in Figure 9.

Modified 8 bit method is categorized into three steps:

- The crumb is encoded by dividend and divisor bits. Crumb is divided into unsigned and signed bit.
- Multiplication and addition is used to perform 8 bit operation.
- By using Crumb method quotient is obtained.

The modified algorithm of Vedic division is elaborated into

Dividend	Sign bit	Value bit	Crumb Representation
0	0	0	00
1	0	1	01
1	1	1	11

three stages:

- In order to perform partial multiplication, the crumb encoded digit of divisor is complimented.
- The algorithm which is used for division is designed using addition and multiplication.
- At the end quotient is decoded into bits.

Depending on these stages in the 1st step: bitwise xor method is done for crumb encoded digit of divisor except the MSC (most significant crumb).Using XOR logic 01 is converted into 11,00 will be same and MSC bit will remain the same it is not complimented. In second stage 2x2 partial multiplier and 2 bit adder is used.

**Table 2: Simulation results for Arithmetic circuits**

	Spartan 6				CADENCE 45nm Technology		
	Name	Logic	Signals	IOs	Area	Total Power(nW)	Delay nS
Kogge Stone Adder(16bit)	Used	69	90	49	394	16786.314	9.566
	Total Available	1920	...	66			
	Utilization %	3.6	0	75.8			
Brent Kung Adder(16bit)	Used	40	63	50	360	16116.889	16.440
	Total Available	1920	...	66			
	Utilization %	2.1	...	75.8			
Brent Kung Subtractor (16bit)	Used	49	63	50	547	21147.336	18.253
	Total Available	1920	...	66			
	Utilization %	2.1	...	75.8			
Ladner Fischer adder(16bit)	Used	38	61	50	370	16655.233	16.447
	Total Available	1920	...	66			
	Utilization %	2.0	...	75.8			
16 bit Vedic Multiplier	Used	270	514	58	7762	377496.974	29.0094
	Total Available	7168	....	141			
	Utilization %	3.8	....	41.1			
Modified booth multiplier (16bit)	Used	43	68	2.2	7168	344456.567	31.115
	Total Available	1920	...	...			
	Utilization %	2.2	....	53.0			
16 bit-Vedic Division(crumb encoding)	Used	270	7168	3.8	21568	1092888.474	348.397
	Total Available	514	....	....			
	Utilization %	58	141	41.1			

**IV. SIMULATION AND RESULTS**

The module design and description of the arithmetic circuits is implemented in using Verilog HDL. Each of the arithmetic operations listed above have been individually simulated using Xilinx ISE (Integrated Software Environment) 14.1 and CADENCE 45 nm Technology simulations are performed in Xilinx 14.1 and synthesized using Xilinx Plan Ahead Virtex6 and also power Area and Delay report are obtained in Cadence 45nm Technology.

**A. Simulation Results**

The proposed arithmetic circuits are implemented. Various performance measurements for the proposed multiplier and the existing multiplier are parametrically obtained and listed

in Table 2 Figure 11 shows Power comparison Figure 10 shows Delay comparison and Figure 10 shows Area Comparison.

Divisor	Dividend	
01 00 01 01	01 00 00 01 00 00 01 01	
	01 11 11	
	00 00 00	
	00 01 01	
	00 00 00	
	00 11 11	
	01 00 11 00 01	01 00 00
	Q= 10001-00100	
	Q= 01101	R=100

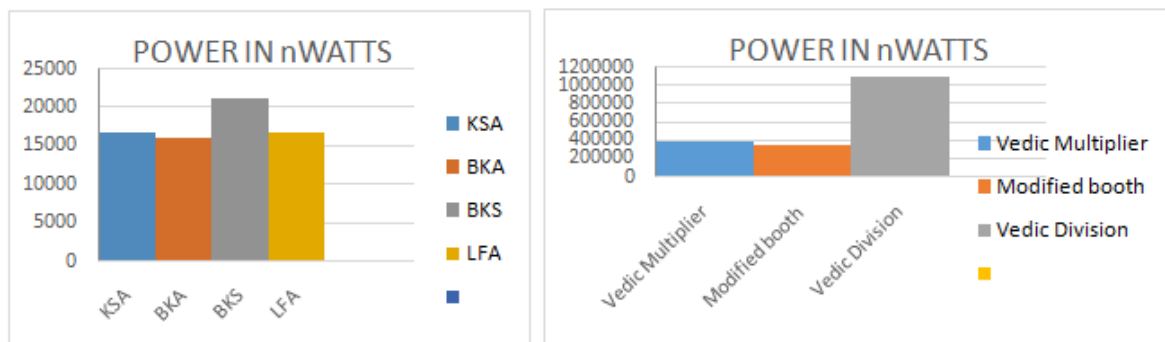


Figure 9: Power in nWatts

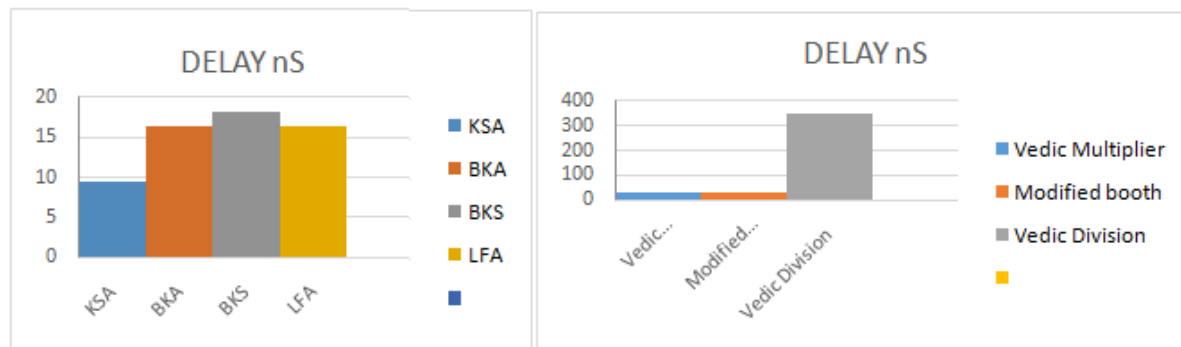


Figure 10: Delay Comparison in nSec

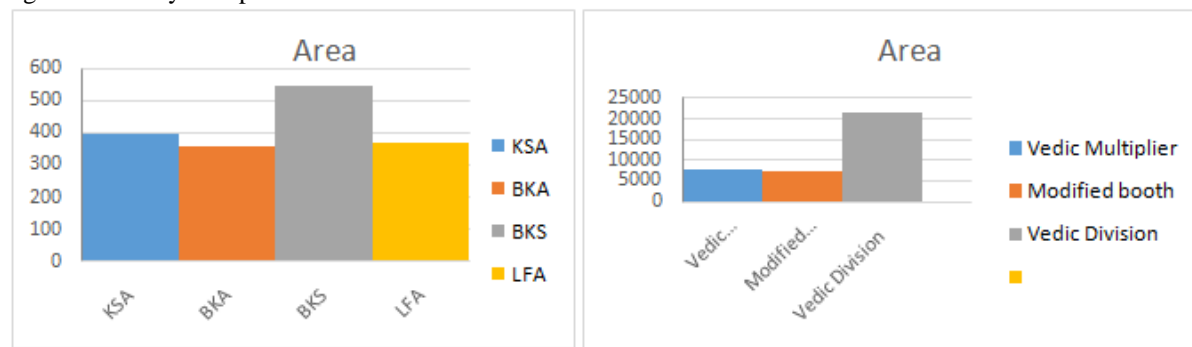


Figure 10: Area comparison

V. CONCLUSION

Depending on LUT Ladner Fischer has less area, and Ladner Fischer has less No of Slices, when comparing the delay Kogge Stone has less delay. In Vedic division when compared to the previous paper it has less delay compared to other normal division method. Since Kogge Stone adder is used in Modified Booth multiplier, it has a less delay in radix-4 when compared to radix-8. Vedic Multiplier has less area and delay when other multiplier is used.

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