

# Low Power Hardware Efficient Comparator using Full Swing 3T XNOR

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**ABSTRACT---** This paper describes a new full swing 3T XNOR for low power, hardware efficient comparator design. This 3 transistor(3T) XNOR can achieve full output swing at an operating voltage one with lesser power and dimension of energy(power delay product) compared to the conventional XNOR designs. Thereby proposed low power area efficient comparator circuits can play a vital role in encryption systems, error detecting circuits, complex ALUs, and DSPs, where power, speed, and area are the major constraints. By realizing this hardware efficient proposed comparator, achieve complex circuit optimization. The proposed hardware is deliberate using CADENCE 5.1.0 EDA tool and simulated in spectre virtuoso.

**Keywords—**comparator; full swing 3T XNOR; low power; optimization; cadence(tool).

## I. INTRODUCTION

In the present scenario, VLSI design demands hardware efficient and low power designs [1]. In this paper, a low power hardware efficient comparator is presented using 3T XNOR. One of the logic gate is XNOR it is based on the principle of equality of logic that is, if both the inputs are equal then the output is one. The XNOR gate contains several inputs although only one output. It is the essential module of some combinational circuits, comparators. Also used in encryption and arithmetic circuits as a combination of XNOR and XOR circuit for low power consumption.

The 3T XNOR gate, which consists of 3 transistors aim at providing the utmost output voltage. It has less area with less power and delay parameters. It attain low power by reducing parasitic effect due to decrease in area[2]. The conventional XNOR failed to work precisely at smaller voltage levels.

Therefore, the main target of this proposed work is to be set to a low power area efficient comparator circuit using proposed 3T XNOR gate with the least area by maintain a symmetry between power and speed at lesser voltage levels and highest output voltage levels.

A digital comparator is a hardware that will accept two numbers as input and determines whether one number is bigger than, less than or equivalent to the other number. Comparators are integral part of CPU, error detection circuits and microcontrollers. Fig.1[3] shows the 1-bit cascaded comparator.

In this paper, the NOR gate is replaced by 3T XNOR thereby, we can reduce the power and hardware

utilization. Section II introduces the architecture of conventional 3T-XNOR. Section III presents proposed 3T-XNOR architecture and in section IV proposed a comparator using full swing 3T-XNOR. Section V presents simulation design using the CADANCE tool and finally, in section VI results are compared followed by a conclusion in section VII.

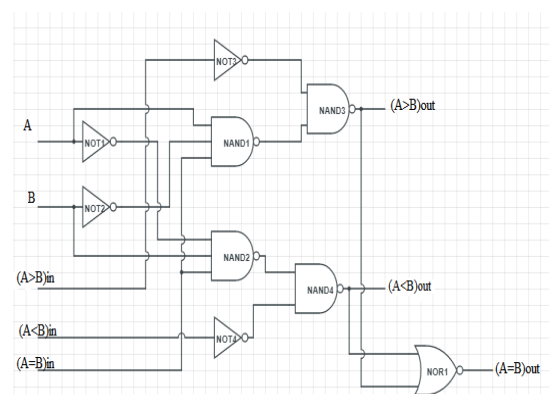


Fig. 1.1-Bit Cascaded Comparator(Gate Level)<sup>[3]</sup>

## II. CONVENTIONAL 3T- XNOR

### A. Architecture

XNOR gate working on the rule of logical equality, that is, if both the inputs are equal then the output is one.

In fig.2 , shows the 3T XNOR which contains one PMOS and two NMOS transistors. The conventional XNOR gates fail to work precisely at smaller voltage levels. It cannot attain the full output wing. The power dissipation is also high.

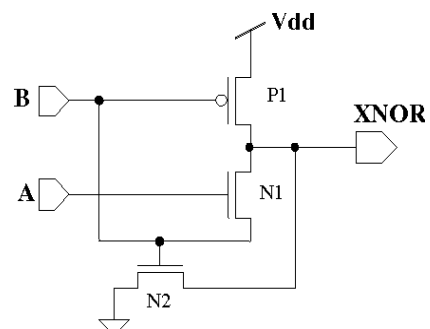


Fig. 2.3T XNOR<sup>[1]</sup>

## III. PROPOSED FULL SWING 3T XNOR

### A. Architecture

Here an XNOR gate with full output voltage swings, without any degradation at the



output. The proposed design includes three transistors, two are NMOS and other is PMOS. The PMOS gate is on voltage of 500mV. The threshold voltage is given to its gate terminal makes the transistor PM<sub>0</sub> is always ON. In order to suppress the body bias effect to the least, the substrate contact of the PMOS is connected to the supply voltage and the substrate contact of the NMOSs are connected to the ground terminal. The PM<sub>0</sub> transfers a strong '1'. Whereas the NMOS transfer a strong '0'. Fig.3 show the proposed 3T XNOR.

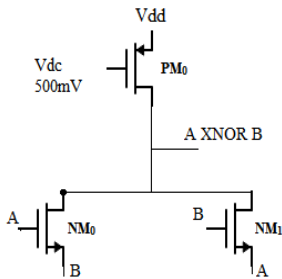


Fig. 3. Full swing 3T XNOR<sup>[2]</sup>

The functional behavior of the 3T XNOR gate is described below:

Case (1): When A=0 and B=0.

The NMOS are turned OFF. Since the PMOS has a voltage of 500mV, the supply voltage appear across the PMOS. This results in HIGH output across output terminal.

Case (2) and (3): When (A=0, B=1) or (A=1, B=0).

The NMOS which is turned ON will pass a strong '0' to the output. This results LOW for both the cases.

Case (4): When A=1 and B=1.

Strong '1' is obtained at the output. Both the NMOS are turned ON, the output across the output terminal is generated by both the NMOS and PMOS. The NMOS generates a weak '1' and the PMOS generates a strong '1'.

By comparing with the existing design, it attains full output swing in all combinations at an operating voltage 1V. Power dissipation is less as compared with existing designs.

IV. PROPOSEDCOMPARATOR

1-Bit cascaded comparator can be cascade any number of times to obtained higher order bits comparison. The input-output equation of the 1-bit cascaded comparator is given below[3]:

$$(A > B)_{op} = (A > B)_{inp} + (A = B)_{inp} \cdot (AB)'$$

$$(A < B)_{op} = (A < B)_{inp} + (A = B)_{inp} \cdot (A'B)$$

$$(A = B)_{op} = [(A > B)_{op} + (A < B)_{op}]'$$

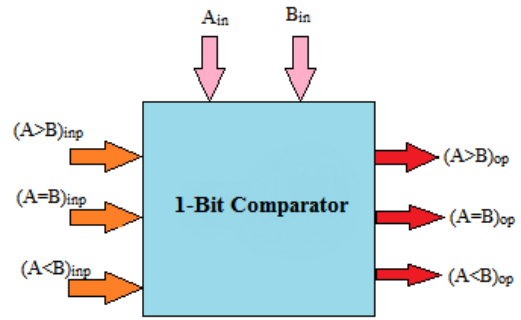


Fig.4. 1-bit comparator<sup>[3]</sup>

From the fig.4 (A > B)<sub>op</sub> , (A < B)<sub>op</sub> and (A = B)<sub>op</sub> are outputs and (A > B)<sub>inp</sub>, (A < B)<sub>inp</sub> , (A = B)<sub>inp</sub>, A and B are the inputs to the comparator. Fig.5 shows the 1-bit cascaded comparator(gate level), which are developed using the equation below.

$$(A = B)_{op} = [AB' + A'B]'$$

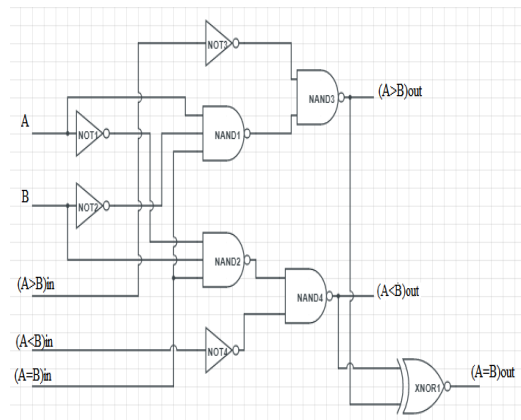


Fig.5.1-Bit Cascaded Comparator(Gate Level) SIMULATION RESULTS

The proposed circuit is designed using the CADENCE 5.1.0 tool and simulated using virtuoso. The circuits are simulated at 100ns and achieve full output swing at an operating voltage of 1V. Fig. 6 shown the circuit diagram of proposed full swing 3T XNOR.

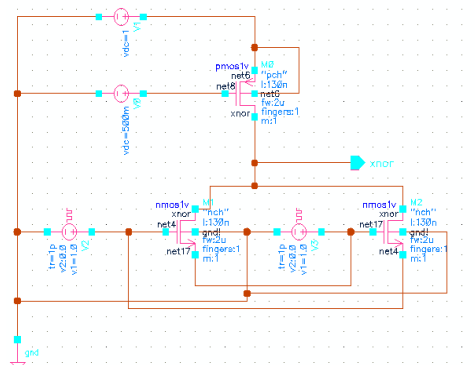


Fig. 6. Circuit diagram ofproposed full swing 3T XNOR



Fig. 7 shows the transient response of full swing 3T XNOR. It shows inputs A, B, and its corresponding XNOR output.

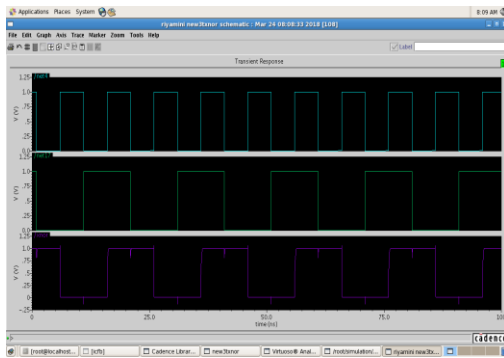


Fig. 7. Transient Response of full swing 3T XNOR

Fig.8 and Fig.9 shows the delay and power calculation using cadence tool. From this, it clears that the proposed XNOR has 5008.2ps delay and average power 0.49924μW.

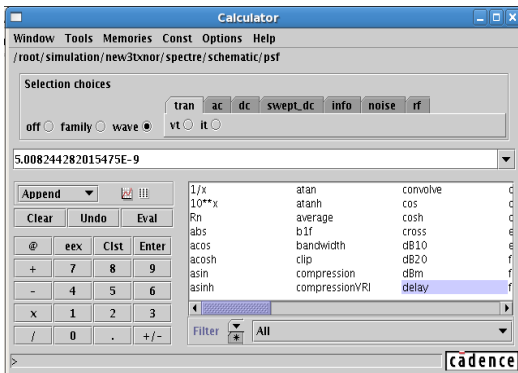


Fig. 8. Delay calculation using cadence tool

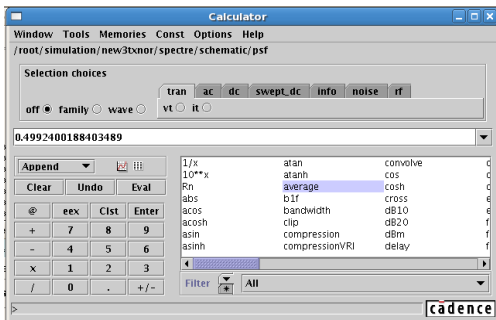


Fig.9. Power calculation using cadence tool

Fig.10 shown a comparator using full swing 3T XNOR.

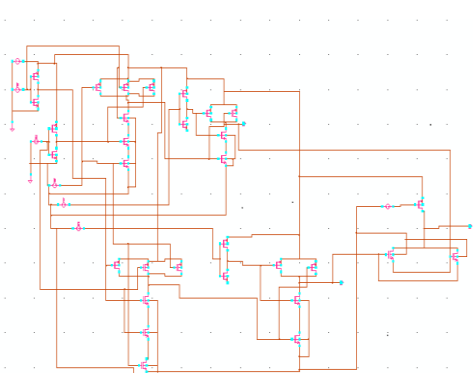


Fig. 10. Circuit diagram of the comparator

Fig.11 shows the transient response of the comparator. It shows inputs A, B and its corresponding outputs AgtB, AltB, AeqB.

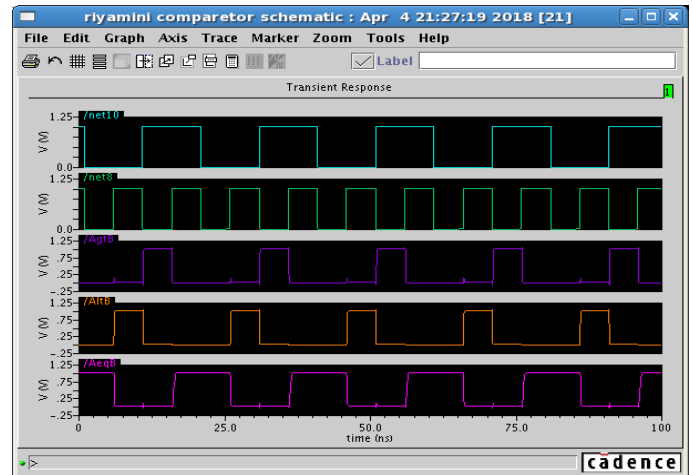


Fig. 11. Transient Response of comparator

## V. PERFORMANCE SUMMARY

TABLE I.COMPARISON BETWEEN PROPOSED FULL SWING 3T XNOR AND CONVENTIONAL XNOR

	3T XNOR(existing)	FULL SWING 3T XNOR
Supply voltage	1V	1V
Power dissipation(μW)	98.124	0.49924
Delay(pSec)	27.617	5008.2
PDP(fJ)	2.709	2.50029

TABLE II. COMPARISON BETWEEN PROPOSED COMPARATOR AND CONVENTIONAL COMPARATOR

	CONVENTIONAL COMPARATOR	PROPOSED COMPARATOR
Supply voltage	1V	1V
Transistor count	32	31
Power dissipation(nW)	91.50	18.92
Delay(nSec)	5.098	5.108
PDP	46.64fJ	96.64aJ

By comparing both 3T XNOR, modified 3T XNOR has less power dissipation and dimension of energy. By using the modified 3T XNOR, the comparator circuit is proposed.

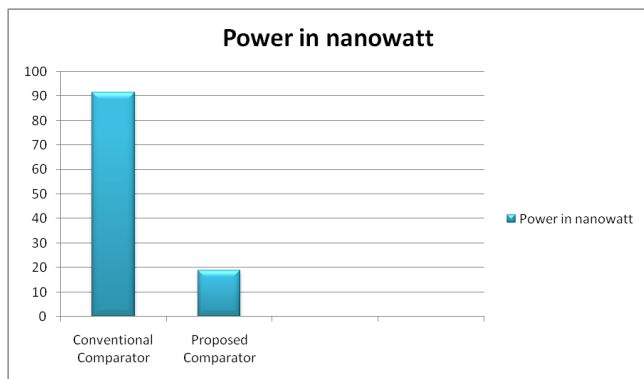


Fig. 12. Graphical representation of power

The modified comparator has less power dissipation and also the transistor count reduced to 31, so we get a low power area efficient comparator using full swing 3T XNOR.

ACKNOWLEDGMENT

We thank to show our gratitude to Dr. J M Mathana, Principal and Dr. T D Subash, head of the Electronics and Communication department for sharing their pearls of wisdom with us. Also, thank all staff members of the department for their support during the work.

VI. CONCLUSIONS

The presented design has a 3T XNOR gate, it achieves complete output swing so the proposed comparator design also attains full output swing without any degradation. Thereby we can eliminate the level of restoring the circuit. The power dissipation is less compared to conventional designs. We reduce the hardware utilization by reducing the transistor count to 31.

We can achieve high speed in the future by minimizing the equation of the comparator. Thereby we can reduce the count of the transistor.

In this paper, a low power hardware efficient comparator is presented using 3T XNOR. Simulation is done by CADENCE tool, 3T XNOR achieves full output swing at an operating voltage of 1V with improved power and energy compared to the existing designs. The results reveal that the designed circuit has less power dissipation and area. Comparator circuits can be used in ALU, DSP thereby we achieve low power area efficient systems.

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