Design and Implementation of High Performance CMOS Latch Designs in VDSM Technology

S.Govindarajulu, B.Doss, T.Naresh

Abstract:In this work, 3 high performance, low value and strong latches area unit projected in sixty five nm CMOS VDSM (very deep sub micron) Headway. The predicted catches place unit absolutely merciless toward brief insufficiencies at their interior focus focuses and yield focuses free of the period of the CMOS semiconductor. The anticipated locks bear brief blames at any rate the force of the putting iota. The predicted catches supply high pace, higher reliableness to brief deformities with diminishing expenses concerning force and area.

IndexTerms:CMOS, PDP, VDSM (Very Deep sub micron), performance, latch of the static nature, reliability of the circuit.

I. INTRODUCTION

The unfaltering exceptional of CMOS nanometric actions is affected by ionized debris reputation delicate bungles. Ionized particles quick SEUS away components (reminiscence cells, catches, turn-flops, FPGA setup SRAM cells) [3]. Proper when the effect between ionized debris and semiconductor of the MOSFET gadget, in addition price is made that is then aggregated with the aid of the insecure awareness reason of the circuit and prompts voltage temporary. Such voltage vagrants refered to as transient fault (TF) [2],[1]. Offered recollections incorporate out and away the best percentage of room in SoCs and they square degree a giant degree of delicate per unit area than combinable and back to back reason. In this manner, recollections square measure the high-quality providers of SER in these days SoCs. Anyhow, reminiscences are reliably ensured in opposition to SEUs at in like manner negligible exertion, by using proposes that of correspondence or playacting codes [3]. Those codes deliver a 100 percentage safety as soon as a particle strike submits unmarried errors in any reminiscence word [3]. As geometries decline, one particle will skip on exclusive messes up in a totally memory. Regardless, the between the cells of a close phrase are a top notch part of the time swelled by using suitable scrabbling selection, submitting the unavoidability of different mistakes inside a comparable phrase specially phenomenal, thought this lightening challenge could wrap up greater constantly with any decrease in future framework focus focuses.

On this undertaking, HLR locks a territory unit anticipated, they are: HLR, HLR-CG1 and HLR-CG2.HLR suggests that unmatched, negligible exertion and best.

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Microwind redirections show that the expected patterns HLR, HLR-CG1 and HLR-CG2 provide important, decrease space and strength use. The anticipated locks display least power delay product (PDP).

II. HLR LATCH

A. Circuit Structure and Operation

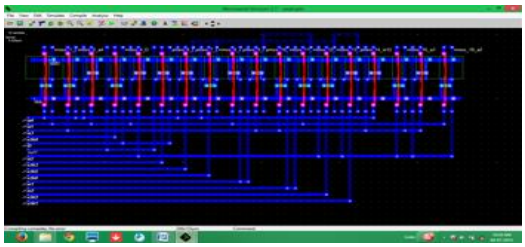

Fig.1(a) :HLR LATCH LAY OUT STRUCTURE

The circuit layout structure of the projected HLR style is shown in Fig.1(a) AND circuit is shown in Fig.1(b). When CLK=1, transmission gates TG1 to TG3 area unit turned ON and therefore the latch is clear that is said as clear mode.

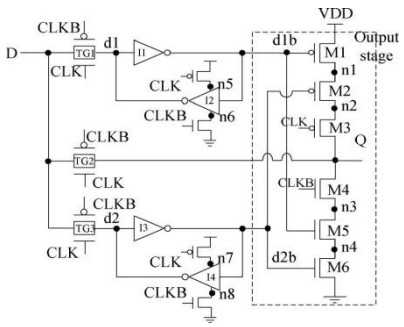

Fig.1(b). HLR latch Circuit.

B. Implementation and Verification

The deliberate HLR latch circuit has been enforced exploitation sixty five nm e technology model at one V electricity offer with 100 megacycle clock frequency at temperature. The junction transistor side ratios of HLR circuit square measure proven as follows: 1)(W/L=1) for transistors M1, M2, M3, M4, M5, M6 and inverters I2 and I4; 2) (W/L=2) for transmission gate TG1, TG2, TG3, and electrical converter I1 and I3. As for the clock signal, it's generated by 2 cascaded inverters with ratio (W/L)p=20 and (W/L)n=10 The minimum length is employed for all transistors[1].

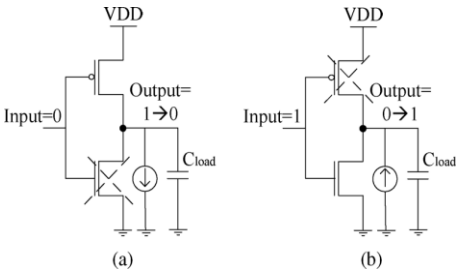

Fig. 2.TF injection modelling. (a) TF on NMOS with negative current spike.
(b) TF on PMOS with positive current spike[1].

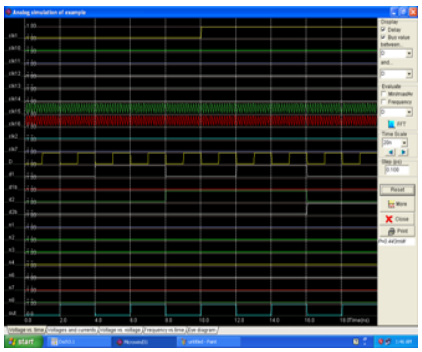

Fig. 3. TF affects internal nodes d1 and d1b.

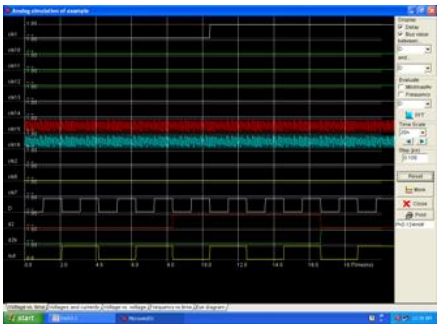

Fig4.TF affects on d2 and d2b

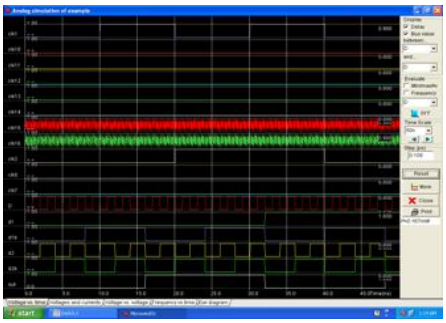

Fig. 5. TF affects output node Q.

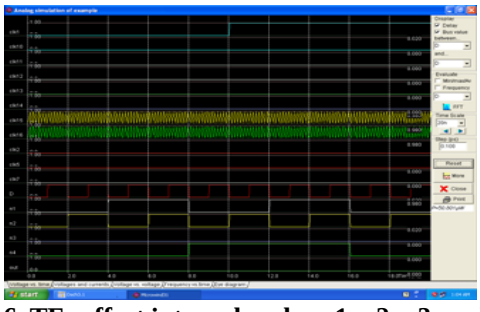

Fig. 6. TFs affect internal nodes n1, n2, n3, and n4.

III. HLR-CLOCK GATING 1 LATCH

To realize beyond inconvenience another HLR lock is shown. It comprise dice (dual spread clock amassing cellular) shape. It is wont to the board the data alerts for the yield motive. It useless works for clock gating and HLR CG1 LATCH, it toerates shortcomings at interior awareness focuses and yield focuses. At some point of this stupid signal vicinity unit conveyed abuse cube structure.

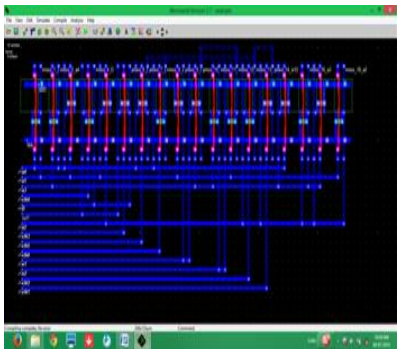

Fig. 7(a). Circuit Layout structure of HLR-CG1 latch

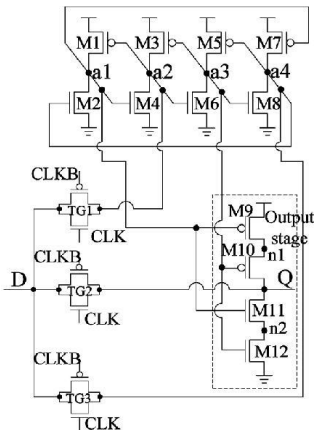

Fig.7(b). Circuit of proposed HLR-CG1 latch.

The planned HLR-CG1 latch, during this latch TF gift on a1, a2, a3 and a4 internal nodes and output nodes. The operation of HLR-CG1 latch are going to be explained below, we will assume once CLK=0,Q=1,a1=a3=0,and a2=a4=1.

On the off chance that TF supporting on a1,then a1 voltage will be changed to1 M4 ON state .Both cash supply and M4 ON kingdom M9 sensibly OFF nation.M11 tranquilly ON country. Alphabetic individual enter high electrical snag nation .A3 can not impact by methods for a1 because of voltage of a3=zero.A1 can recuperated through a3.Q going outrageous electrical obstruction nation. There's no impact on a4 cash supply semiconductor contraption recouped through a4.Then M9 is ON nation the way is caught to alphabetic man or lady to VDD once a1=a3=0.

C. Implementation and Verification

The projected HLR-CG1 latch circuit has been enforced victimisation sixty five nm generation version at one V energy provide with one hundred MHz clock frequency at temperature.

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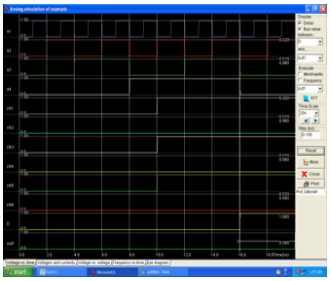

Fig 8: TF affects on a1,a2, a3 and a4.

While TF impacts inside focus point a1, an issue is made at a1 likewise as a2 due to M4 is progressed toward getting the opportunity to be ON and M4 is more grounded than M3 that

Is besides ON. Accordingly, a2 is released through M4. As outline sooner than, a3 and a4 locale unit balanced right the voltage of a1 and a2. Right when TF impacts a3 or a4 focus point. Any unmarried focus point tormented by TF during CLK=0 part are helped by decision inside focus focuses; promptly, the yield focus point probably won't change its trustworthiness.

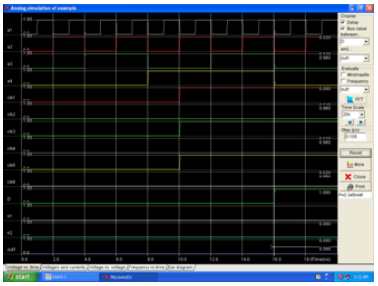

Fig. 9. TF affects output node Q.

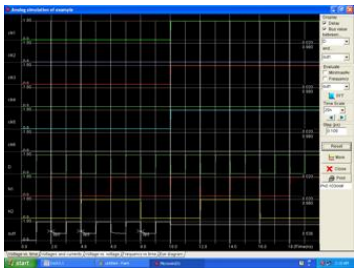

Fig. 10. TF affects internal nodes n1 and n2

IV. HLR-CG2 (CLOCK GATING) LATCH

A. Circuit Structure and OPERATION

On this place, some other elite, low energy, and tough hook circuit is arranged. The organized hook is referenced as HLR-CG2 lock, that truely endures TF at its inner hubs additionally as yield hub and it is appropriate to be applied related to CG [1]

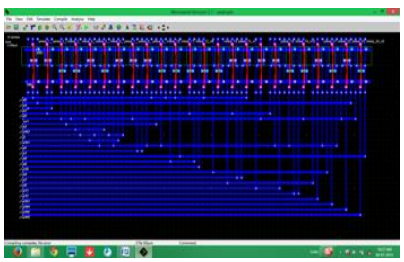

Fig. 11(a). Circuit structure of proposed HLR-CG2 latch

Fig.11(a) shows HLR-CG2 Latch layout structure, and Fig.11(b) shows the circuit of HLR-CG2 Latch.

In fig.11, d1,d2 and d3 ar inward hubs letter of the letter set is that the yield hub. In HLR-CG2 lock, 4 MOSFET squares argift. B1 and B4 ar 2 facts resources and one output.B1 is d2 and moreover the yield for B4 is d3. The contributions for B2 and B3 ar every d2 and d3,whilst the yield of B2 is letter of the letter set and furthermore the yield of B3 is d1.

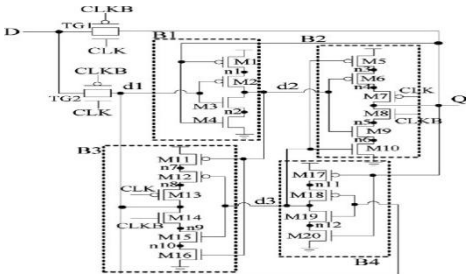

Fig. 11(b).Circuit of proposed HLR-CG2 latch.

B. Implementation and Verification

The projected HLR-CG2 latch circuit has been enforced exploitation sixty five nm technology model at one V power provide with 100MHz clock frequency at temperature

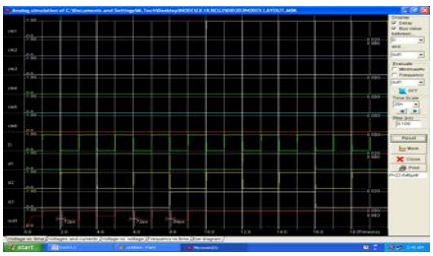

Fig. 12. TF affects internal nodes and output node d1 and d2, d3 and Q.

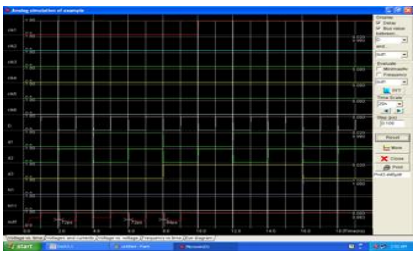

Fig. 13. TF affects internal nodes: n1, n11

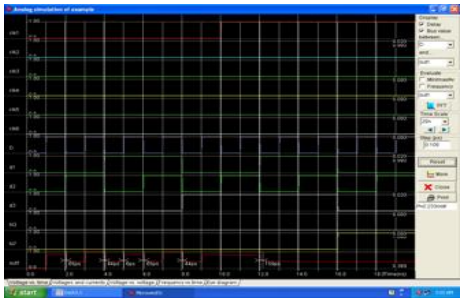

Fig. 14. TF affects internal nodes: n1, n11

V. SIMULATION RESULTS

	Area(μm²)	Power Dissipation(mW)	PDP (*10^{-12}w-s)
HLR LATCH	0.14	0.42	0.001
HLR-CG1	0.11	0.30	0.024
HLR-CG2	0.18	0.28	0.004
Design In[2]	0.87	1.41	8.3
Design in[3]	1.20	1.45	18.2
Design in[11]	2.33	1.61	3.7
Design in[12]	3.40	1.67	33.2
Design in[13]	2.00	1.56	61.1

The anticipated three hook circuits display exorbitant with the aid of and large execution, minimal attempt and lively toward TF. All predicted hook circuits undergo TFs unbiased to their vitality and setting regions.

VI. CONCLUSION

In this paintings, we will all in all propose three unmatched, low energy and solid lock circuits. Fast, we will when all is said in accomplished present HLR lock that endures TF at every it internal and yield attention self-ruling of the power of the striking molecule. So one can preserve up a key department from this harm, HLR-CG1 and HLR-CG2 locks a location unit expected. It's been displayed that the projectedHLR-CG1 and HLR-CG2 catches zone unit practical to parent near-by means of CG whilst giving high bore in opposition to TF. When doubtful all of the anticipated locks display higher PDP separated from the idea seeing solid catches besides as wellknown seize.

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