Data Integrity Maintenance using and Logic Feed based Low Power SRAM Cell

A. Dinesh Babu, J. Akash, Vishnu Varadhan Janardhanan

Abstract--- Continuous Nano-Scaling of transistors, coupled with increasing demand for ultra-low power applications where expanded system operation time under limited energy resource constraints increments the susceptibility of VLSI circuits designs to soft errors. The robustness and energy efficiency are vital design parameters for Body Sensor Nodes, intelligent wearable,Internet of Things and space mission projects. In contrast for graphics (GPU) processors, servers, high-end applications and general purpose processors, energy is consumed for higher performance. To meet the increasing demand for larger embedded memories like SRAM in highly integrated SoCs to support a wide dimensions of functions. As a result, further strengtheningthe design constraints on performance, energy, and power is needed. In general SRAMs dominates as being a basic foundational building block for such memory arrays. Any minor modifications in the fundamental unit will have significant impact in the overall design. This work presents a AND gate feed based SRAM cell, which significantly upgrades read and write static noise margin (SNM) and utilizes low power. Simulation was done using 180nm technology library file of Cadence virtuoso design software. The finalresults shows how the cell achieves the lowest leakage power dissipation among the other cells in the existing state of art designs. Investigations are also done in terms of process voltage, average power variations etc.

Index Terms--- Static Random Access Memory, Static Noise Margin, Silicon on Chip, Internet of Things.

I. INTRODUCTION

SRAM plays a vital role in System on Chip (SoC) design toenhancesthe logic performance. SRAMs are the basic foundational unit of storing data bits in SoC. Therefore, high performance and stable SRAM cell with reliable data integrity is the prime need. Added to that thedemand for radiation harden ,reliable, stable, ultra-low powerbattery-operated devices are growing continuously, mostly in applications such as satellites,tiny medical instruments,satellite launch vehicles and wireless body sensing networkswhere reliability, stability, and low power SRAMs are neededfor expanded system operation time under limited energyresources.SRAMmakes up a huge portion of a system-on-chip area, and most of the time, it also dominates the entire performance of a system. In addition to this, the tremendousgrowth in the popularity of pervasive devices and other emerging applications, such as wireless body sensing networks and implanted medical instruments, necessitates the requirement of low-power SRAMs. Therefore, a robust low-power SRAM circuit design has created a great research attention and has become important [1]–[3].

Moreover, a design of robust low-power SRAM takes many process and performance related tasks. Due to this, in deep sub - micrometer technology, near/sub-threshold operation is very challenging due to increased device variations and reduced design margins. Further, with each technology node, the share of leakage power in the total power dissipated by a circuit is increasing. Since, mostly, SRAM cells stay in the standby mode, thus, leakage power is very vital. The increasing leakage current along with process variations tends to large spread in read static noise margin (RSNM) and results in read failures at the tail of the distribution. Advanced microprocessors demand increasingly large memories, which cannot be fulfilled with(i) planar DRAMs, or with (ii) embedded DRAMs due to increased manufacturing cost which have not been proven to be feasible for high-yield, high-volume microprocessors. Furthermore the charge within the capacitor leaks, it is important to refresh each memory cell periodically. This refresh requirement paves way to the term dynamic whereas static memories do not have a need to be refreshed. Thus SRAM has become a major component in many VLSI Chips because of their large storage density and small access time.

SRAM has become the topic of substantial research due to the rapid development for low voltage memory, low power design during recent years due to increase need for notebooks, laptops, IC memory cards and hand held communication devices. SRAMs are widely used for mobile applications as both on chip and off-chip memories, since their ease of use and low standby leakage. Hence, conventional 6T cell SRAMs is the main option for today's cache applications. A high-density static embedded memory makes use of a 6-transistor single-bit line memory cell [1].Although SRAM has many more advantages as compared to DRAM, still designing a hardware efficient SRAM cell was always a challenge.As inverter sizing to ensure good hold time and easy read/write operation is also not an easy task to do.

Moreover in today's world area constraints have become a major concern especially in the fields of VLSI which involves integrating thousands of transistors, area does become a major concern. Thus consideration of minimum use of transistors while designing a SRAM is also an important parameter.However, one should always keep in mind certain parameters such as Delay and average power while designing a SRAM cell.

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As delay of SRAM cell determines its data retain capacity. Similarly there are certain other parameters which should be taken into account such as hold time, read and write time .Thus challenging the design process of SRAM. In this work the conventional 6T SRAM [3] though being hardware efficient its delay and average power is more when compared with the 11T SRAM cell. Despite these merits in 11T SRAM cell [4], it is still bulky in a hardware perspective as it contains a very complex circuit containing BL, RBL, WL, RWL, WLB and also a discharge path with two transistors.The remaining part of this paper is organized as follows.

Section II discusses the fundamentals of a SRAM cell and also the working of SRAM in the real world application.Section III explicates on the important parameters of conventional SRAM cells and also discusses on the Schmitt Trigger based Inverter design.Section IV describes in detail about the proposed SRAM design using modified ST and AND feed logic.Section V discusses about the simulated results and comparison of performance parameters of the proposed SRAM designs with conventional designs.Section VI concludes the overall work by highlighting the salient features of the proposed design and also gives the scope of future enhancement.

II. LITERATURE SURVEY AND RELATED WORKS

Static random-access memory (static RAM or SRAM) is a semiconductor memory that uses bi-stable latching circuitry (flip-flop) to store each bit. SRAM exhibits data remanence, though it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. The term static differentiates SRAM from DRAM (dynamic random-access memory) which must be regularly refreshed. SRAM is faster and more expensive than DRAM; it is mostly used for CPU cache while DRAM is used for a computer's main memory [5]. SRAM ‘s cell primarily exist as a as RAM or cache memory in micro-controllers (usually from around 32 bytes up to 128 kilobytes), also it exist as a as the primary caches in powerful microprocessors, such as the x86 family, and many others (from 8 KB, up to many megabytes) and stores the registers and parts of the state-machines used in some micro processors. Where as in computers SRAM’S are used as a peripheral equipment in order to save CPU register files, internal CPU caches and external burst mode SRAM caches, hard disk buffers, router buffers, etc. LCD screens and printers also normally employ static RAM to hold the image displayed (or to be printed).

Static RAM was used for the main memory of some early personal computers such as the ZX80, TRS-80 Model 100 and Commodore VIC-20.SRAMs, have standard SRAM functionality, but they save the data when the power supply is lost, ensuring preservation of critical information. Non-volatile SRAMs are used in a wide range of situations – networking, aerospace, and medical, among many others where the preservation of data is critical and where batteries are impractical. By Transistor types, Bipolar junction transistor (used in TTL and ECL) are very fast but consumes a lot of power.MOSFET (used in CMOS) – low power and very common today. By flip flop types, Binary SRAM uses one’s and zero’s and the ternary SRAM computing is commonly implemented in terms of balanced ternary, which uses the three digits −1, 0, and +1. The negative value of any balanced ternary digit can be obtained by replacing every + with a − and vice versa.

Conventional 6T SRAM Cell [1]

A typical SRAM cell is made up of six MOSFETs is shown in figure [1]. Each bit in an SRAM is stored on four transistors (M1, M2, M3, and M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations.

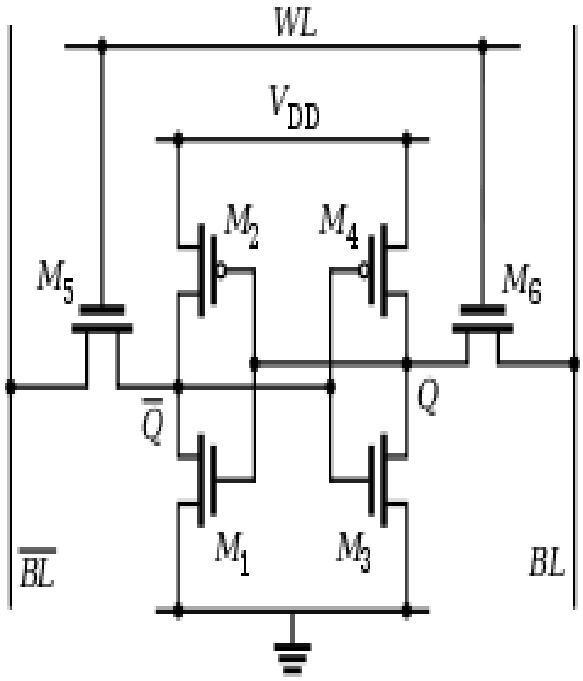

Fig. 1: Conventional 6T SRAM Cell

A 6T SRAM cell includes an inverter for inserting the data into the cell (write) which includes a pull-up transistor and a pull-down transistor, and another inverter which reads a data from the cell (read) which includes a pull-up transistor and a pull-down transistor, two access transistors for both read and write operation respectively. Both the process of data to be written into the cell and to be read from the cell can be done through via their corresponding access transistors in a one-sided read operation. Accordingly the equivalent resistance of the access transistors are higher than that of their corresponding read pull-up transistor and pull-down transistor.

In addition to such six-transistor (6T) SRAM, there are other kinds of SRAM cells which uses 4, 8, 10 or more transistors for per bit of storage[6].The most important advantage of the cross coupled inverter type SRAM cell circuit topology is that it shows very small static power dissipation, essentially, it is limited by small leakage current. It also shows high immunity to noise due to larger noise margins, and the ability to operate at lower power supply voltage.

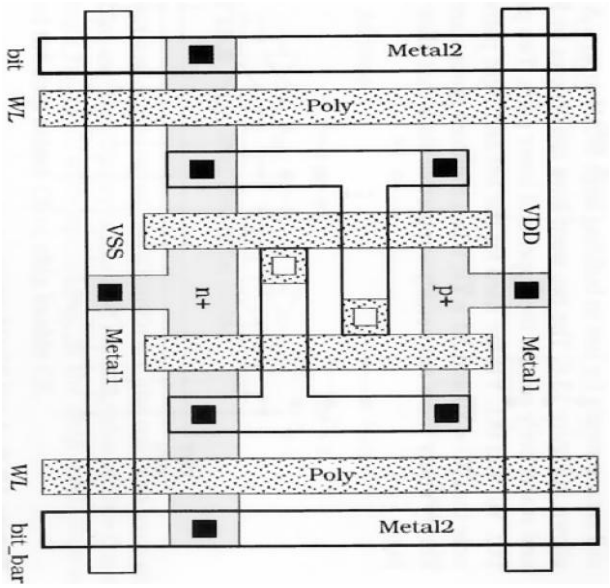

Fig. 2: Layout of SRAM Cell

8T SRAM CELL [5]

The data stability of a SRAM cell will be a primary concern for future technologies due to variability and decreasing power supply voltages. Hence optimization can be done in 6T-SRAM for stability by choosing the cell layout, device threshold voltages. The 8T-SRAM proposed [5], provides a much greater enhancement in stability by eliminating cell disturbs during a read access.

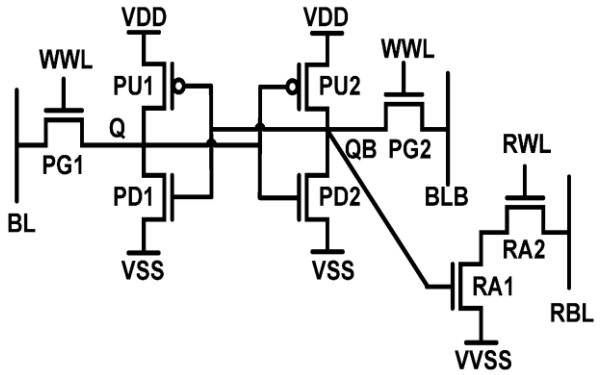

Fig. 3: 8T SRAM Cell

10T SRAM CELL [4]

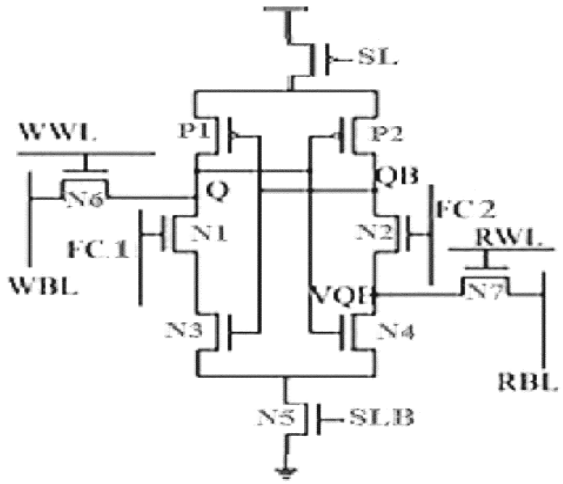

Fig. 4: 10T SRAM Cell

A 10 - Transistor static random access memorycellwith reduced power and with improved values of static noise margin (SNM) is proposed in [4]. The single bit-line incorporated with dynamic feedback control is employed in 10-T SRAM which enhances the SNM at ultra- low power consumption. Further, the power consumption is reduced drastically down by the use of sleep transistors.

11T SRAM CELL [1]

A Schmitt-trigger-based single-ended 11T SRAM cell, which significantly improves read and write static noise margin (SNM) and consumes low power is proposed in [1]. The design which achieves the lowest leakage power dissipation among the cells considered for comparison is proposed. The impact of various parameters such as temperature, process voltage, and hold SNM, read SNM, write margin, immunity to half-select issue, ION/IOFF ratio of read path is further analyzed.

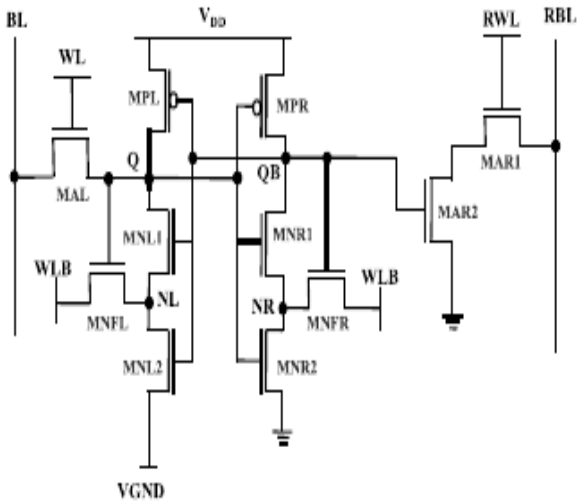

Fig. 5: 11T SRAM Cell

III. ST INVERTER AND SRAM DESIGN

Schmitt Triggered Inverter

In SRAM cell operating at very low supply voltage, the stability of the cross-coupled inverter pair is not very promising. In addition, because of the degraded inverter characteristic, the power consumption becomes very high. A Schmitt Trigger based inverter [7] is therefore used to exploit the enhanced characteristic of the inverter. The basic data storage element in a Schmitt trigger -based SRAM cell uses a cross-coupled Schmitt trigger-based inverter pair displayed in Fig 3.1. Schmitt trigger is used as a comparator, with a positive feedback.

Considering the switching of output voltage, Vout from 1 to 0, in the case of inverter, the transition starts as soon as the input voltage reaches the threshold voltage of the pull down transistor, Vthn. On the other hand, in case of ST-based inverter, for Vout = 1, the feedback transistor MNF is ON and the voltage at node VNX is Vdd − Vthn. In this case, the minimum voltage required at the input for switching will be much higher than Vthn.

The characteristic for inverter and ST is shown in Fig.6 (a) and (b).

Due to the improved inverter characteristic by incorporating the concept of feedback, the ST-based SRAM offers higher SNM. In a ST Inverter we get a higher retain and hold time with respect to a normal inverter. By increasing retain and hold time, we reduce the chances of a bit slip or malfunctioning of the system due to error at the input. It thereby results in a more stable and safe circuit to be used. It also has better parametric analysis values at it also reduces the delay and power thereby making the system both speed efficient and hardware effective.

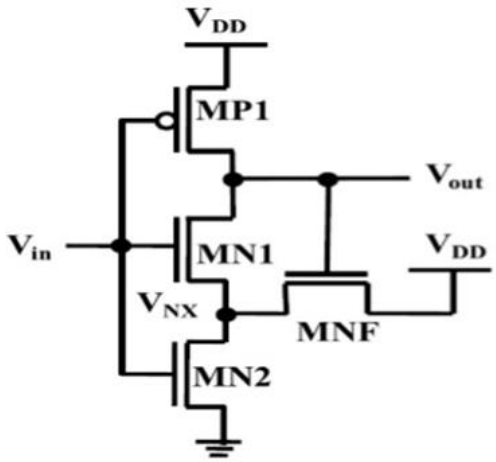

Fig. 6 (a): Schmitt Triggered Inverter

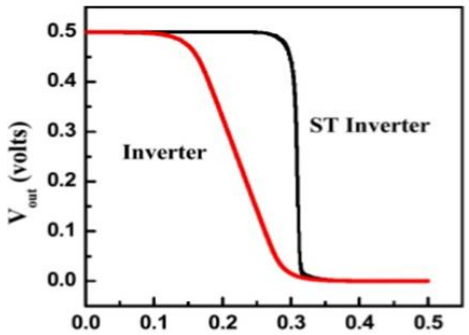

Fig. 6 (b): ST Inverter Characteristic Curve

When logic (1) is feed in at the VIN, an N-mos transistor MN1 and MN2 are enabled and at the same time P-mos transistor mp1 is turned off.When both MN1 and MN2 are ON,it results in a completing the discharge path to ground.Thus 0(GND) flows through the circuit to VOUT.WhenVout is 0, N-mos transistor MNF is off.MNF is basically a feedback transistor which takes VDD as feedback into the junction Vnx.When MNF is off no feedback is given into the junction Vnx.When logic (0) is feed in at the VIN,n-mos transistors MN1 and MN2 are disabled and at the same time P-mos transistor mp1 is turned ON.When both MN1 and MN2 are off,the connection to the GND is broken.WhenP-mos mp1 is ON there is a complete path from VDD to the circuit which makes VDD(logic 1) to flow.Therefore 1 is present at the output Vout.WhenVout is high, it switches the feedback transistor MNF ON. When MNF is ON, VDD flows through it into the junction Vnx thus giving a high feedback into the circuit. The basic importance of the feedback is that we need not toggle the inputs everytime. When an input for example 0 is fed, the output from the inverter is 1 and the same 1 is fed back into the circuit thus enabling the operation for 1 in the next pulse. This results in a higher threshold and it also lowers the power dissipation.In a St Inverter we get a higher retain and hold time with respect to a normal inverter. By increasing retain and hold time, we reduce the chances of a bit slip or malfunctioning of the system due to error at the input. It thereby results in a more stable and safe circuit to be used. It also has better parametric analysis values at it also reduces the delay and power thereby making the system both speed efficient and hardware effective.

As we can see from figure 6 there is a clear difference in characteristics curve between a normal inverter and a ST based inverter. The characteristic curve of ST inverter denoted in black color clearly has a fall off at higher voltage thus resulting in a higher retain time. On the other hand the characteristic curves of a normal inverter being denoted in red colour has a lower fall off and thus have a lower retain time. The fall off of the ST based inverter starts at around 0.3 volts but for a normal inverter it starts as low as 0.1 volts.At the same time the delay can be calculated from this graph and the variation between the St based inverter and a normal inverter can be easily visible. While the ST inverter takes absolutely no time to change its state from 1 to 0 or vice versa(the voltage at which change happens is approximately 0.3v),for a normal inverter to change its state has a higher delay as it takes from 0.1 to 0.3 volts as visible in the graph. Thus ST based inverter results in a more speed efficient approach and this benefits the overall SRAM operation to a great extent.

Schmitt Triggered Inverter Based SRAM Cell

The ST11T SRAM cell comprises of a cell core with a cross-coupled ST inverter, a read path comprising of two transistors, and a write-access transistor. The read-access transistor MAR1 is controlled by row-based read WL (RWL) and, the write-access transistor MAL is controlled by row-based WL. The feedback transistors of MNFR, MNFL, and ST are controlled with the help internal storage nodes Q and QB, respectively, and their drains are connected with a control signal Word line bar (WLB).The WLB and BLs (BL and RBL) are column-based and the virtual ground is row based. The use of VGND and WLB control signals inevitably mitigates the half-select disturb problem in the cell.

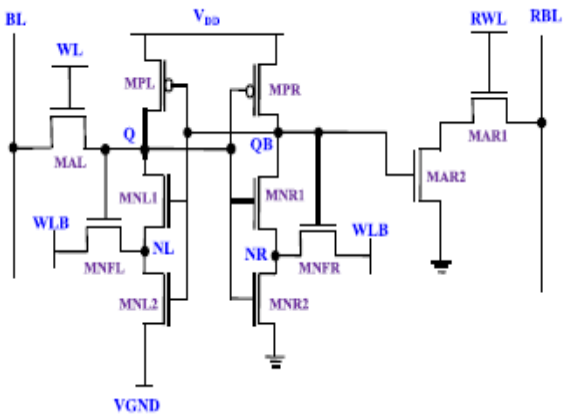

Fig. 7: ST Inverter Based SRAM Cell

During hold mode operation, the word line and read word line both are disabled and VGND is grounded. Hence, due to the feedback mechanism, the cross-coupled ST inverter is isolated from both the bit lines and thus the data-holding capability gets increased.

During the read operation, Word line is disabled, and read word line is enabled, providingdischarging path for read bit line through transistors MAR1 and MAR2 depending on the data which is stored at QB. The disabled word linein turn makes data storage nodes (Q and QB) decoupled from BL during the read access process.

IV. PROPOSED DESIGN

Effect of W/L Ration in Transistor Operation

The gate length specified for a MOSFET technology means the MINIMUM length. In design it can be larger than the minimum length. The W/L ratio is linked to the trans-conductance and the current capability, together with the multiplicity factor m. A higher w/l ratio increases the current gain and subsequently a higher current for a given Vg.In practice, for the gain stages are useful large transistors, i.e. large W/L ratios or/and large m. As example, the differential input stage of Op- Amps needs high gain. However, the good matching of the input differential stage has to be considered as well. In the current mirrors, a higher transistor gate length is beneficial, for a better matching of the mirror's currents. You can play with these parameters in simulations to observe the impact of the length on the mirrors current matching. In general, a larger transistor ensures a better matching because it minimizes the edge effects, but this is paid with a significant area price.Thus by varying the W/L ratio of the feedback N-mos i.e. MNF of Schmitt trigger inverter the hold average delay increases tremendously and also there has been a significant reduction in the average power as compared to the normal inverter.

Modified 11T SRAM Cell

As discussed above, that by increasing the W/L ratio of Schmitt triggered inverter there is a dramatic characteristic improvement as compared to the normal inverter. This characteristic improvement is utilized in the conventional 11t SRAM cell [1].Thus by varying the W/L ratio of the feedback n-mos. i.e. MNFL and MNFR of two cross coupled Schmitt trigger inverter the hold average and the average power of the conventional 11t SRAM varies beneficially. It is evident from both the table that there has been a significant decline in average power while comparing the two SRAM'S. Hence the overall performance of the 11t SRAM cell improves much beyond the expectations.

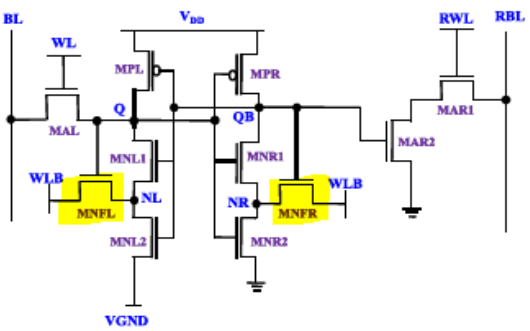

Fig. 8: Modified ST Inverter 11T SRAM Cell

Proposed AND Logic Feed Based 10T SRAM Cell

Keeping the underlying concept of 11T SRAM cell we made few changes to generate an even more beneficial output. Firstly instead of one bit line here in 10T we use two bit lines. Secondly the two cross coupled inverters are replaced by a single AND gate. In our new circuit there is no need for Write Logic or Write Logic Bar, instead we give two normal inputs to the And gate. We know by characteristic property of and gate, when one terminal of the gate is kept high i.e. logic 1, the output of the and gate will then be same as the other unfixed input. This logic of and gate is used for Writing and Hold concept. On the reading part of the circuit, here we use two bit lines which are always high and two discharge N-Mos transistors connected to ground. The last bit line actually stores the written data and the data can be retrieved from that. Overall we are using two P-Mos transistors and 8-nmos transistors in our new proposed design.

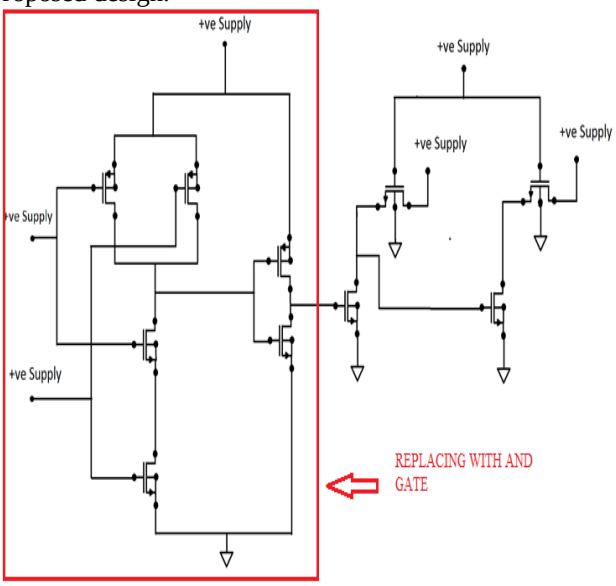

Fig. 9: Proposed AND Logic Feed Based 10T SRAM Cell

Write operation is based on the simple property of and gate. As already mentioned one input to the AND gate is kept high always and therefore the data that has to be written is given on the other unfixed input terminal. Suppose we want to write 0 into the SRAM,the 0 is applied on terminal 1.Terminal 2 being always 0, the output from the AND gate at terminal 3 will also be 0.Suppose we want to write 1 into the SRAM circuit, so 1 is applied in terminal 1.The terminal 2 being always 1,the output at terminal 3 will also be 1.This is how the data is written into the proposed SRAM system.

As far as the hold operation is concerned the data is stored in between the 6 transistors used for and gate and the opposite values keep toggling between terminal2.1 and terminal 3 but this time with a better retaining capacity and lesser delay as compared to the pre-existing 11T SRAM circuit.

For reading the data we initially set both the bit lines high i.e. having a logic 1 and5V DC voltage.

Read 0- When the output at the terminal 3 from the And gate is 0,it fails to turn the transistor D1 ON and so there is no discharge path connected between the bit line B1 and ground G1.Hence when we take the output from terminal 4,the data is high as the B1 did not discharge. Hence the transistor D2 is turned ON and a direct discharge path is connected between the bit line B2 and ground G2.What it does is it makes the bit line B2 to go to 0.So when the final output is taken from terminal 5,the output is 0.Read 1-When the output at the terminal 3 from the And gate is 1,it turns the transistor D1 ON, as a result of which the Bit Line B1 is directly connected to ground G1.Thus the high value stored in Bit Line B1 is discharged to 0.Thus output taken at terminal 4 is 0 and it does not turn ON the transistor D2 thereby providing no discharge path for Bit Line B2 to ground. Thus when output is taken from terminal5 it is always 1.This is how the read operation is performed for both low and high inputs.

V.RESULTS AND DISCUSSIONS

Parametric analysis which includes the transient response, hold / write time delay, average power of conventional 6T SRAM cell, 11T SRAM Cell, Modified ST Based 11T SRAM Cell, Proposed AND Logic feed based 10T SRAM Cell has been done. The simulations were carried out in 180nm library file of cadence virtuoso design software.

Table I: Performance Measures of ST Inverter with Different Channel Widths

Different Channel Widths	DELAY (Sec)	POWER (µW)	Fall off @ (Volts)
2um	9.475E-12	2.506	3.6
1um	10.77E-12	2.501	2.515
4um	7.545E-12	2.511	3.609
8um	3.415E-12	2.517	4.00
16um	3.012E-12	2.521	4.302
24um	3.023E-12	2.523	4.4

From the Table I, it is quite evident that by increasing the width of the channel, delay and fall off voltage varies whereas the average power remains the same. In fact this increase in fall off voltages is beneficial when used in SRAM cell .As the hold time increases, data retention also increases thus improving the characteristic of SRAM cell.

Table II: Performance Comparison of 11T and Modified 11T

Parameters	DELAY (sec)		POWER (µW)	
	11T	Modified 11T	11T	Modified 11T
Hold time(0)	153.6E-12	22.85E-12	9.491	2.38
Write time (0)	154.4E-12	283.2E-12	2.504	2.38
Read time(0)	160.6E-12	33.2E-12	5	2.09
Hold time (1)	165.7E-12	25.65E-9	2.64	2.38
Write time(1)	153.5E-12	4.353E-9	2.5	2.90
Read time (1)	150.4E-12	21.34E-9	5	2.09

Table III: Performance Comparison of Conventional 6T and Proposed AND Feed Based 10T SRAM Cell

Parameters	DELAY (sec)		POWER (µW)	
	6T	10T	6T	10T
Hold time(0)	15.00E-9	124.9E-12	3.382	2.507
Write time (0)	15.02E-9	124.9E-12	3.382	2.507
Read time(0)	14.98E-9	6.9E-12	3.375	2.276
Hold time (1)	15.00E-9	12.95E-12	3.382	2.507
Write time(1)	2.198E-12	12.95E-12	3.304	2.507
Read time (1)	15.32E-9	24.86E-12	1.625	2.276

The overall analysis of the SRAM circuits shows a good improvement in characteristics with every new design. Our proposed 10T cell has improvement in delay and power consumption. Moreover our 10T cell uses one less transistor as compared to the 11T circuit thus making it hardware efficient. The reduction in delay increases the hold and retains time of the cell and also makes the circuit speed efficient as it enhances the speed of working. The overall power leakage is reduced as the average power consumption is reduced.

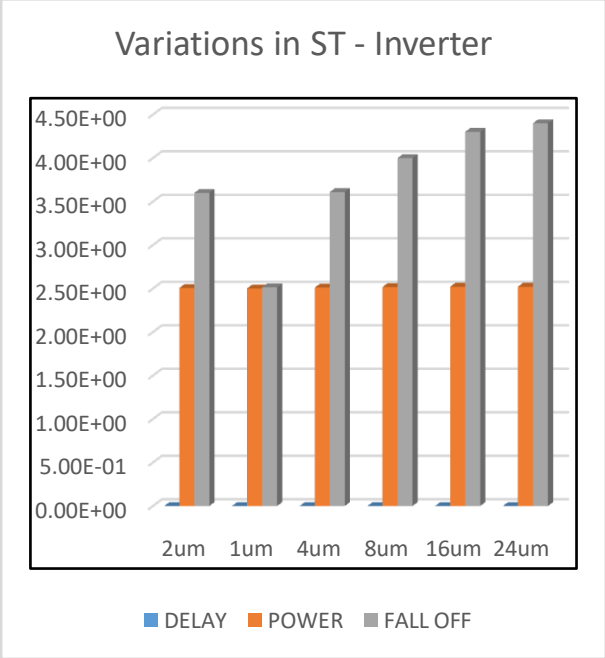

Fig. 10: Chart Showing the Variation in W/L ratio in ST Inverter

The application of the ST Inverter with different channel widths shows the significant effect on the 11T SRAM Cell. From table II and Figure 11, we can observe that the proposed 11T SRAM with increased W/L ratio has high delay average as compared to the normal 11T SRAM cell. Thus driving us to a conclusion that the data retain capacity is high in the proposed 11T SRAM.

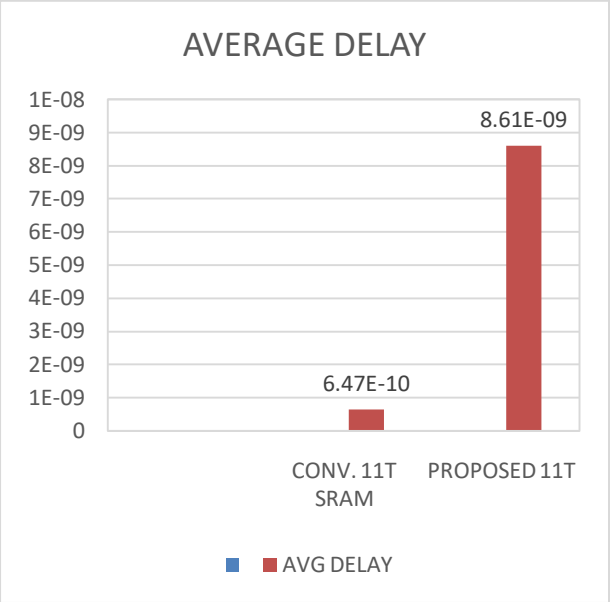

Fig. 11: Chart Showing the Variation in Data Retention of 11T and Modified 11T

VI. CONCLUSION

The newly designed AND LOGIC BASED ROBUST LOW POWER SRAM CELL provides improvement in the fields of power consumption and delay as shown in the tables previously. The newly designed SRAM CELL also uses 10 transistors instead of 11 as was previously used. Thus it provides a more hardware efficient approach too. The delay being reduced enables the SRAM CELL to be more speed efficient and robust. Thus the overall analysis of the SRAM circuits shows a good improvement in characteristics with every new design.

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