Performance evaluation of multiple carrier scalar PWM Algorithms for Cascaded Multilevel Inverter fed Induction Motor Drive

Nayeemuddin.M, T. Bramhanada Reddy, M.Vijaya Kumar

Abstract—This paper explores and compares about different multiple carrier PWM techniques for three-level three-phase voltage source Inverter. Several algorithms for CMV decrease have been proposed in the literature. This paper investigate four various control strategies namely Common Carrier (CC), Inverted Carrier (IC), Phase Shifted (PS) and Inverted Phase Shift (IPS) for cascaded multilevel inverter fed induction motor drive. In Sinusoidal PWM, variable AC output voltage of inverter is produced by comparing a sinusoidal reference signal with triangular signal, where as Conventional SVPWM utilizes complex voltage vector for PWM control. It is seen that SVPWM method makes it conceivable to the fundamental output voltage to increase 15.5% in comparison with SPWM. More over traditional SVPWM method requires angle and sector information for calculating sequences for the gate terminal of the inverter, a simplified SVPWM algorithm is also described, which does not require angle and sector calculation. In this algorithm with the proposed technique it easy to program for pulse patterns generation of various multi carrier based PWM algorithms. To verify and validate the proposed research work laboratory experimental tests have been conducted using dSPACE controller, which proved the reduction in common-mode voltage with fewer harmonics for a motor drive.

Index Terms—Cascade inverters, multicarrier PWM, SVPWM, common mode voltage (CMV), Total Harmonics Distortion.

1. INTRODUCTION

The 2-level inverter produces higher total harmonic content in the stator voltage and current [1-4]. To diminish the THD switching frequency (Fs) has to be expanded, which gives higher switching loss, consequence heating the power devices [5-6]. This problem can be besieged by utilizing the idea of multilevel inverters. Different inverter topologies like capacitor clamped, diode clamped and H-bridge are proposed in the literature [7-10].

The proposed 3-level inverter topology is illustrated in Fig.1. In this circuit, two 2-level inverters are connected in cascaded to accomplish 3-level inversion. From Fig.1, it can be noted that the output phases of inverter-1 are connected to the DC-input points of the corresponding phases in inverter-2 as shown in Fig.1.

The inverter-2 produces a pole voltage \( V_{w_2} = V_{dc} \) at any phase, under the following circumstances:

i) The top switch \( (S_{15}/S_{25}/S_{35}) \) of that leg in inverter-2 is turned on.

ii) The top switch \( (S_{13}/S_{23}/S_{33}) \) of the corresponding leg in inverter-1 is turned on.

Correspondingly, the pole voltage \( V_{w_1} = V_{dc}/2 \) at any phase for inverter-2, under the following circumstances:

i) The top switch \( (S_{13}/S_{23}/S_{33}) \) of that leg in inverter-2 is turned on.

ii) The bottom switch \( (S_{12}/S_{22}/S_{32}) \) of the corresponding leg in inverter-1 is turned on.

From the inverter pole voltage \( V_{w_1} \), the numerical expression for the common mode potential can be derived as

\[
V_{com} = \frac{V_{a_2o} + V_{b_2o} + V_{c_2o}}{3}
\]

Fig.1 proposed 3-level cascaded inverter configuration

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Revised Manuscript Received on June 10, 2019.

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Published By:
Blue Eyes Intelligence Engineering & Sciences Publication
Conventional SVPWM Algorithm

The mathematical expressions for the various zero states time durations and active state time duration in the first sector in case of traditional SVPWM method is given by

\[ T_1 = \frac{V_{ref} \sin(\pi/3)}{\sin(\pi/3)} T_s \]

(1)

\[ T_2 = \frac{V_{ref} \sin(\pi)}{\sin(\pi/3)} T_s \]

(2)

\[ T_Z = T_s - T_1 - T_2 \]

(3)

The calculation of switching times requires sector and angle information which increases difficulty of the algorithm.

Hence to reduce complication involved in conventional SVPWM, simplified scalar PWM algorithm has been proposed which does not require sector and angle information.

Consider three reference modulating signals given as

\[ V_x = V_p * \sin(w_i t - 2(y - 1)\pi/3) \]

(4)

Where \( x = a, b, c \) and \( y = 1, 2, 3 \) ( \( x = y \))

The proposed PWM technique uses the concept of injected zero sequence signal for three phase 3-level cascaded multilevel inverter as shown in fig. 1.

A generalized mathematical expression that generates the zero sequence components \( V_0 \) as a function of \( Z_0, V_M \) and \( V_m \) is given by

\[ V_Z = (1 - 2*Z_0) + Z_0 * V_M + (1 - Z_0) * V_m \]

(5)

Where \( V_M \) is maximum of \( V_i \) and \( V_m \) is minimum of \( V_i \) obtained from magnitude test.

By using the zero sequence component PWM Modulator can be generated, can be expressed in terms of \( V_0 \) and reference signal as

\[ V_1 = V_i + V_Z \]

(6)

Fig. 2. Block diagram illustrating scalar PWM method for cascaded 3-level inverter configuration

By using the idea of unequal division of zero state time, different PWM methods can be generated. When \( Z_0=0.5 \), from equation (5) describes the equal division of zero state time, i.e. \( T_0=\frac{T_s}{2} \) which results in the traditional space vector PWM algorithm. These modulating signals as shown in figure 2 are compared with high frequency carrier signals to produce pulses for inverter-1 and inverter-2.

II. MULTICARRIER CONTROL STRATEGIES

Collectively with the improvement of multilevel inverter topologies showed up the challenge to broaden traditional PWM methods to the multilevel case [12-15]. The proposed work concentrate only on some high switching frequency control techniques such as CC, IC, PS and IPS.

A. Common Carrier Control technique (CC)

A common carrier control technique is shown in Figure 4.

It is one of the PWM control method for multilevel inverter. For N level inverter N-1 in-phase carriers signals and a reference signal with the amplitude (Am) and the frequency (Fm=50 or 60 Hz) are required.

Fig. 3. Modulating signals and zero sequence signals

The control idea is the top carrier and bottom carrier signal are in phase with one another and are compare with a three phase reference signals given in equation (5) to get 3-level operation. Top carrier signal (Amplitude, Am= 0.5 to 1) produces the pulse pattern for inverter-1 and similarly bottom carrier signal (Amplitude, Am= 0 to 0.5) produces pulse pattern for inverter-2.
B. Inverted Carrier Control Scheme (CC)

Figure 5 shows the inverted carrier control technique, top carrier and bottom carrier signal are in out of phase (180°) with each other and are compared with a three phase reference signals given in equation (5) to get 3-level operation. Top carrier signal (Amplitude, Am = 0.5 to 1) produces the pulse pattern for inverter-1 and similarly bottom carrier signal (Amplitude, Am = 0 to 0.5) produces pulse pattern for inverter-2.

Fig. 5 Proposed ICPWM technique for cascaded 3-level inverter

C. Phase Shifted control scheme (PS)

In this phase shifted control technique, each leg carrier signals are phase shifted by 120° horizontally. It may be noted that which is shown in figure 6, top and bottom carrier signals are in same phase.

Fig. 6 Proposed PSPWM technique for cascaded 3-level inverter.

D. Inverted Phase Shifted control technique (IPS)

In this inverted phase shifted control technique, each leg carrier signals are phase shifted by 120° horizontally, and also it may be noted that which is shown in figure 7, top and bottom carrier signals are in out of phase (180°).

III. RESULTS AND DISCUSSION

To assess and prove the validity of the proposed multi carrier PWM methods, experimental tests have been conducted using dSPACE controller on v/f controlled induction motor drive having the following ratings.

<table>
<thead>
<tr>
<th>S.No.</th>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Power</td>
<td>1 Hp</td>
</tr>
<tr>
<td>2</td>
<td>Stator Voltage</td>
<td>415 V</td>
</tr>
<tr>
<td>3</td>
<td>Stator Current</td>
<td>1.8 A</td>
</tr>
<tr>
<td>4</td>
<td>Rotor Speed</td>
<td>1440 RPM</td>
</tr>
<tr>
<td>5</td>
<td>Frequency</td>
<td>50Hz</td>
</tr>
<tr>
<td>6</td>
<td>Effective DC Voltage</td>
<td>540 V</td>
</tr>
<tr>
<td>7</td>
<td>Switching Frequency</td>
<td>1 KHz</td>
</tr>
<tr>
<td>8</td>
<td>Input Voltage for each inverter</td>
<td>270 V</td>
</tr>
<tr>
<td>9</td>
<td>Voltage Regulator</td>
<td>LV20-P</td>
</tr>
<tr>
<td>10</td>
<td>Current Regulator</td>
<td>LA20-P</td>
</tr>
</tbody>
</table>

The obtained results are shown from figure 8 to figure 27.
PERFORMANCE EVALUATION OF MULTIPLE CARRIER SCALAR PWM ALGORITHMS FOR CASCADED MULTILEVEL INVERTER FED INDUCTION MOTOR DRIVE

Fig. 10. CCC Technique at $M_i=0.81$: Voltage THD

Fig. 11. CCC Technique at $M_i=0.81$: Current THD

Fig. 12. CCC Technique at $M_i=0.81$: CMV

Fig. 13. ICC Technique at $M_i=0.81$: Modulating Wave, Pulses

Fig. 14. ICC Technique at $M_i=0.81$: Line Voltage & Current

Fig. 15. ICC Technique at $M_i=0.81$: Voltage THD

Fig. 16. ICC Technique at $M_i=0.81$: Current THD

Fig. 17. ICC Technique at $M_i=0.81$: CMV
Fig 18. PSC Technique at $M_i=0.81$: Modulating Wave, Pulses

Fig. 19. PSC Technique at $M_i=0.81$: Line Voltage & Current

Fig 20. PSC Technique at $M_i=0.81$: Voltage THD

Fig 21. PSC Technique at $M_i=0.81$: current THD

Fig 22. PSC Technique at $M_i=0.81$: CMV

Fig 23. IPSC Technique at $M_i=0.81$: Modulating wave, Pulses

Fig. 24. IPSC Technique at $M_i=0.81$: Line Voltage & Current

Fig. 25 IPSC Technique at $M_i=0.81$: CMV

$+V_{dc}/3$

$-V_{dc}/3$
CONCLUSION

This paper presents multi carrier based scalar SVPWM techniques for cascaded 3-level inverter fed v/f controlled induction motor drive. Traditional SVPWM method requires angle and sector information for calculating sequences for the gate terminal of the inverter, a simplified SVPWM algorithm is also described, which does not require angle and sector calculation. This can be accomplished by adding a zero sequence signal to the sinusoidal modulating signals. In this work four different multi carrier control schemes have been evaluated and tested experimentally. From the experimental results it is concluded that CCC technique gives less harmonic distortion but gives higher common mode voltage Vdc/6 which causes motor bearing currents affecting motor performance. Progressively over, the proposed later control technique reduces higher common mode voltage from Vdc/3 to Vdc/6 with less harmonic content. Finally it can summarized and concluded that among all the four control techniques IPC technique gives fewer harmonic with reduced common mode voltage.

REFERENCES