Primitive Cells using Gate Diffusion Input Technique: a Low Power Approach

G.R.Mahendra Babu, S.Bhavani

ABSTRACT: ***Newer design techniques are the key factor that reduces area and power in VLSI circuits. Reduction in area improves the system functionality and less power consumption improves the energy efficiency particularly in IoT applications, mobile phones, battery based electronic devices…etc. Gate Diffusion Input (GDI) technique is presented in this paper. Using GDI technique, primitive cells such as logic gates and MUX logic function is designed. This GDI based primitive cells and functions are compared with CMOS based design styles. It is clear GDI technique uses less minimum transistors compared to CMOS based design styles. This GDI based primitive cells and functions can be used in adders, multipliers, system building blocks...etc to reduce the area and power significantly.***

Keywords: ***Gate Diffusion Input (GDI), Low Area, Low Power, Primitive cells, CMOS***

I. INTRODUCTION

In VLSI digital circuits, power and area reduction is the important parameter which decides the efficiency of the circuit [4 & 9]. Power consumption is the primary factor in high performance computing application [5-6], Image processing applications [7], Portable applications [8 & 10] and wireless applications. Silicon area also has the direct impact on device size and cost. CMOS logic was introduced in early 80's and from that several design techniques was developed to save power & area and also to increase the speed of operation. Another one design technique known as Gate Diffusion Input (GDI) style [1-3] that replaces CMOS logic and it was originally developed for fabrication in SoI and twin-well CMOS process. In GDI style, complex logic functions such as MUX, encoder, decoder…etc., can be implemented using only two transistors.

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It's clear that, area and dynamic power consumption in GDI style based combinational and sequential logics were significantly reduced as compared to CMOS logics. In GDI style, the voltage swing at the output side is reduced due to threshold drops as compared to pass transistor logic (PTL) technique. This causes the degradation in performance and increased short circuit power. But this performance degradation is negligible, since GDI style uses only two transistors as compared to other techniques.

The performance of the system increases day by day and this results in increasing number of transistors in the circuit. To manage this, it is necessary to develop standard cells with low power to improve the overall system performance. In ASIC design methodology standard cell libraries are required by all CAD tools for IC design. Standard cells are predesigned and verified blocks. This helps the designer to reduce the product development time and easily manages the overall chip complexity. CMOS logic based standard cell are popular and almost used in all designs. Here we proposed GDI style based standard cells and its one of the power reduction techniques compared to CMOS logic.

A single GDI cell consists of one NMOS & PMOS transistor and it has three input terminals and one output terminal. Fig 1 shows the single GDI cell. The advantages of GDI technique are:

(i) Less power dissipation
(ii) Reduced delay
(iii) Reduced area.

II. GATE DIFFUSION LOGIC

Figure 1, shows the single GDI cell and looks like CMOS inverter, since it consists of two transistors. However it contains three inputs, G (common gate input of both the nMOS and pMOS), P (input to the source/drain of pMOS) and N (input to the source /drain of nMOS). Using this single GDI cell, different logic functions (AND, OR NOT) can be implemented as shown in table 1. These logic functions implementation were complex in standard CMOS logic (6-12 transistors), hence these

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logic functions are implemented using only 2 transistors.

The Multiplexer (MUX) function can also implemented using GDI style and it's efficient as compared to CMOS implementation. GDI gates can be affected by threshold voltage drops at the output side which reduces current drive strength and reduces the performance of the standard cells. This drop also increases the direct path static power dissipation. The above said two effects can be overcome by using swing restoration buffers with a multiple Vth approach (MVT). This MVT suggest uses of low threshold transistors where voltage drop is expected.

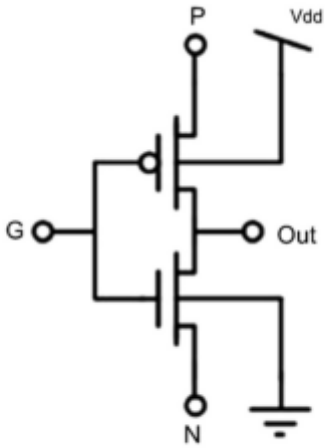

Fig. 1. Basic GDI cell.

Table.1 GDI configuration for AND, OR, NOT & MUX

G	N	P	FUNCTION	OUT
A	B	0	AND	A.B
A	1	B	OR	A+B
A	0	1	NOT	$\overline{A}$
A	S	B	MUX	AB+$\overline{A}$S

Using this technique, voltage drop will be minimized. Also high threshold transistors can be used to minimize the above said effects.

Majority of the digital designs are based on CMOS NAND and NOR gates. This two functions as a universal gate set and uses 4 transistors for implementation. The above table 1 shows GDI based standard cells AND, OR & NOT which uses only 2 transistors as CMOS technique uses 6 transistors to implement the same functions.

In the above table 1, GDI based MUX implementation is also shown. The implementation of GDI based standard cells and MUX function is discussed in the next chapter.

GDI TECHNIQUE BASED LOGIC GATES (PRIMITIVE CELLS)

AND GATE

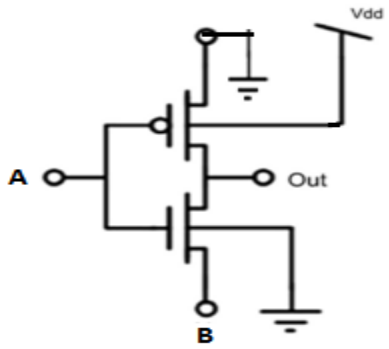

Fig.2 GDI based AND gate

Fig.2 shows the GDI based AND gate. Input 'A' is connected to gate input terminal of both NMOS and PMOS. Input 'B' is connected to NMOS source terminal and NMOS bulk is connected to ground. PMOS source is connected to ground and PMOS bulk is connected to Vdd.

OR GATE

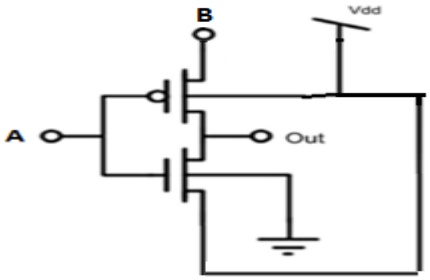

Fig.3 GDI based OR gate

Fig.3 shows the GDI based OR gate. Input 'A' is connected to gate input terminal of both NMOS and PMOS. Input to the NMOS source terminal is connected to Vdd and NMOS bulk is connected to ground. Input to the PMOS source is connected to input 'B' and PMOS bulk is also connected to Vdd.

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NOT GATE

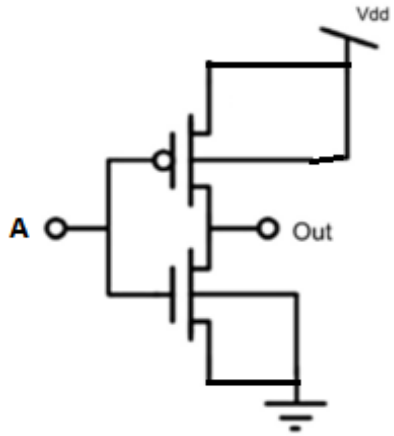

Fig.4 GDI based NOT gate

Fig.4 shows the GDI based NOT gate. Input 'A' is connected to gate input terminal of both NMOS and PMOS. Input to the NMOS source and NMOS bulk is connected to ground. Input to the PMOS source and PMOS bulk is connected to Vdd.

MUX

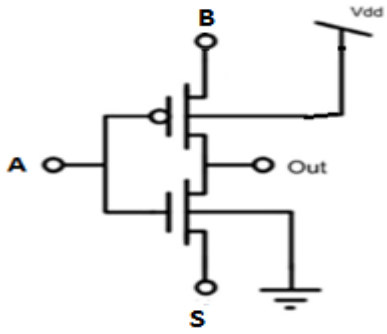

Fig.5 GDI based MUX

Fig.5 shows the GDI based 2x1 MUX. Input 'A' is connected to gate input terminal of both NMOS and PMOS. Selection line 'S' of MUX is connected to the NMOS source terminal and NMOS bulk is connected to ground. Input 'B' is connected to PMOS source terminal and PMOS bulk is connected to Vdd.

III COMPARISON OF GDI AND CMOS LOGIC STYLES

The GDI and CMOS logic design styles are compared based on the number of transistors required. In GDI logic design style two transistors are enough to build logic functions such as AND, OR, NOT and 2x1 MUX. Whereas in CMOS logic design styles the transistor count increases for the above same logic functions as shown in table 2.

Table.2 No of transistors required for logic functions

Logic Functions	GDI design style	CMOS based design style
AND	2	6
OR	2	6
NOT	2	2
MUX (2x1)	2	4

In this paper, CMOS based design styles are not discussed in detail. Since the CMOS based style is familiar and it's discussed. From the table 2, it is clear that the number of transistors required for logic functions such as "AND, OR, NOT and MUX" is less in GDI design style compared to CMOS based design style. For logic function 'AND' and logic function 'OR' the transistor count is reduced to 33 %, for logic function 'NOT' the transistor count is same as CMOS based design style, for logic function 'MUX (2x1)' the transistor count is reduced to 50 %.

Almost in all the above logic functions except 'NOT', the transistor count is reduced. This will reduce silicon area and hence the power consumption is also reduced.

IV CONCLUSION

The Low power primitive cells are required for ASIC designers to incorporate in all digital circuits such as adders, multipliers, decoders…etc. In order to incorporate more function in silicon die, circuit complexity has to be reduced to achieve low area. Gate Diffusion Input (GDI) technique reduces the transistor count compared to CMOS based design style. From table 2 its shown that, the transistor count is reduced to 30 % for logic function "AND & OR", the transistor count is reduced to 50 % for logic function 'MUX' and the transistor count is same for logic function 'NOT'. This drastic reduction in transistor count reduces the area and power significantly. The GDI based low power primitive cells can be used to build digital circuits for low power designs.

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