

Simulation of Network on Chip for 3D Router Architecture

Navinkumar Agrawal, Arpit Jain, Ambuj Agarwal

ABSTRACT—A NoC can be structured and arranged by various topologies in terms of complete organization of the routers and cores and the approaches used to understand the technique for routing, flow control, and switching. The data flow control is related to the data traffic or intensity inside the routers and in the channels. Routing is a technique or method that defines the optimized path between a data or message to take place from the transmitter to the target end or receiver. The research work focuses on the modeling, simulation and synthesis of mesh and ring topological network. The cluster size of the network is considered as (2×2) , (4×4) , (8×8) , (16×16) , (32×32) , (64×64) , (128×128) and (256×256) for 2D NoC design and $(2 \times 2 \times 2)$, $(4 \times 4 \times 4)$, $(8 \times 8 \times 8)$, $(16 \times 16 \times 16)$, $(32 \times 32 \times 32)$, $(64 \times 64 \times 64)$, $(128 \times 128 \times 128)$ and $(256 \times 256 \times 256)$ for 3D NoC router design.

Keywords—Network on Chip (NoC), Router Architecture, System on Chip (SoC).

I. INTRODUCTION

Integrated circuits design and their manufacturing is completely depends on the integration of different sub modules which are the pre design block of the intellectual property (IP) and cores at single chip. The property of reprocessing is always resided in any ICs design. Manufacturing and semiconductors companies are working on the new challenges in the field of network on chip design and their throughput. The reuse of already developed sub modules or functional blocks is a new idea to design the circuits having high performance in shorter time period having larger gate counts.

Traditionally the approach of System on Board (SoB) was used in which each block of the function is created and manufactured individually after that they mounted in a discrete board while now a days SoC used which has a single chip, in which all the cores are synthesized together. Later on the entire functional blocks are synthesized and manufactured in different units, and can be mounted in a discrete board. SoB is based on the already developed blocks. Moreover, the parts of SoC that can be reused are called virtual modules which are only used as the functional logics instead of fabricated ICs. It expresses a main comparison among the core based systems and traditional design methods.

The design and development time of the products depends on the technological expertise of the design, verification, signal processing, and security by encryption and decryption, RF design and analog interfaces. It is very difficult to predict that the technology has only the single house challenges. The chip size reduction, minimize power

consumption, higher throughput, minimum delay, less area, reduced memory, fast response are the general requirements of these application. Moreover, it is the requirement that the all functions modules should be integrated in the system such as ADC, DAC, memory, microprocessors, mixed signal blocks etc. The business model is following the optimized design cycle to meet the requirements of application engineer, follow the RF or core solutions and focus on the basic system aspects.

II. NETWORK ON CHIP (NOC)

NoC provides the architecture and communication model in which multiple nodes can communicate and utilize the resources. Due to this reason, it is possible to design and implement the chip working under independent resource utilization in one block and multiple blocks as the working node or processing element of the communicating network. The flexibility and scalability in the chip design is cable to provide the feasibility to configure the NoC with different cluster size and workloads. The NoC architecture consists of the multiple resources which are designed and arranged in particular topology.

III. 3-D ROUTER ARCHITECTURE

The router is the device used to forward the data packets in communication network. The data packets are transferred from one source router to another destination router in the inter network. Router connected to two or many data lines inside the network to transfer the packets to destination. When the data packets are arrived on these lines the router read the address of then destination network to deliver the data packets. In the routers can transmit the packets from one network to another network in this way. The common used routers are small office routers and homes which are passing simple IP based routers between the internet and home computers. The example of a router can be DSL or owner's cable that provides the connectivity to the internet through internet service provider (ISP). Some examples of the more safe and sophisticated routers are enterprise routers which are helpful to connect large ISP networks and large business networks as power main routers that can forward the data at very high speed rate in the direction of the optical fiber lines along with internet backbone. The routers are designed based on dedicated routing and these are dedicated hardware device. There is the existence of software based routers also.

Revised Manuscript Received on May15, 2019.

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Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

The interconnections are not depending on the communicating network cluster size. The routing of the 2D network can be done in easiest way and gives the overall scalability, large bandwidth and short period clock cycle. The NoC have the switches are resources which are interconnected in such a manner that they can communicate directly among each other using packet data transfer technique. The resource is the computation and storage unit. The NoC switch is used to provide the path or routing to incoming traffic and buffered the same traffic between the other resources. There are many inputs and output channels or interconnections through which the switch can connect to other neighbor's switches. Each interconnection channel has two or more buses in one direction between two switches as point to point connections. The incoming traffic is handled using wait and go technique for queue and controlled by switch.

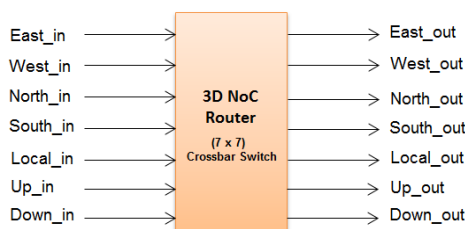


Fig.1- 3D NoC Router

IV. NOC ROUTER WITH 3D

The crossbar switch (7 x 7) for 3D NoC is shown in figure 1. The 3D router accept the seven inputs and seven outs as input and output directional ports.

The data is coming from down input ports, south input port, east input port, north input port, local input port, Up input port, west input port in the packet form and connected to the control unit which decide the size of the data packets need to transmit. The data coming from the east output port, west output port, north output port, south output port, local output port, Up input port, Down input ports is stored in their associated registers. The architecture of 3D NoC Router is shown in figure 2 that depicts the functionality of the NoC design.

V. ROUTING

Routing in NoC is very important to suggest the optimal path. The routing algorithm, decides the output port for the forward packet. There are many routing techniques used to address in NoC, each one having several tradeoff between cost and performance. The same path is used by the data packet in case of deterministic routing, when communicating between two particular nodes. The general deterministic routing schemes used are XY routing and source routing. Source core are used to specify the route to destination in source routing. In case of the XY routing technique, the row and column approach for routing is used in which the packet is moving towards rows first and then towards column or vice versa is also possible. In another routing technique, alternative paths are possible to communicate among different nodes, in case of original link or path is not available or route is congested. This routing is referred as adaptive routing. This routing is used in modular approach

based design for large scale networks in which multiple chances may occur of failure the original links and traffic may be delayed or blocked due to the discontinuation of the original link.

The link load is evaluated using dynamic evaluation technique and follows the strategy based on dynamic load balancing. The other examples related to adaptive routing methods are Negative First (NF) algorithm and West First (WF) algorithm.

The static routing is also one of the important routing that provides the local path between the different cores and depends on the time required in the completion of the application, but in case of dynamic routing the routing path is depending on the run time required in the completion of the communication. The data packet can have a single target to deliver the data, called unicast routing whereas one data can be routed to multiple nodes simultaneously with the help of multicast routing technique. It is similar to bus communication or the concept used in master-slave node communication. In the same way, a broadcast communication has the destination for all the nodes but narrowcast communication is started by a master node and associated with single slave. The routing method is also said as minimal routing or non-minimal routing.

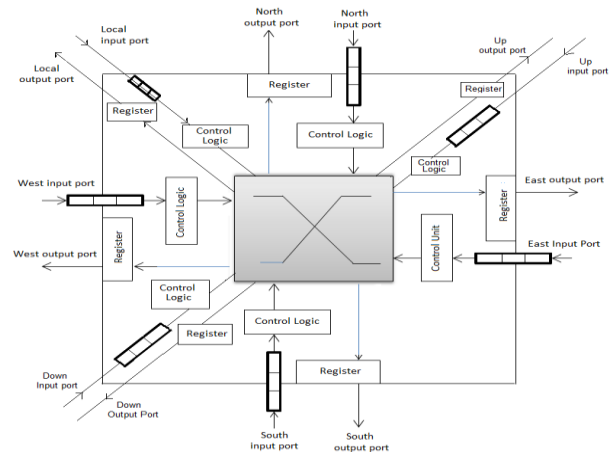


Fig. 2 The Architecture of 3D router

VI. FLOW CONTROL

A flow control is the method for packet movement along the NoC because it is involved at both level NoC chip level and local router level. It is possible to do flow control and judge the deadlock free routing for specific measures to avoid certain paths within the NoC. The optimization in the NoC depends on the channel requirements and bandwidth and it can guarantees the requirements and need of flow control. The selection technique of the routing algorithm reduces the critical path and traffic congestion is minimized by implementing virtual connections. The quantity of the communication infrastructure and performance is called the Quality of Service (QoS).

The control mechanism is NoC can be classified as centralized control or distributed control. The routing decisions are taken globally and applicable to all the nodes



associated in NoC, followed with a strategy that guarantees that traffic contention is not affecting the NoC performance. The approach avoids the bus requirements that all nodes are sharing in bus in a common time. Time Division Multiplexing (TDM) approach is used in which each packet is concern to frame. The NoC uses the distributed approach in which each router can take the decision locally. Virtual channels are very important for the flow control in NoC. These channels are helpful in multiplexing a single physical channel over different or separate logical channels associated in single and independent buffer queues. The actual use of the VC is to implement the NoC to enhance the performance to avoid deadlocks, increase traffic handling capacity, and optimize wire usage. The situation of the deadlock may occur when multiple request sate coming to service node and network resources are fully busy and the nodes are waiting to each other to be that the connection will be free or nodes are waiting to release the connection and proceeding with the communication entity. It is also possible when the two communicating paths are blocked in cyclic manner. If the status of the resources is changing time to time, live lock may occur but no guarantees of communication may be successful.

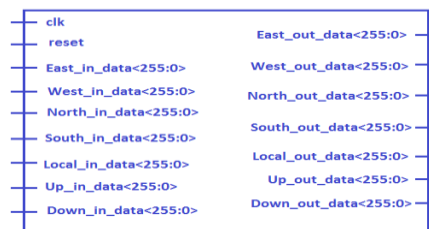


Figure 3: RTL of Router in 3D

VII. RTL AND WAVEFORM SIMULATION

The RTL view of the developed 3D router chip is shown in figure 3 and its internal schematic is depicted in figure 4. Internal schematic presents the internal structure having different logic gates and internal hardware required in the design. Figure 3 shows use, size and detail of the pins used. The functional verification is carried for 256 bit data transfer and simulation waveforms are shown in figure 6. Modelsim waveform in Figure 5 presents the result for 3D router for 256 bit data transfer in hexadecimal and ASCII. The data is coming from the port local_in_data<255:0>, Up_in_data<255:0> and down_in_data<255:0> and output is obtained at local_out_data<255:0>, Up_out_data<255:0> and down_out_data<255:0>.

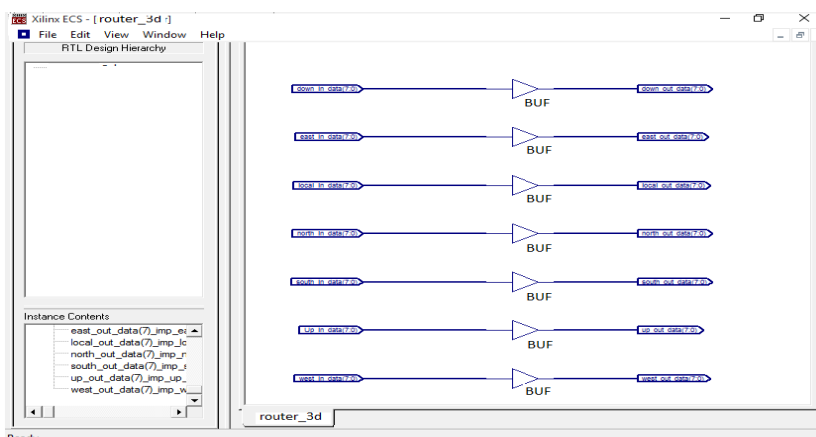


Figure 4: Internal schematic of the 3D router

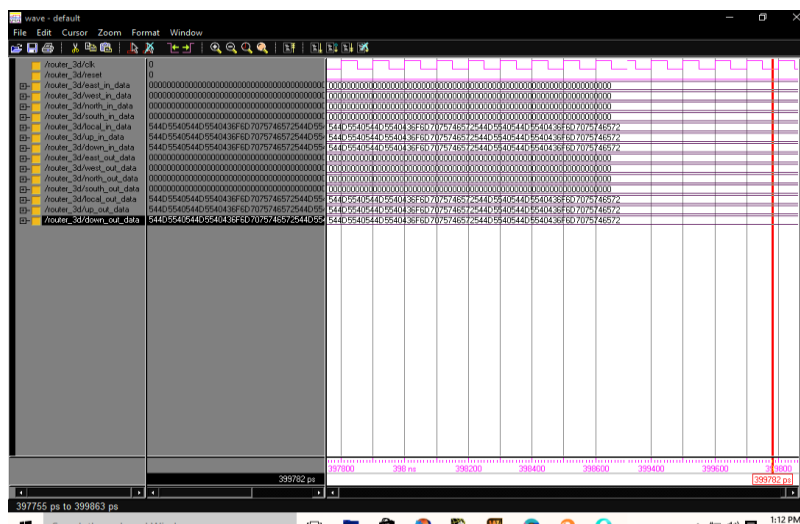


Figure 5: Modelsim waveform result for 3D router data transfer, 256 bit (Hexadecimal)



VIII. FPGA HARDWARE UTILIZATION

The hardware summary report extracted directly from the Xilinx software about device utilization is the detail of utilized FPGA device hardware parameters. The synthesis report is generated and contains the information for hardware utilization in terms of No of slices, No of flip flops, No of input LUTs, Number of bounded IOBs and No of gated clocks (GCLKs) used in the implementation of design. Timing analysis is also carried out for the staged network which provides the information of delay, minimum period, and maximum frequency, minimum input arrival time before clock and maximum output required time after clock. In future the same can be designed with more cluster size.

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