

# An Improved Genetic Algorithm for 3d Ic Partitioning In Asic Design

R.Dinesh, R.Manikandan

**Abstract :** Partitioning is the course of dividing a chip into sub-blocks in VLSI Physical design cycle. Partitioning in VLSI is well-thought-out to be a NP hard problem and such problems can be solved using numerous heuristics algorithm. The problems are global optimum in Very large-scale integration circuit partitioning. VLSI Partitioning theatres a foremost role in Very Large-Scale Integration physical design flow. The circuit is sliced towards sub-circuits, so called blocks. The sub-divided blocks are assigned into one layer in 3D IC partitioning. The primary aim is to reduce interconnections among non-contiguous layers. The rapid growth in technology (3D) IC designs allowed devices to be fabricated in smaller size. Using through-silicon via (TSVs) between adjoining dies the IC stack vertical connections are made to get 3D-ICs. In 3D IC partitioning interconnect delay is drastically limited when correlated with 2D IC partitioning by using Through Silicon Via (TSV). The article focuses on genetic algorithm with a new factor called force which is used for 3D partitioning. The proposed work is to modify genetic algorithm with probabilistic moves instead of random moves. Genetic Algorithm is one of the approaches that is used broadly. Experimental results show that the force-directed move triggers the convergence which coax the better result i.e., cost function evaluation of genetic algorithm maintaining the excellence of execution time. Force Genetic Algorithm (FGA) is effectual in 3D IC partitioning and perhaps used in further optimization problems. In MATLAB genetic algorithm (GA) gives the good result in ASIC design when compared to other methods.

**Keywords:** 2D and 3D IC, Force-directed Genetic Algorithm, Force-directed Simulated Annealing, VLSI Partitioning, Through-silicon via (TSV).

## I. INTRODUCTION

As already known, it is not conceivable to partition the whole wafer in the single stride considering the boundaries of memory space along with computation time. Thus, the circuit is sliced towards sub-circuits, so called blocks. Block size, block quantity and number of interconnections among blocks are the factors that are taken into account when it comes to partitioning. In recent days partitioning has become an exigent task as a consequence system complexity is increasing constantly [1]. 3D heap manifold dies and a smaller footprint is obtained by vertical interconnect [2]. To carry out vertical interconnects between different layers through silicon via (TSV) is one of the efficient techniques.

The interconnect delay is drastically reduced in 3D partitioning using TSV when correlated with 2D. TSV fabrication process still experience large TSV pitch size as well as relatively low yield. Henceforth, using minimum number of SVs is enviable in yield and area cost [3]. In physical design reducing number of TSVs is the primary step for partitioning. Sub-blocks are placed one above other and connections between adjacent partitions marks in using more than one TSV in 3D circuits [4]. In physical design, Genetic algorithm (GA) is one among the approaches that are used. GA is known for its promising result, when compared to the other methods using ASIC design in MATLAB. The objective is to advance GA which improves the act of genetic algorithm by speeding up the evaluation of fitness value and display that the force-directed genetic algorithm gives better fitness/cost function value compared with the existing methodology.

## II. EXISTING METHODOLOGY

As many heuristic algorithms available now-a-days, the existing method addressed about simulated annealing by introducing a new factor called force in it. The solution of SA is switched by a random neighbour solution in FSA. The main difference between standard SA and FSA are in the force update and neighbour function. As 2D partitioning it is projected to divide the circuits into numerous partitions to get the initial solution. The partitions are placed one above the other, so called layers. After merging to get a minimum number of TSVs the layers are ordered using the linear ordering technique. Some cells are being applied by forces that are connected directly to the layers but are in different layers. The tiers are assigned with the cells in 1D placement such a way the force from one layer does not impose another. One dimensional placement is for reducing the complexity of the program [5, 6, 7, 8]. The FSA chooses a block randomly and the shortest distance is analysed with 100 iterations using MATLAB and the result is given below. However, the FSA gives the result with low computation time, the main drawback of FSA is that its result is not that optimized.

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III. PROPOSED METHODOLOGY

A) Force-directed Genetic Algorithm

Genetic Algorithm are said to be a population-based optimization technique. In genetic algorithm cross over operator plays an imperative role to avoid information loss [9]. The algorithm creates an initial population as its primary step. Then the fitness function of each block is determined, where fitness function can be well-defined as addition of wire length with chip area [10]. The genetic algorithm chooses an individual from the existing population as random and proceeds with it. Likewise, the functioning of Force-directed Genetic algorithm in VLSI partitioning is shown in the below figure.4 and the optimization process starts by selecting a random block from rectangular blocks of the IC [11]. Then their cost function is evaluated for each block to optimize the area. In the resulting step crossover is performed by taking any two rectangular blocks from several blocks, which gives a new partitioning output [12]

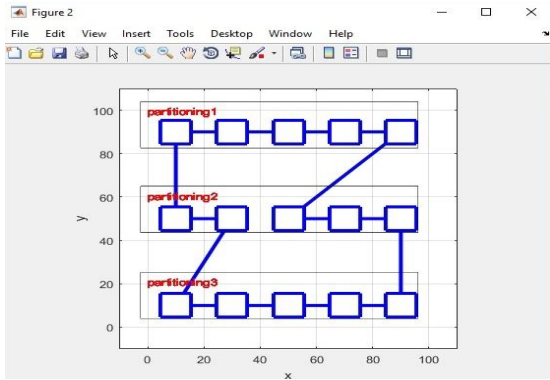


Figure: 1 Partitioning of cells using Force-directed Simulated Annealing

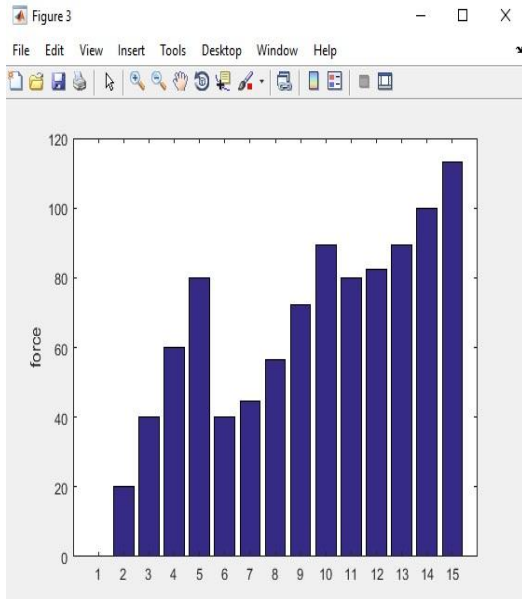


Figure: 2 Applying Force factor step-by-step

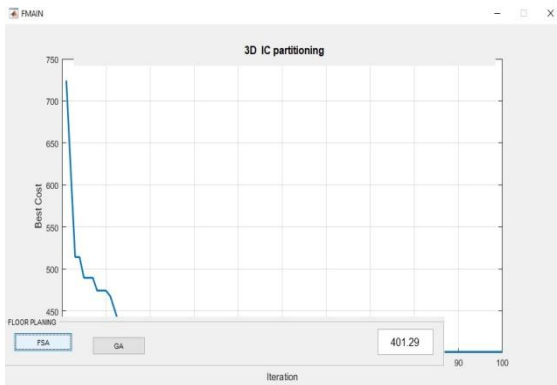


Figure: 3 Cost function of Force-directed Simulated Annealing

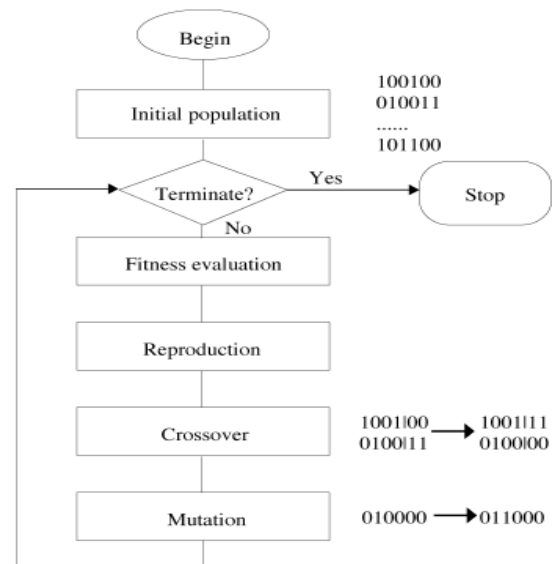


Figure: 4 Force-directed Genetic algorithm flowchart

Mutation is done by reversing the blocks in the chip. The new partition output thus achieved is added to the chip. The random moves are changed into force-directed moves as mentioned in the diagram. Then, the cost function is evaluated once again and the procedure is continued until a shortest distance with desired objective is achieved.

IV. EXPERIMENTAL RESULTS

The proposed force-directed genetic algorithm is implemented using MATLAB version 9.1. The output obtained is having reduced cost function as well as minimum area i.e., shorter wire length due to the application of force-directed moves instead of random moves. The below result is implemented with 100 iterations.

Optimization Algorithm	Best Cost Function
Force-directed Simulated Annealing	401.29

Table: 1 Cost function of Force-Directed Simulated Annealing in 40 iterations

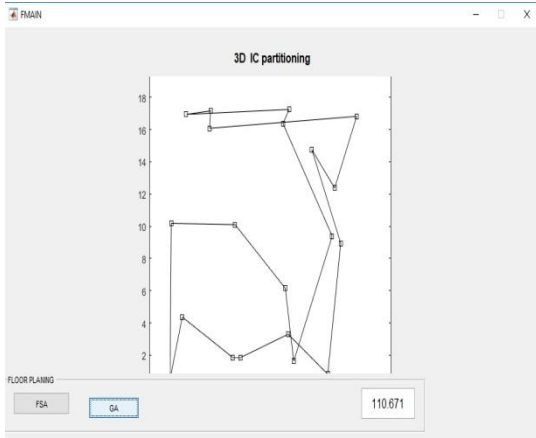


Figure: 5 Partitioning of cells using improved genetic algorithm

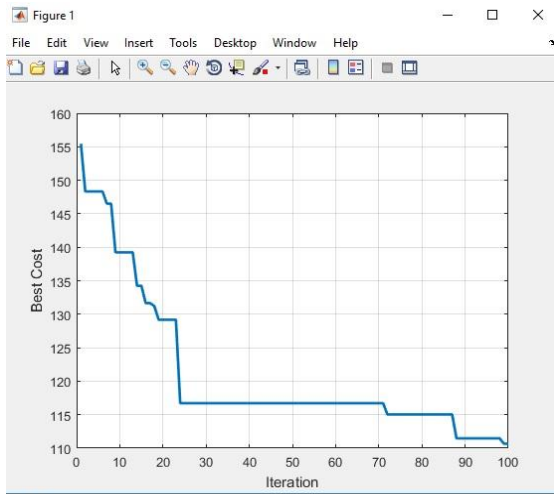


Figure: 6 Cost function of improved genetic algorithm

Optimization algorithms	Best cost function
Force-directed Simulated Annealing	401.29
Improved Genetic algorithm	110.671

Table: 2 Comparison of cost function between two algorithms

The experimental output shows that from the above methodology force-directed genetic algorithm has an excellent cost function reduction and gives a best solution compared with other algorithms.

### V. CONCLUSION

In general, area, power consumption and speed are the major factors when it comes to VLSI design. The proposal behind this study is to achieve minimum wire length while assigning the modules in the chip by partitioning process. This paper gives a comparative study about force-directed simulated annealing and force-directed genetic algorithm based on its cost function which is implemented using MATLAB. From the above two algorithms, the improved genetic algorithm gives the better result with optimized cost function. The future work that is taken in to account is the

computational time as genetic algorithm needs it more when compared with other algorithms.

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