International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-8, Issue-1, May 2019

Design of Modified Reconfigurable Unsymmetrical Six Parallel FIR Filter with Retiming Technique for Low Power & High Speed Applications

P.Radhika, T.Vigneswaran, J.Selvakumar

Abstract: ***Currently, filters with larger length are being widely used in several applications. Hence parallel processing is needed for digital signal processing (DSP) applications. Parallel reconfigurable FIR filter is mainly used for several applications such as SDR, multi standard video codec, digital communication system and wireless communication etc. Fast Fourier algorithm (FFA) technique is used to design the parallel FIR filter to reduce the complexity of the filter structure. The ordinary six parallel FIR filter without FFA and with Wallace multiplier is designed in the conventional technique. It needs more number of adders and multiplier to perform six parallel FIR filter. Hence the area and power is high in the existing filter. FFA technique is applied in the proposed six parallel FIR filter to reduce the number of adder and multiplier by simplifying the existing filter equations. Also the compact booth multiplier structure is applied in the proposed filter instead of Wallace multiplier. Hence it is called as Modified Reconfigurable unsymmetrical six parallel FIR filter (MRUSPF). The MRUSPF structure is presented in this paper to reduce the number of adders, register, half adder and full adder by clustering the filter coefficients. The number of gates and transistors are reduced by using logical and circuit level reduction method based on Boolean logic. Also sum of the coefficients are reused. Combinations of 2X2 FFA and 3X3 FFA structures are used to form the reconfigurable unsymmetrical six parallel. Also retiming technique is applied in reduced carry select adder, booth multiplier and proposed six parallel FIR filter to reduce the number of registers and switching activity of the clock. Retiming is nothing but changing the position of delay element such as flip-flop in order to achieve low area and low power. Simulation and synthesis processes are carried out by analog and digital Cadence virtuoso tools with 90nm CMOS technology. From the obtained results, it is concluded that, the proposed reconfigurable unsymmetrical six parallel FIR filter with retiming technique provides 28.3% power reduction and 50.3% delay reduction than the conventional proposed six parallel FIR filter without retiming structure.***

Index Terms: ***Reconfigurable Unsymmetrical six parallel FIR filter, retiming technique, FFA technique, Wallace multiplier, booth multiplier and reduced carry select adder.***

I. INTRODUCTION

Generally, Digital signal processing (DSP) is mainly used in an extensive range of concurrent applications. Also digital finite impulse response (FIR) filters is the one of the fundamental processing elements, which is mainly used to improve the stability.

Revised Manuscript Received on 30 May 2019.
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Implementation of digital FIR filter is the one of the easiest scheme when compared to analog FIR filter design [1]. Although, the existing FIR filter needs high area and power consumption due to large number of multiplier a

FIR filters is mainly used in the mobile communication. Consequently, an efficient design and implementation of FIR filters is achieved by using several schemes. In the multiple constant multiplications (MCM) method, the coefficient value is constant. We cannot change the coefficient value during the run time. But in the programmable shift method (PSM), the coefficient value can be altered during the run time. In this work, the binary common sub expression elimination (BCSE) based MCM technique with FFA is followed to generate the different coefficient by reusing the number of shift and adder. Hence the power and delay is lower than the all other conventional techniques [2]. This technique is applied only for single filter operation. If we need to perform more number of filters at the same time, we have to apply this filter sequentially. Hence the delay is high.

Parallel (or concurrent) processing can be beneficial to digital FIR filters to similarly reduce the power utilization of the unique filter and increase the effective throughput [3]. Implementation of the sequential FIR filter is extensively used in parallel FIR filter design. The parallel FIR filter with sequential implementation offers low resource utilization (area) and low power consumption when compared to the existing parallel FIR filter. Normally, the application of parallel processing into an FIR filter involves the replication of the hardware units that exist in the unique filter. The L-parallel FIR filter circuits needs L X A area utilization, where A is the area of unique filter circuits. Currently, the coefficient reuse technique is used in the parallel FIR filter design to attain low area and low hardware cost by reducing the number of multiplication and additions. In the existing scheme, the ordinary six parallel FIR filter without grouping the coefficient and FFA is designed, which needs more power and high delay. To avoid this kind of problem, the new compact six parallel FIR filter is constructed in this paper by using FFA, reduced XOR gates, full adder, multiplier and retiming technique in order to obtain the high speed and low power. Also previously FFA based parallel filter is designed up to four parallel structures. But in this paper a compact six parallel is designed using FFA.

II. DESIGN OF A MODIFIED CARRY SELECT ADDER WITH REDUCED XOR GATE

The design of a modified XOR gate by using improved gate diffusion input (IGDI) logic is presented as shown in Fig.1.

In the existing XOR gate by using regular GDI logic requires 4 transistors to perform the XOR operation. It consumes more area and power. To overcome this problem, the improved XOR gate is proposed by using circuit level reduction to achieve low area and low power than the existing GDI logic based XOR gate.

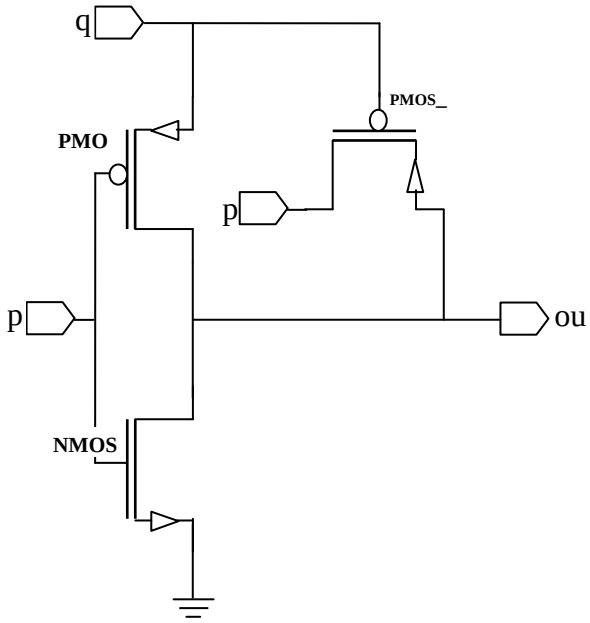

Fig. 1. Circuit diagram of a reduced XOR gate for adder and multiplier circuits.

The schematic diagram, of 8-bit reduced carry select adder is shown in Fig.2 [5]. This circuit is designed by using Boolean logic with Demorgan's theorem. It consists of AND-OR logic circuit as in Fig.3, half sum generation, half carry generation units and XOR gate. This adder is designed by using only half adder instead of full adder. So it provides low area and low power than the existing carry select adder. Also improved GDI logic based reduced AND, OR, XOR and half adder circuit is incorporated into the proposed carry select adder to achieve low area & low power than the existing adder circuits [6]. Finally, this adder is used in the Wallace multiplier and reduced six parallel FIR filter circuits

III. DESIGN OF WALLACE AND BOOTH MULTIPLIER WITH REDUCED FULL ADDER

Wallace multiplier is mainly used for high speed application. Similarly, the booth multiplier is generally used to reduce the resource utilization (area) and power of the circuits. Wallace multiplier is designed by using the half adder and full adder as the basic building block [7]. Initially, the partial product is generated and stored in invert triangle form in dot notation.

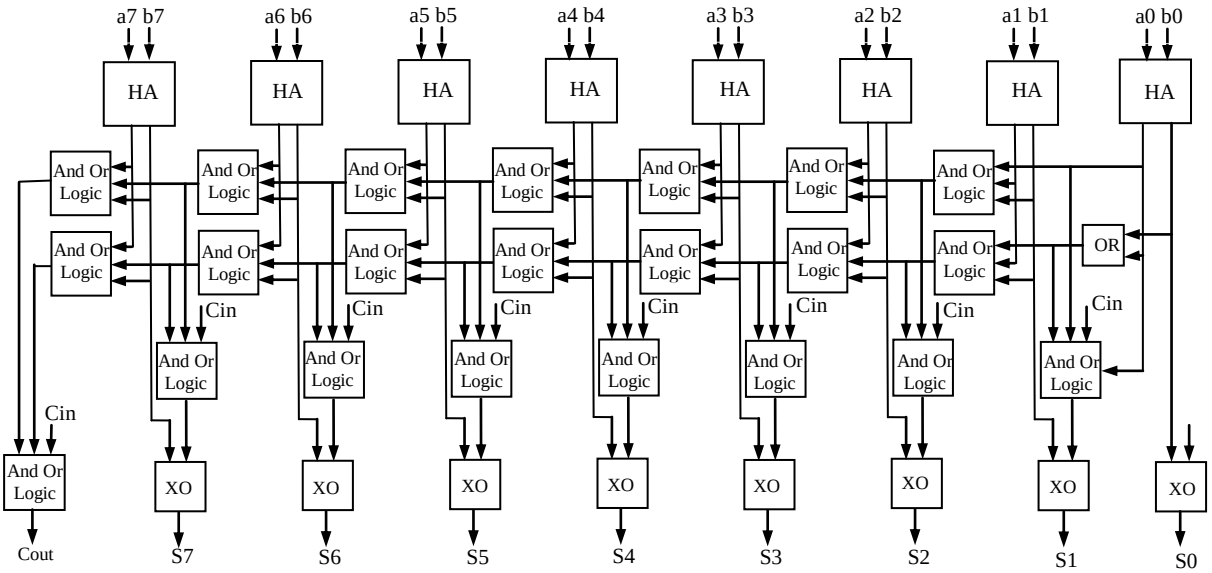

Fig. 2. Schematic diagram of 8bit reduced carry select adder.

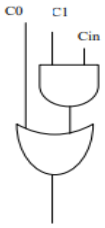

Fig. 3. Circuit diagram of AND OR logic.

The full adder is applied for to reduce the partial product generation stages. The partial product generation stage is reduced into 2 from 4 stages for 8x8 Wallace multiplier structures [8]. The performance is better than the booth multiplier. But area and power is high in Wallace multiplier. Because large number of full adder and half adder are used to design a Wallace multiplier. To overcome this problem, booth multiplier is designed in the proposed technique.

The booth multiplier is designed by using data path unit and FSM modules.

The multiplier is designed based on add & shift method. This multiplier is used to perform both signed and unsigned multiplication operation. Also approximate radix4 recoding technique is applied into booth multiplier in order to reduce the number of shift and add operation. The radix4 recoding technique is formed by using the truth table of radix4 recoding technique. Y means only one shift, -y means shift and subtract,2y means 2 shifts and add -2y means 2 shifts and subtract. 3y is formed by adding y+2y or 4y-y. Finite state machine is used to control the shift and add operation based on radix4 recoding technique. Also control signal is generated to data path units [9]. FSM consists of present state logic, next state logic and output logic. Two types of FSM are there such as Moore and Mealy FSM. In Moore FSM the number state is higher than the number of bits. But in the mealy, the number of states is equal to the number of bits in state diagram. A compact full adder is proposed to further reduce the area and power of the Wallace and booth multipliers.

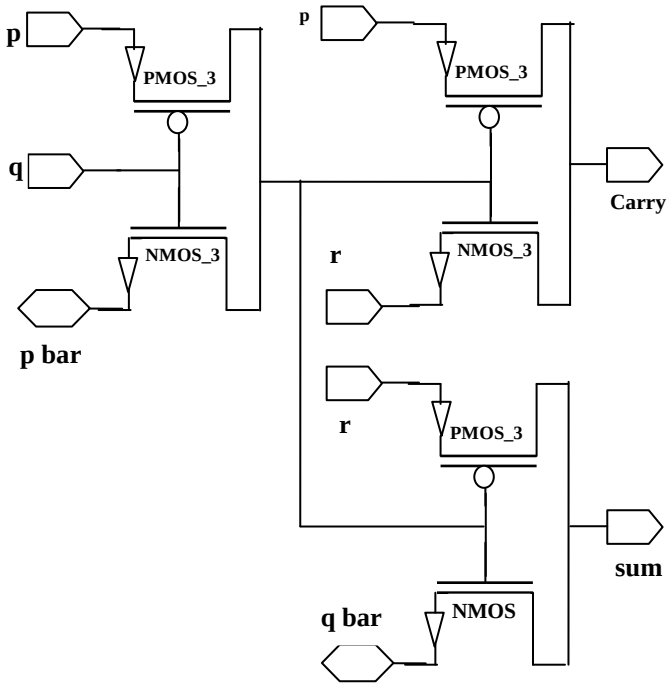

Fig. 4. Circuit diagram of compact full adder for Wallace and booth multiplier.

From the figure4, the inputs p=q=r=0 is given to circuits to produce the exact output. PMOS1 is on and NMOS1 is off. But the drain o PMOS1 is connected to the input p. so the p value (zero) is passed to the next stage. PMOS3 is on and NMOS3 is off. But the drain terminal of PMOS3 is connected to the P. So the carry output is zero. PMOS5 is on and NMOS5 is off. But the PMOS5 is connected to the input r. Hence the r value (zero) is passed to the output terminal for sum of the full adder circuit. Similarly, the inputs p=q=r=1 is given to circuits to produce the exact output. PMOS1 is off and NMOS1 is on. But the drain of NMOS1 is connected to the pbar (complement of p=0). So the pbar value (zero) is passed to the next stage. NMOS3 is on and PMOS3 is off. But the drain terminal of NMOS3 is connected to the r. So the carry output is one. PMOS5 is on and NMOS5 is off. But the PMOS5 is connected to the input r. Hence the r value (one) is passed to the output terminal to produce the sum output for one bit full adder. Likewise all other inputs combination are given to generate the exact sum and carry value for a compact full adder.

$$Sum = P \oplus Q \oplus R \quad (1)$$

$$Sum = (P \oplus Q) \oplus R \quad (2)$$

$$a \oplus b = \bar{a}b + a\bar{b} \qquad where\ a = (P \oplus Q)\ and\ b = R$$

by using this Boolean logic, equation (2) can be written as

$$Sum = (P \oplus Q)\bar{R} + \left(\overline{P \oplus Q}\right) R \quad (3)$$

Equation (3) is the final expression to generate the sum of the one bit full adder circuits. The general carry generation formula is

$$Carry = PQ + QR + RP \quad (4)$$

The equation (4) can be simplified into equation (5) by using Boolean logic formula and De-margons theorem in order to reduce the number of transistor count. The equation (5) is the final formula to design the carry generation of a compact full adder with low die size and power.

$$Carry = \left(\overline{P \oplus Q}\right) P + (P \oplus Q) R \quad (5)$$

The equation (3) and equation (5) are used to generate the sum and carry of a compact full adder for adder and multipliers units. It consumes low power and less number of transistor counts. The reduced Wallace multiplier, booth multiplier and reduced carry select adder are incorporated into the modified unsymmetrical six parallel FIR filter.

IV. Existing ordinary six parallel FIR filter

Six filtering operation is carried out at the same time by using standard six parallel FIR filter. Hence it is called as ordinary six parallel FIR filter based on concurrent processing. Consequently, throughput is enhanced and processing delay is decreased when compared to sequential FIR filter. Since serial FIR filter gets N number of clock to produce the N number of coefficients.

Common equation of parallel FIR filter is defined by

$$\sum_{n=0}^{N-1} Y_n Z^{-n} = \sum_{n=0}^{N-1} X_n Z^{-n} \cdot \sum_{n=0}^{N-1} H_n Z^{-n} \quad (6)$$

Here N=6, from the equation (1), it's further simplified to get the values from Y_0 to Y_5. This is illustrated in the below equation.

$$Y_0 = X_0H_0 + X_1H_5Z^{-6} + X_2H_4Z^{-6} + X_3H_3Z^{-6} + X_4H_2Z^{-6} + X_5H_1Z^{-6} \quad (7)$$

$$Y_1 = X_0H_1 + X_1H_0 + X_2H_5Z^{-6} + X_3H_4Z^{-6} + X_4H_3Z^{-6} + X_5H_2Z^{-6} \quad (8)$$

$$Y_2 = X_0H_2 + X_1H_1 + X_2H_0 + X_3H_5Z^{-6} + X_4H_4Z^{-6} + X_5H_3Z^{-6} \quad (9)$$

$$Y_3 = X_0H_3 + X_1H_2 + X_2H_1 + X_3H_0 + X_4H_5Z^{-6} + X_5H_4Z^{-6} \quad (10)$$

$$Y_4 = X_0H_4 + X_1H_3 + X_2X_2 + X_3H_1 + X_4H_0 + X_5H_5Z^{-6} \quad (11)$$

$$Y_5 = X_0H_5 + X_1H_4 + X_2H_3 + X_3H_2 + X_4H_1 + X_5H_0 \quad (12)$$

Form these equations, regular six parallel FIR filters it's drawn to perform ordinary six parallel filter operation [4].

V. PROPOSED UNSYMMETRICAL SIX PARALLEL FIR FILTER

In the time-field symmetry means the frequency response has linear phase. Hence a FIR that is unsymmetrical in time domain will have non-linear phase in frequency field. In this paper, proposed an unsymmetrical six parallel FIR filter is designed by mixing of 2X2 FFA and 3X3 FFA architecture [10]. The purpose of mixing both 2x2 FFA and 3X3 FFA to reuse the repeated values of coefficients. By using the reusable concept, power and delay is reduced in the unsymmetrical six parallel FIR filter than the regular six parallel FIR filter. The equation (13 -18) is used to design the circuit of reconfigurable modified unsymmetrical six parallel FIR filter. Fast Fourier algorithm (FFA) is incorporated into the regular six parallel FIR filter to construct a proposed unsymmetrical six parallel FIR filter. Also the regular six parallel FIR filter needs more number of adder and multipliers [11]. To overcome this problem, the optimized unsymmetrical six parallel FIR filter with complexity reduced adder and Wallace multiplier circuits are applied to achieve the low area, delay and power than the regular six parallel FIR filter. Further to reduce the area and power, the booth multiplier will be applied into the enhanced unsymmetrical six parallel FIR filter with retiming technique.

$$Y_0 = H_0X_0 - Z^{-6}H_4X_4 + Z^{-6}[(H_2+H_4)(X_2+X_4) - H_2X_2] + \{(H_1+H_3+H_5)(X_1+X_3+X_5) - [(H_1+H_3)(X_1+X_3) - H_3X_3] - [(H_3+H_5)(X_3+X_5) - H_3X_3]\}Z^{-6} \quad (13)$$

$$Y_0 = H_0X_0 - Z^{-6}H_4X_4 + Z^{-6}[(H_2+H_4)(X_2+X_4) - H_2X_2] + \{(H_1+H_3+H_5)(X_1+X_3+X_5) - [(H_1+H_3)(X_1+X_3) - H_3X_3] - [(H_3+H_5)(X_3+X_5) - H_3X_3]\}Z^{-6} \quad (14)$$

$$Y_1 = (H_0+H_1)(X_0+X_1) - Z^{-6}(H_4+H_5)(X_4+X_5) + Z^{-6}[(H_2+H_3+H_4+H_5)(X_2+X_3+X_4+X_5) - (H_2+H_3)(X_2+X_3)] - (H_0X_0 - Z^{-6}H_4X_4 + Z^{-6}[(H_2+H_4)(X_2+X_4) - H_2X_2]) - (H_1X_1 - Z^{-6}H_5X_5 + Z^{-6}[(H_3+H_5)(X_3+X_5) - H_3X_3]) \quad (15)$$

$$Y_2 = [(H_0+H_2)(X_0+X_2) - H_2X_2] - (H_0X_0 - Z^{-6}H_4X_4) + (H_1X_1 - Z^{-6}H_5X_5 + Z^{-6}[(H_3+H_5)(X_3+X_5) - H_3X_3])$$

$$\begin{aligned} Y_3 = {} & [(H_0+H_1+H_2+H_3)(X_0+X_1+X_2+X_3) - (H_2+H_3)(X_2+X_3)] - (H_0+H_1)(X_0+X_1) \\ & - Z^{-6}(H_4+H_5)(X_4+X_5) - \{[(H_0+H_2)(X_0+X_2) - H_2X_2] - (H_0X_0 - Z^{-6}H_4X_4)\} \\ & - \{[(H_1+H_3)(X_1+X_3) - H_3X_3] - (H_1X_1 - Z^{-6}H_5X_5)\} \end{aligned} \quad (16)$$

$$Y_4 = (H_0+H_2+H_4)(X_0+X_2+X_4) - [(H_0+H_2)(X_0+X_2) - H_2X_2] - [(H_2+H_4)(X_2+X_4) - H_2X_2] + [(H_1+H_3)(X_1+X_3) - H_3X_3] - (H_1X_1 - Z^{-6}H_5X_5) \quad (17)$$

$$Y_5 = (H_0+H_1+H_2+H_3+H_4+H_5)(X_0+X_1+X_2+X_3+X_4+X_5) - [(H_0+H_1+H_2+H_3)(X_0+X_1+X_2+X_3) - (H_2+H_3)(X_2+X_3)] - [(H_2+H_3+H_4+H_5)(X_2+X_3+X_4+X_5) - (H_2+H_3)(X_2+X_3)] - \{(H_0+H_2+H_4)(X_0+X_2+X_4) - [(H_0+H_2)(X_0+X_2) - H_2X_2]\} - \{(H_1+H_3+H_5)(X_1+X_3+X_5) - [(H_1+H_3)(X_1+X_3) - H_3X_3] - [(H_3+H_5)(X_3+X_5) - H_3X_3]\} \quad (18)$$

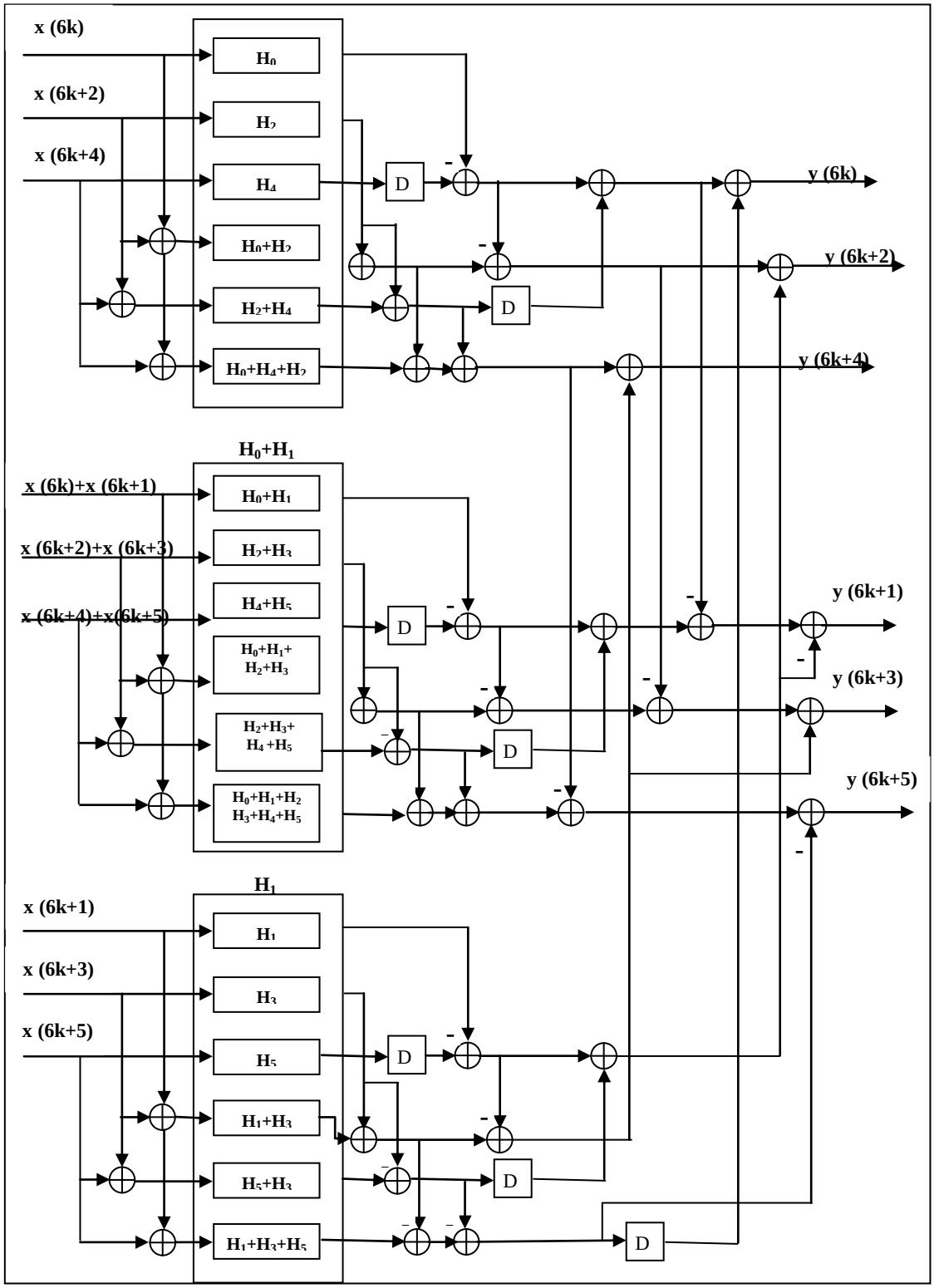

Fig.5. Implementation of modified unsymmetrical six-parallel FIR filters using FFA.

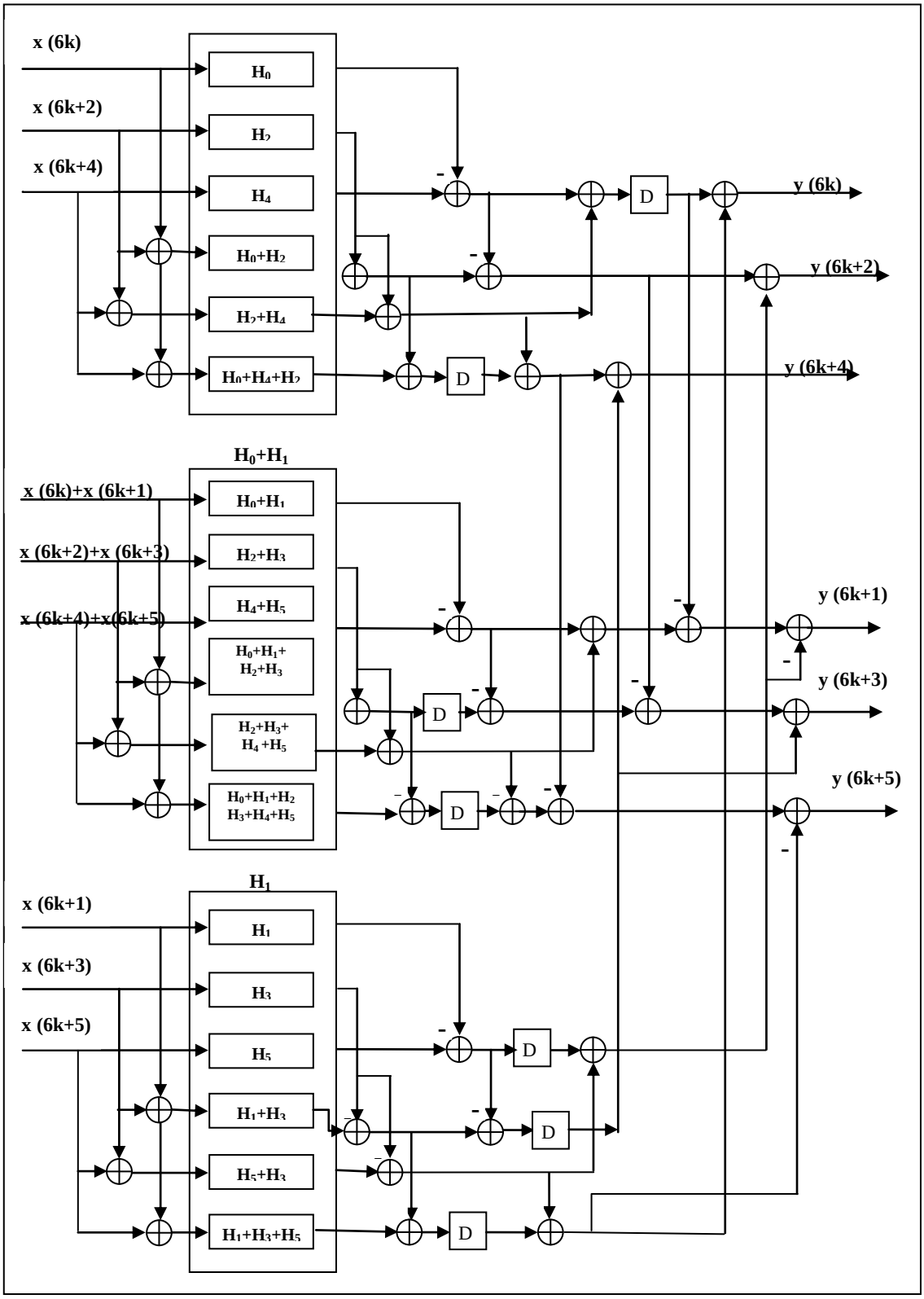

Fig.6. Circuit diagram of enhanced unsymmetrical six parallel FIR filter with retiming technique

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The modified unsymmetrical six parallel FIR filter is designed by using reduced booth multiplier, carry select adder and retiming technique to achieve the low area and low power consumption. Retiming technique is nothing but altering the location or place of the register (D-flip-flop) in order to achieve the low power and high speed utilization as shown in fig.6. The register is placed in an optimized place. Unwanted register is removed to achieve low area and reduce the clock period to achieve the output very quickly [12] and [13]. Retiming is mainly used to reduce the critical path by reducing delay elements, and relocate the pipelined register (D) as shown in fig.6 when compared to fig.5.

VI. RESULTS & DISCUSSION

In this paper, a compact XOR gate, full adder is designed to incorporate into the adder and multipliers circuits. The boolean logic based optimized carry select adder is constructed by using reduced half adder, AND, OR, XOR gates based on improved GDI logic. Gate diffusion input (GDI) logic is mainly used to reduce the number of transistor and power by giving the input into source, gate and drain of MOSFET transistors instead of gate terminal only. So the number of transistor is reduced, which leads to the low power consumption. Improved GDI logic is worked based on logical reduction in the circuit level. Logical reduction is done by using boolean logic or karnaugh map to simply the corresponding circuit. The transistor level simulation is performed by using analog cadence virtuoso.

The simulation output of a reduced XOR gate is checked to verify the functionality. Initially, the input p and q are 1. So the output is zero; the second clock cycle the inputs p=1 and q=0, hence the output of a reduced XOR gate is one. In the third clock cycle, the inputs p=0 and q=1, the corresponding output is one. Finally, the inputs p=0 and q=0, then the output of a compact XOR gate is zero. Likewise, the inputs are processed to generate the accurate outputs.

Table 1
Comparison between different carry select adders circuits by using different gates structure

Adder Types	Existing CSLA	CSLA using GDI logic	Proposed CSLA using improved GDI logic
	Number of transistors	Number of transistors	Number of transistors
8-bit	510	260	252
Half adder	18	6	6
Full adder	28	16	10
XOR	12	4	3
AND	6	4	4
OR	6	4	4

From the table.1, it is illustrates that the proposed CSLA using improved GDI logic provides less number of transistors than the existing CSLA using static CMOS logic and reduced CSLA using GDI logic. The proposed CSLA with IGDI provides 3% area reduction than the existing GDI logic based CSLA and 50.58% area reduction than the existing static CMOS logic based CSLA.

The simulation output of a compact full adder is verified to check the functionality of full adder. We know that the inputs p=q=r=1 is given to the proposed full adder circuit. Hence the output sum=1 and carry=1. In the next clock cycle, p=q=1 and r=0, the sum is zero and corresponding carry output is one. Then the inputs p=q=0 and r=1 is given to produce the sum is one and carry is zero. Similarly, all other inputs are given to produce the exact output based on the truth table to check the functionality of full adder circuits.

Table 2
Existing and proposed CSLA power comparison

Types of full adder	Area (total number of transistors)	Power (uw)
Existing full adder	16	295
Compact full adder	10	116

The power consumption of existing and proposed carry select adder is measured based on 90nm nano technology. Similarly, the proposed CSLA provides 19.6% power reduction than the conventional CSLA with 90nm CMOS technology. The power results are obtained by using cadence tool. The schematic are designed in analog cadence tool. The functionality of the circuits is checked in digital cadence tool

Table 3
Comparison between existing and proposed full adder for power consumption

.

Types of full adder	Area (total number of transistors)	Power (uw)
Existing full adder	16	295
Compact full adder	10	116

The table.3 describe that the compact full adder needs only 10 transistors instead of 16 transistors to achieve low area utilization by using some logical reduction in the proposed full adder circuit. Hence, the reduced full adder consumes low power than the existing full adder. The reduced full adder circuits with modified GDI logic offers 37.5% area reduction 61% power reduction than the existing GDI logic based full adder. These reduced full adders are applied into the Wallace and booth multiplier to reduce the area and power.

The simulation output to test the functionality of booth multiplier is shown in fig.9. From the results, two input multiplier=-63 and multiplicand=-57 (negative multiplication) is given to multiplier circuits to produce the exact output as 3591, when the output done signal from the FSM is one and reset value is one. Active low reset is used. Likewise next inputs multiplier=63 and multiplicand=-121

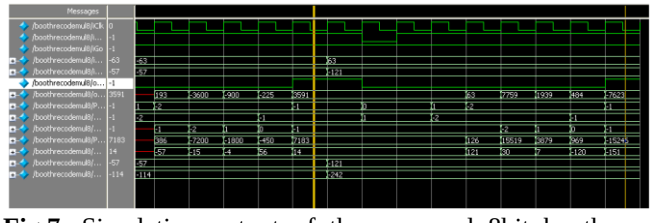

Fig.7. Simulation output of the proposed 8bit booth multiplier (signed multiplication) is set to give the value of -7623 as the output of 8bit booth multiplier.

Table 4
Comparison between existing and proposed 8-bit multiplier for ADP product using cadence tool

Types of multiplier	Slices(area)	Power (nw)	Delay(ps)
Existing Wallace multiplier	5349	348039.791	6914
Proposed Booth multiplier	4218	120553.207	3520

The table.4 illustrates the proposed booth multiplier needs only 36 slices instead of 85 slices to achieve low area utilization by using a reduced full adder circuit. Hence, the proposed booth multiplier consumes low area and power than the conventional Wallace multiplier. The proposed booth multiplier circuits with modified GDI logic based full adder offers 57.6% area reduction 12.7% power reduction than the existing Wallace multiplier. These multipliers are incorporated into the enhanced unsymmetrical six parallel FIR filter to reduce the area, delay and power.

Table 5
Comparison between existing and proposed six parallel FIR filter using cadence tool

Types of Parallel FIR filter	Slices(area)	Power (mw)	Delay(ps)
Existing six parallel FIR filter with Wallace multiplier	67027	1.852	8429
Proposed six parallel FIR filter with booth multiplier	20354	1.213	6927

From the table.5, it is shows that the proposed six parallel FIR filter with booth multiplier offers low area and low delay than the existing six parallel FIR filter with Wallace multiplier.

Table 6
Computation elements of proposed six parallel FIR filter over existing six parallel FIR filter

Method	Adder	DFF	FA	HA
Ordinary six parallel FIR filter	85	2754	2100	978
Modified six parallel FIR filter	66	2319	1802	756
Proposed six parallel FIR filter with retiming	30	522	155	496

From the table 6, the number of adder is reduced in the proposed six parallel FIR filter. Delay elements are reduced to achieve the low power. The number of half adder and full adder also reduced than the existing six parallel FIR filter.

VII. CONCLUSION

The parallel FIR filter is generally used for complex application in faster way. The design of a compact XOR gate and full adder are proposed to obtain the low area and low power consumption. This adder is applied into the carry select adder, reduced Wallace and booth multiplier circuits. Because the parallel FIR filter contains addition, multiplication and subtraction operations. Normally, the parallel FIR filter offers high speed by concurrent process. But the area and power is high due to adding the number of adder and multiplier units is more. To overcome this problem, the optimized adder and multiplier are used in the enhanced unsymmetrical six parallel FIR filter. The proposed carry select adder offers 58.8% APP (area and power product). Similarly, the reduced booth multiplier gave 35.17% area and power product. After that these adders and multiplier are applied into unsymmetrical six parallel FIR filter to achieve the speed, area and power by retiming technique and optimized adder and multiplier units. The proposed six parallel with retiming and booth multiplier offers 56.5% power delay product (PDP) reduction than the existing six parallel FIR filter.

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