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A 1GHz Cascaded CMOS Low Noise Block-Down Converter using 0.13µm CMOS Technology

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Abstract: ***Low Noise Block-down Converter is a crucial and an essential element in Radio Frequency receiver design. It magnifies the received weak Radio Frequency signal with minimum noise level. Designing Low Noise Block-down Converter with CMOS technology provides many advantages such as low power requirement, low cost and higher integration. This paper proposes the design of Low Noise Block-down Converter using 0.13µm CMOS technology. The proposed Low Noise Block-down Converter has two cascaded Common-Source (CS) stages. The cascaded stages provide high gain with less noise figure. A matching component called inter-stage inductor which is placed between the two stages of Block-down Converter. An inter-stage inductor can provide improved input return loss and gain due to careful optimization. By using the proposed topology Block-down Converter achieves maximum gain of 35.603 dB, input return loss of -27.690 dB, output return loss of -28.143 dB, reverse isolation of -41.211 dB, noise figure of 1.712 dB and stability factor of 1.216 is achieved at 1 GHz. The designed Low Noise Block-down Converter is simulated in ADS tool.***

Index Terms: - Low Noise Block-down Converter, Radio Frequency, 0.13µm CMOS technology, Antenna Design Software.

I. INTRODUCTION

Wireless systems encompass of a front-end and a back-end section. Analog signals are processed at the front-end section at the RF frequency range while analog and digital signals are processed at the back-end section at the baseband low frequency range. Radio frequency is the range of frequency in the electromagnetic spectrum typically from 100 KHz to 100 GHz that is used for radio communication [3].

With the faster development of high-performance wireless communication systems, the demand for portable wireless communication systems to provide greater performance, high packing density and low-cost radio frequency (RF) receiver that has considerably grown in consumer electronics market [4].

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The received radio frequency signal strength by the receiving antenna is very weak. For making this received signal is suitable for further processing, the system needs an amplifier which should have high gain and good noise performance [3]. Such an amplifier is referred to as Low Noise Block-down Converter. The main requirement of Low Noise Amplifier is low noise figure and high gain. All battery-powered communication systems work with Low Noise Block-down Converter since it has low power consumption. The performance of the Low Noise Block-down Converter is evaluated in terms of gain, noise figure, stability and linearity [12]. In the past, instead of using CMOS technology, GaAs pHEMT and mHEMT technologies were used. Due to the *advantages* of less cost and high packing density, CMOS technology is widely used in Low Noise Block-down Converter design. In earlier days 0.35 µm CMOS and 0.18 µm CMOS technologies were used. Due to the resulting advantages of reduced chip size, 0.13 µm technology is used nowadays. It covers the frequency range of many popular wireless products such as Cell phones, GPS and Bluetooth.

The complete design of Low Noise Amplifier consists of three main sections, namely Main transistor section, Input matching network and the Output matching network [5]. The first step in designing LNA is the selection of Transistor. The selected transistor must achieve high gain, low noise figure and high IIP3 Performance. The input matching and output matching network is used to increase the power transfer and to reduce the reflections.

For narrowband block-down converter, the common-source topology is the popular architecture [1]. It is very attractive approach due to improved noise performance, good reverse isolation and high gain [6]. The main advantage of inductive degeneration common-source topology is that it consumes less amount of power. Only one disadvantage is that poor isolation. So, to overcome such limitation, cascade inductive source degeneration topology is used. The cascade inductive degeneration also provides higher gain with low noise figure. Chang et al. proposed a Low Noise Block-down Converter design in [3]. In the main circuit, additionally add one inductor at the drain terminal, by which to reduce noise level present in the circuit [1]. It also uses source degeneration inductor for impedance matching and also for good noise performance.

This method exhibits gain of 8.4 dB and noise figure of 1.92 dB. In [1] common-source topology is used to achieve high gain, low noise figure and low power consumption [11]. any approaches to reduce noise performance of low noise block-down converter is also presented in this paper.

A technique for reducing the noise of a Complementary Metal Oxide Semiconductor low noise block-down converter by inserting a capacitance parallel to the transistor [7]. Self Forward Body Bias (SFBB) technique is proposed to reduce supply voltage in. This low noise block-down converter is implemented in 0.18 µm CMOS technology. This method achieves gain 16 dB and noise figure of 2.65 dB.

Po-Yu Chung et al. [3] have stated that the low noise block-down converter is composed of four cascaded stages. Gate source transformer feedback technique is used at the input which is used for both noise and input impedance matching. Gate Drain transformer feedback is used for other stages to achieve inter-stage and output matching.

Chen-ming et al. [8] discuss seven different noise optimization techniques for inductively degenerated cascode Complementary Metal Oxide Semiconductor low noise block-down converter. From the seven techniques five noise optimization techniques are used for power match. A new input matching topology is proposed in. The input matching design is based on capacitive feedback with π matching network. It achieves gain of 21.7 dB and noise figure of 5 dB. Thus, a low noise block-down converter operated at 1 GHz is design in this paper [10]. This frequency lies in the IEEE L band. This band is suitable for GPS, Television Broadcast, Satellite Navigation applications [9][2].

II. PROPOSED METHOD

The configuration of the proposed low noise block-down converter is the two-stage cascade amplifier based on the design of single stage one. The first step in designing LNA is the selection of Transistor. The selected transistor must achieve high gain, low noise figure and high IIP3 Performance. BSIM (Berkeley Short-Channel IGFET Model) model version 3.3 is used in the proposed low noise block-down converter design for the CMOS transistor modeling. Matching Network design is an important concept in low noise block-down converter design. Matching Network is mainly used to increase power transfer and to reduce reflection. The matching networks can be designed by some methods such as using lumped components, stubs, quarter-wave transformer or transmission line. The proposed low noise block-down converter design uses T matching network by using lumped components for the matching network design.The circuit diagram for the proposed low noise block-down converter with inter-stage matching inductor is shown in Figure 1.

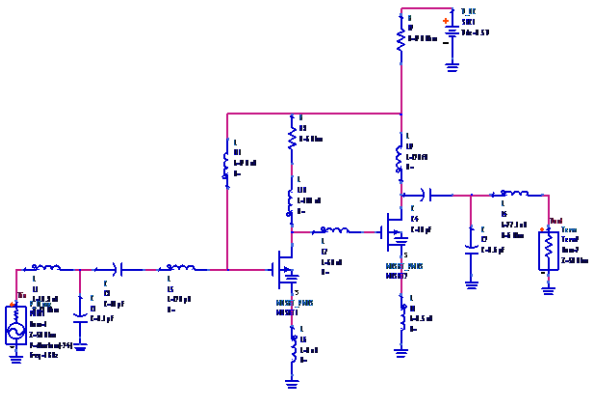

Fig. 1. Proposed LNA

In proposed circuit design, the inductively degenerated cascaded low noise amplifier topology can be used as a common source-common source (CS-CS) two stage low noise amplifier. To optimize low noise block- down converter design, appropriate technology must be chosen for low power and low voltage. The proposed low noise block-down converter uses inductive degeneration common source topology. Inductive negative feedback common source topology provides less power consumption but poor isolation and low gain, which are not considerable for better performance of the system. For this reason, cascade inductor source degeneration topology is used. For designing inductively degenerated CS-CS low noise amplifier, the optimum width of common source stage is calculated using the formula,

$$W_{opt1} = (\frac{2}{3} w_0 L C_{ox} R_s Q_s)^{-1} \quad (1)$$

The transistor unity gain frequency is obtained using,

$$w_T = \frac{g_m}{C_{gs}} \quad (2)$$

Where the gate to source capacitance is given by,

$$C_{gs} = \frac{2}{3} W_{opt1} L C_{ox} \quad (3)$$

Where C_{ox} is the oxide capacitance. w_0, L, R_S and Q_s are the operating frequency, gate length of the transistor, source resistance and optimum quality factor of the input circuit respectively.

The oxide capacitance C_{ox} is given as,

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$$C_{ox} = \left(\frac{\varepsilon_{ox}}{T_{ox}}\right) W_{opt} \qquad (4)$$

L_s is the source degeneration inductor. The source negative feedback inductor L_s is added for simultaneous noise and output matching between the source resistance R_s and the input transistor M_1. Usually the value of L_s is chosen as low. For the common source LNA the value of L_s is given as,

$$L_s = \frac{R_s C_{gs}}{g_m} \qquad (5)$$

L_g is the gate inductance. The inductance L_g should be large, then the circuit performance in terms of noise has been improved. The gate inductance is also used to set the resonant frequency. If the gate inductance L_g is increased quality factor of the input network will be high which leads to minimum noise figure. For the common source LNA the value of L_g is given as,

$$L_g = \frac{1}{w_0^2 C_{gs}} - L_s \qquad (6)$$

The proposed low noise block-down converter relies on the use of inter-stage matching inductor between the two common source stages. By using these inter-stages matching inductor optimum noise figure, high gain and matching between two stage is achieved.

The coupling capacitor couples the RF input to the gate of the amplifier. The proposed low noise block-down converter also consists of resistive and inductive feedback, which is used to improve stability factor.

Usually the supply voltage should be selected as greater than twice of the threshold voltage. The power dissipation of the proposed low noise block-down converter is given as,

$$P_d = V_{dd} I_d \qquad (7)$$

III. RESULTS AND DISCUSSION

Advanced Design System designs and simulates the proposed LNA using TSMC 0.13 µm CMOS technology . The performance of the proposed system is evaluated by S-parameters such as gain (S_{21}), reverse isolation (S_{12}) and input/output return loss (S_{11}, S_{22}).

The ability of proposed LNA is evaluated by an important performance measure such as voltage gain. Voltage gain of LNA is measured by the following formula.

$$Gain = 20 \log\left(\frac{V_{out}}{V_{in}}\right) \qquad (8)$$

In this proposed LNA, the gain value is increased by inter-stage matching inductor L_m at low bias voltage and using the resistor. Figure 2 shows the voltage gain of proposed LNA.

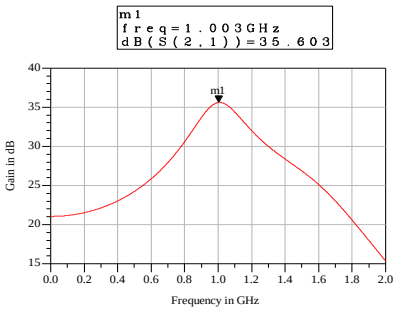

Fig. 2. Gain

The Input return loss a measure discontinuity in the transmission line while the input signal is propagating from source to load through it. If matching is good, it shows that the transmission line has minimum discontinuity.The input return loss is calculated using the formula,

$$RL(dB) = 10 \log 10\left(\frac{P_i}{P_r}\right) \qquad (9)$$

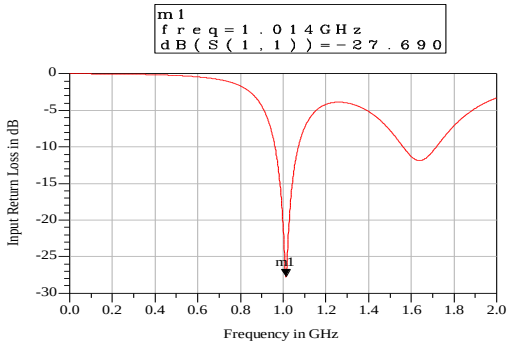

Fig. 3. Input Return Loss

Return losses are sometimes used as the negative value of the quantity, but this usage is, strictly speaking, incorrect based on the definition of loss.The input return loss is calculated with proper input impedance matching and it is shown in Fig. 3.

The Output Return Loss and input return loss has a similar definition, but output return loss applied to the output port. The output return loss of proposed LNA is shown in Fig. 4.

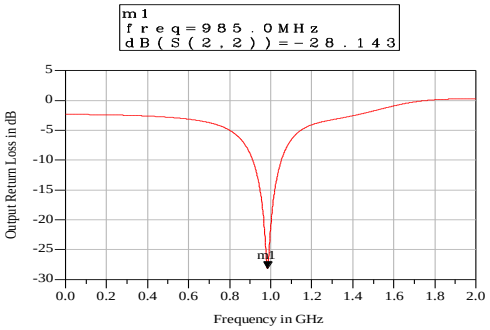

Fig. 4. Output Return Loss

Reverse Isolation define how well the signal at the input and output are isolated. Reverse isolation of the proposed LNA is shown in Fig. 5.

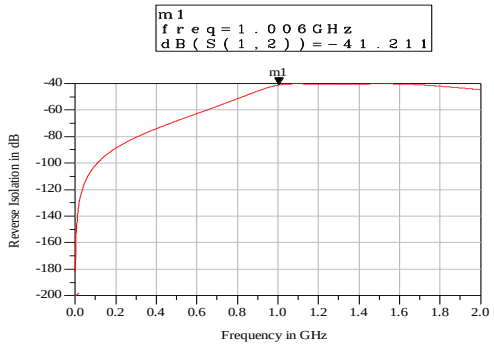

Fig.5. Reverse Isolation

The performance of proposed LNA is measured in terms of another important measure called Noise figure. Generally, the noise figure indicates how much amount of noise is introduced by the input source in the system and the same is available at the output of the system. Transistor small signal parameters are used here to calculate the noise figure of the proposed system. The achieved noise figure of the proposed LNA is shown in the Fig. 6.

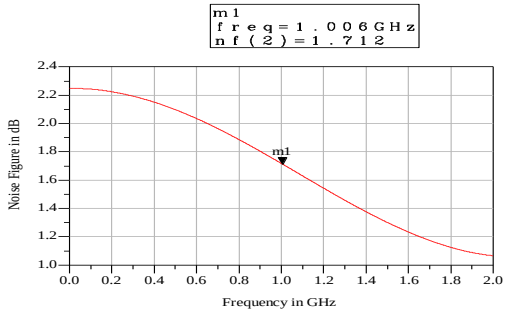

Fig. 6. Noise Figure

Stability is another important performance measure of LNA. The stability of a circuit is characterized by stern stability factor which is given as,

$$K=\frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} \qquad (10)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \qquad (11)$$

A circuit is unconditionally stable if,

$K>1$ and $|\Delta|<1$

The stability factor of the proposed LNA is shown in Fig. 7.

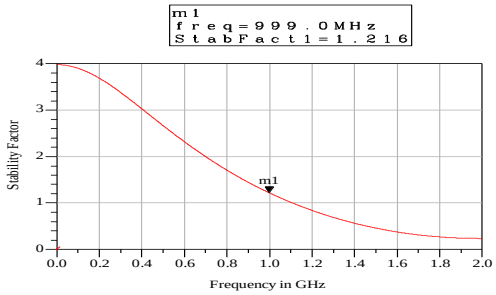

Fig. 7. Stability Factor

Table. 1. Summary of LNA Performance

Performance Parameter	**Value of proposed LNA**
Gain (S_{21} in dB)	35.603
Return Loss at Input (S_{11} in dB)	-27.690
Return Loss at Output (S_{22} in dB)	-28.143
Reverse Isolation (S_{12} in dB)	-41.211
Noise Figure (dB)	1.712
Stability Factor	1.216

The performance summary of the proposed Low noise amplifier is shown in Table. 1.

IV. CONCLUSION

A 1 GHz two stage Common Source low noise amplifier is designed and simulated using TSMC 0.13µm CMOS Technology in Advanced Design System. The proposed Low Noise Amplifier achieves high gain, low noise figure and good reverse isolation with low power consumption. The proposed design is useful for low power and Narrow band applications. The proposed Low Noise Amplifier has gain of 35.598 dB, input return loss of -27.690 dB, output return loss of -28.143 dB, reverse isolation of -40.763 dB, noise figure of 1.712 dB and Stability Factor of 1.203. Thus, the proposed LNA is useful for low power and Narrow Band Application.

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