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A Novel Two Fold Edge Activated Memory Cell with Low Power Dissipation and High Speed

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Abstract: ***In today's increasing demand of higher integration levels in VLSI and ULSI circuits' memory capacity and frequency of RAM is playing a major role in designing. Flip-flops are the micro cells for memories to store binary values. D flip-flops now days are used instead of any other because its designing is easy as far as area and power constraints are considered. So as to increase the bit rate of Flip-flop many triggering techniques were propose like single edge triggering and dual edge triggering. A novel D Flip-flop which uses only 14 transistors is explained using Two Fold Edge Triggering in this paper. From this paper we come to an understanding that at any temperature or at any supply voltage levels the proposed Flip-flop is efficient. Even though Power Delay product increases at lower voltage levels but still it is less compared to existing method. The input to output delay is greatly decreased as the number of transistors is reduced in dual data paths.***

Keywords: Memory Cell, Clock Efficiency, signal feed-back, Mentor Graphics.

I. INTRODUCTION

The increasing usage of High Speed devices need to limit static power dissipation and leakage current in Very Large Scale Integration (VLSI) chips. There was an incredible interest for different and quick upgrades in power effective designing during the ongoing years [1],[3]. The advanced IC plans embrace synchronous circuit procedures and utilize many flip-flop rich modules, for example, register, shift register and first-in first-out. In today's smart phones and electronic gadgets size of memory is the customer's first priority. Memories which use hard edge triggering with Flip-flop rich modules have non-negative setup time resulting in large data path delays. To increase usage of clock signal of any digital system dual edge pulse triggered flip-flops has been proposed. It reduces the compilation time from two clock cycles to one and is characterized by soft edge property [4]. A pulse triggered memory cell (Flip-Flop) is inbuilt with pulse generator and a bi-stable latch for storing binary values. The circuit complexity and number of stages inside these pulse triggered flip-flop are reduced for small D to Q delay. Pulse triggered flip-flop are broadly divided into two types Implicit Pulse triggered flip-flop and Explicit Pulse triggered flip-flop [5]. In implicit pulse triggered flip-flop the pulse generated inside the flip-flop. For example: data close-to-output, Hybrid Latch flip-flop (HLFF)[2], Semi dynamic Flip-Flop (SFF).

In Explicit pulse activated flip-flop (E p-ff), the pulse is produced remotely with the goal that all the neighboring flip-flops can share. A portion of the systems like Explicit Pulse Triggered Data Close to Output (EP DCO), static Conditional Discharge flip-flop (S-CDFF)[10] are the fundamental plan methods. This check appropriation helps in disseminating the intensity of the pulse generator crosswise over numerous Explicit pulse activated flip-flop. A framework utilizing express pulse activated flip-flop will be increasingly productive as far as area and power are concerned than a framework utilizing implicit pulse activated flip-flop. It is easy to implement Dual-Edge Triggering (DET) in Explicit Pulse Triggered flip-flop when compared to Implicit Pulse Triggering. Both in clock appropriation system and flip-flop power utilization is decreased utilizing DET. Regardless of whether we utilize a large portion of the recurrence, we can keep up a similar throughput of unique framework. Simulations are finished utilizing Mentor Graphics software and results are compared with double edge activating flip-flops.

II. EXISTING CIRCUITS

As Dual Data Rate VLSI circuits have come into existence many circuits were proposed in Two Fold Edge Triggered Flip-Flops. In order to increase Clock performance two edges of the Clock are used to trigger the Flip-Flops, this increases the clock frequency. Pulsed-based flip-flop is mainly for its soft-clock edge property, which allows time borrowing and reduces clock skew. It also provides superior latency and is capable of incorporating complex logic. Some of the recently proposed Two Fold Edge Triggered FF's are Explicit-Data Close to Output (EXDCO)[6]. It uses NAND-logic gates for clock generation; the power consumption of Clock Generator is less because transistor ON time for MN2 is less. But D to Q path of the Flip-Flop shows more delay as data has to pass through transistors MN1 and MN2 and clock signal has to on MN3 transistor. Node X in the circuit shows more discharge time which results in positive Set-up time. In order to avoid excess charge discharge at node X in EP-DCO DETFF a new circuit called Explicit Pulse Triggered Conditional Discharge Flip-Flop(EXCDFF) is proposed[7]. In this system just inverter is utilized to hold the estimated bit value of Node X. even though EXCDFF shows better performance when compared to EXDCO for node Q to change its value from 0 to 1 more number of transistors need to be switched which increases dynamic power dissipation. To reduce dynamic discharge of node X Static Conditional Discharge Flip-Flop (SCDFF) is proposed. It uses a static latch to avoid continuous discharge of node X [7].

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This static Latch however decreases dynamic power utilization but results in leakage and static power dissipation.

2.1 Improved Two Fold Edge Triggered Flip-Flop-1 (ITFETFF1)

In Improved Two Fold Edge Triggered FF shown in Fig:1 the upper data path is activated on '0' to '1' rising edge and lower information way is activated on '1' to '0' falling edge. In this memory cell an inverter and a PMOS transistor shapes a bi-stable component to hold the bit value. On the off chance that information bit is high the inverter changes the flag to low voltage this prompts PMOS transistor to dismantle the information up to high voltage. In the event that information is rationale '0' the inverter changes the flag to high which will segregate the information from VDD and keep the incentive to low voltage. The ITFET flip-flop performs to appear out just solid Logic-1 and does not give solid usefulness to Logic-0. Region and power is less when broke down with past strategies talked about in this paper.

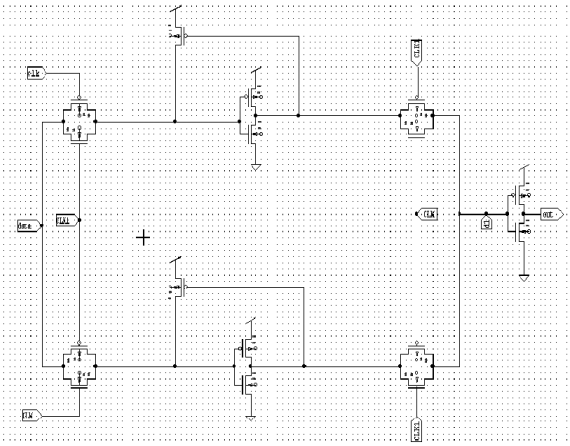

Fig1. ITFETFF1 memory-cell circuit diagram

2.2 Improved Two Fold Edge Triggered Flip-Flop-2(ITFETFF2)

IDETFF2 shown in Fig:2 is obtained just by replacing transmission gates of Clock input with n-MOS switches [8]. It has two data paths from D to Q shows master slave Flip-Flop features. As n-MOS transistor along with inverter is used as latch it stores both strong-‘0’ and strong-‘1’.The ITFETFF2 [9] flip-flop is free from edge voltage loss issues of pass transistor. By utilizing NMOS transistor in transmission gates .By supplanting the p-type pass transistor by n-type transistor we can diminish the area due to NMOS is smaller than PMOS transistor. It is remunerated that portability requirement of NMOS and PMOS. In this way recently altered two fold edge activated flip-flop is progressively proficient in region, power and speed when contrasted with past flip-flop.

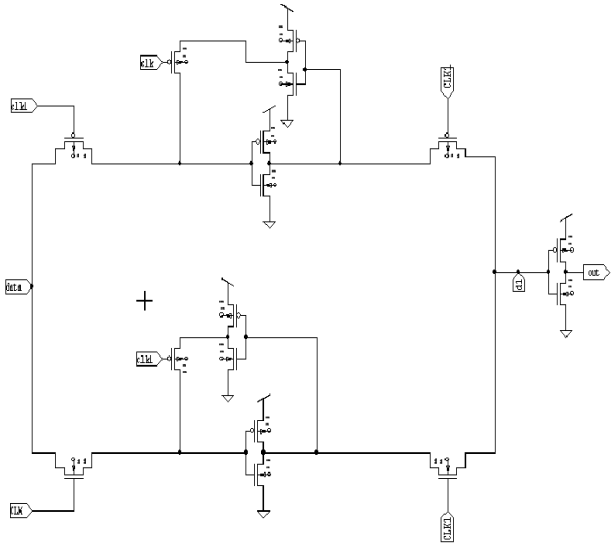

Fig2. ITFETFF-2 memory cell circuit diagram

III. PROPOSED 14T Two Fold Edge Triggered Flip-Flop(TFETFF)

14 Transistor Dual Edge Triggered Flip-Flop: In this paper a novel ITFETFF is proposed by modifying the 16T flip-flop, the two n-mos transistors connecting back to back inverters are removed. From the circuit we observe that, in the upper D to Qn path n-mos transistors switching for clkb used for the same read operation during positive edge, and bottom path clk signal switches n-mos connecting inverters for read operation. Since in a single path two transistors switch for the same edges of the clock for same operation n-mos transistors connecting back to back inverters are removed. This reduces the transistor count to 14 and the circuit diagram is shown in Fig:3.

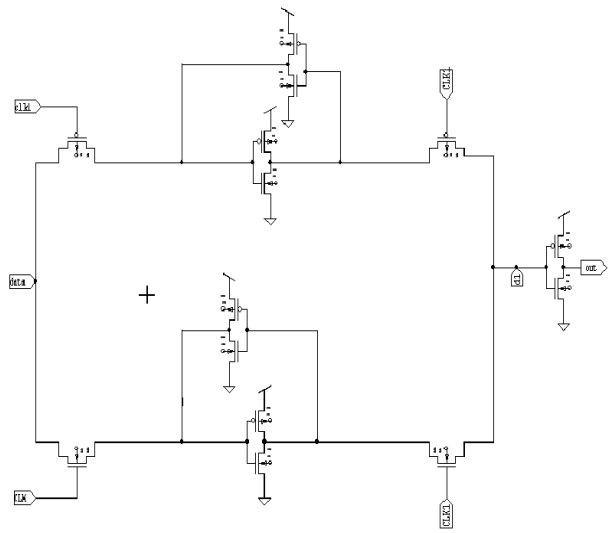

Fig3: Circuit Diagram of Novel 14T Flip-Flop

IV. RESULTS

Power area and delay are calculated and the proposed technique is compared both with explicit single and Dual edge triggered flip-flops. All the circuit simulations and calculations are done using Mentor Graphics 130nm technology.

Dynamic power, Static Power and Leakage Power are calculated for all mixes of Clock and Data inputs . Comparisons are done in terms of area (number of transistors), Delay and Power.

4.1 Observations

The following graph shows the area and Static Power comparison between previous techniques with the proposed ITFETFF. Static power is calculated by giving continuous 0's and continuous 1's for 10 clock cycles. Dynamic power dissipation is calculated by giving varying 0's and 1's as D-input for 5-bit,10-bit and 15-bit of data ITFETFF1, ITFETFF2 and novel 14T Two Fold Edge Triggered FF .

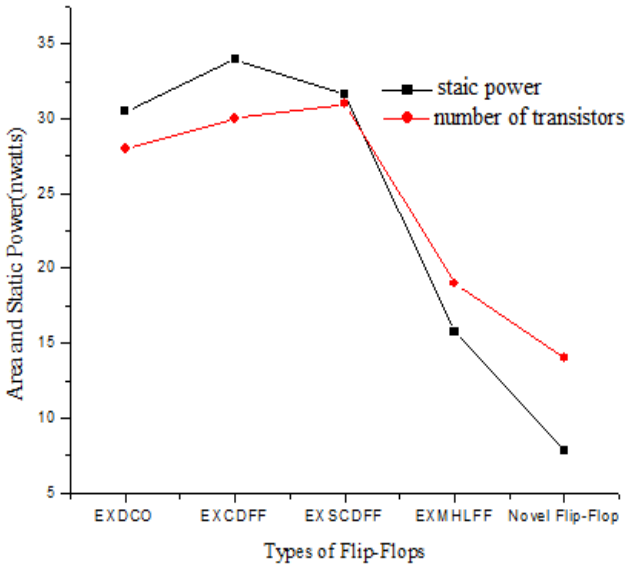

Fig4:Area and static power comparison of previous and present techniques

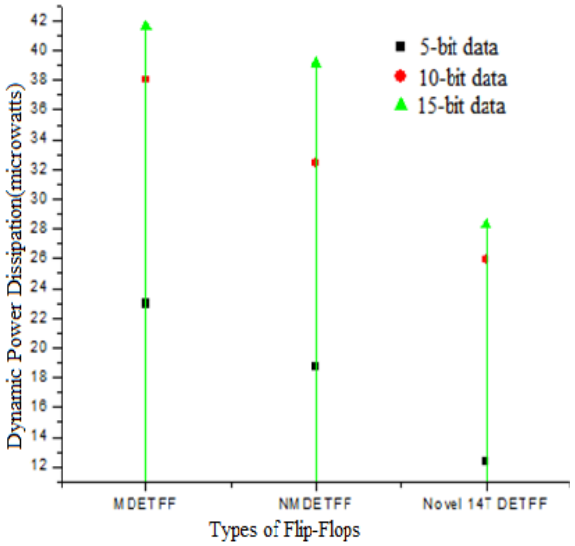

Fig5: Dynamic Power Dissipation comparison for multi bits

The following graph shows the plot between varying supply voltage verses power delay product. For ITFETFF2 and Novel 14T TFETFF. The voltage values are varied by keeping temperature constant.

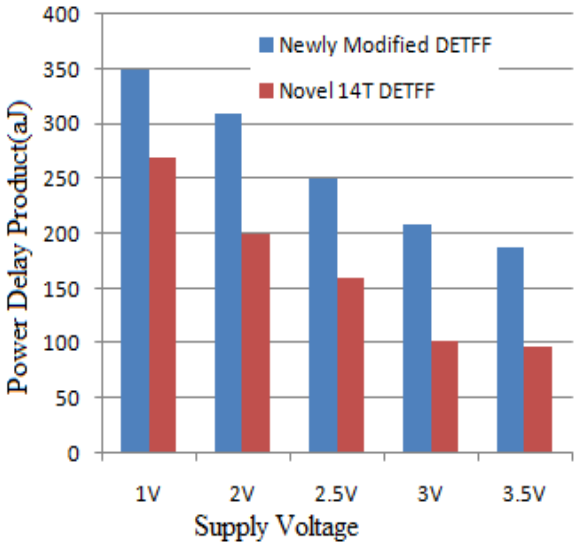

Fig6:PDP comparison between Newly Modified DETFF and Novel 14T DETFF

At a fixed voltage of 3.5V leakage currents are calculated for DETFF, MDETFF, Newly MDETFF, and Novel 14T DETFF at different temperatures.

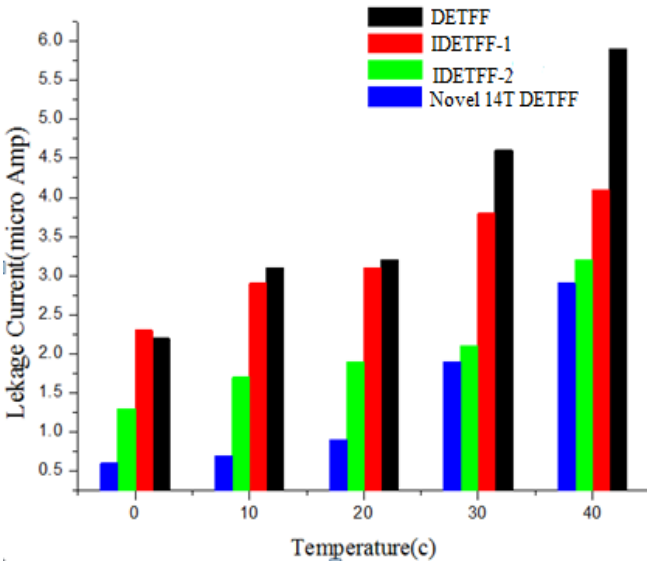

Fig7: Leakage Current comparison at different temperatures

Table1: Leakage Power Calculation of DETFF

Flip-flop Designs	Two Fold Edge Triggered memory cell (Power in µwatts)	Improved Two Fold Edge Triggered memory cell (IDETFF1) (Power in µwatts)	Improved Two Fold Edge Triggered memory cell (IDETFF2) (Power in µwatts)	Novel 14T memory cell (Power in µwatts)
(CLK, Data)= (0 , 0)	5.12	5.5	6.9	3.98
(CLK, Data)= (0 , 1)	3.21	1.55	4.45	2.64
(CLK, Data)= (1 , 0)	1.34	5.5	11.56	6.474
(CLK, Data)= (1 , 1)	3.05	1.55	11.6	4.39

Table2: D-to-Q delay of DET Flip-Flops

Flip-flop Designs	Two Fold Edge Triggered memory cell D-to-Q Delay(nano sec)	Improved Two Fold Edge Triggered memory cell-1 D-to-Q Delay (nanosec)	Improved Two Fold Edge Triggered memorycell-2 D-to-Q Delay(nano sec)	Novel Flip-Flop D-to-Q Delay(nano sec)
(CLK, Data)= (0 ,00)	156.74	109.49	96.21	74.63
(CLK, Data)= (0 ,01)	203.5	198.4	143.2	98.4
(CLK, Data)= (1 ,10)	144.31	167.4	113.4	87.5
(CLK, Data)= (1 ,11)	198.67	137.1	95.6	94.3

V.CONCLUSION

In Two Fold Edge Triggered Flip-Flops, clock frequency has doubled. The delay of the memory cell is diminished by removing the transistors in the latch. The data path delay in both the paths of the circuit is much less when compared with existing Dual-Edge Triggered Flip-Flops. The Novel 14T D Flip-Flop is efficient in terms of area, delay and power. In order to reduce area and extra switching activity, we removed two transistors in the latch. This reduced data path delay to a greater extent.

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