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Hardware-Efficient Decimation Filter Design of Zero-IF Receiver for Wireless Network

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Abstract: ***The digital scheme realized in this work emphasize on hardware-efficient decimation filter implementation along with their use in the processing of the digitized baseband signal of Zero-Intermediate Frequency (IF) Receiver. This technique allows quick selection of filter coefficients which will yield minimum error in the frequency response characteristics with less hardware complexity in terms of the number of hardware components, especially adders. The overall decimation filter is designed for Digital European Cordless Telephone (DECT) standard specifications. The performance of the entire system is analyzed by counting the number of adders used for each filter coefficient. In this simulation, it is proved that this type of design requires only 15 adders, which is less than 14.2% for droop correction filter and 40% for the Half-band filter.***

Index Terms:. Decimation, Digital filter, Half-band filter, Sigma–Delta conversion, Wireless Communications.

I. INTRODUCTION

Today most receivers are usually prepared in a single chip. Nevertheless, extensive growth of wireless communication systems results in rapidly changing standards, and the development of single-chip receivers [1] is particularly important in the recent years. The reasons for building such wireless communication receivers are low-cost and low-power requirements. Direct downconversion receivers are well suited in these surroundings as they further reduce the use of many external chip components by converting RF signals directly to baseband, consequently eliminating the need for bulky off-chip IF filters. Subsequently, all channel selections are performed at low frequency, digital low pass filter can be employed for better selectivity as well as for power efficiency. This digital technique meets the demands of low data rate applications such as DECT and Global System for Mobile (GSM) standards cellular telephones. Digital processing of baseband signals needs pre- and post-processing devices such as the Analog to Digital (A/D) and Digital to Analog (D/A) conversions. Oversampling converters such as sigma-delta A/D converters are used to achieve a high resolution which uses low-accuracy analog components. Then this signal can be fed to a decimation filter that realizes both filtering besides the out of band quantization noise cancellation. Additionally, digital lowpass filter must have sharp cutoff frequency constraints as the adjacent channel interference level is comparable to the signal level in mobile radio environment. This type of converter is currently employed in radio transceivers [3-4].

The complete multistage decimation filter structure for GSM and DECT standard transceivers is presented by C. J. Barrett in [5]. In his work, it was shown that entire structure basically consists of sigma-delta modulator, fifth order multiplier free comb filter, half-band frequency response filter sections and Finite Impulse Response (FIR) droop correction filter. They have improved the computational efficiency by reducing the numbers of operations per second. However, their schemes are implemented without considering the coefficient perturbations effect and without representing the coefficients in terms of sum of the signed power of two. Numerous methods of realization of downsampling filters for multi-standard transceivers are described by A. Ghazel *et al* [6]. It is proved for the minimum power consumptions by reducing unnecessary computations with the help of polyphase structure and simplifying multiplication by sequence of shift and add operations.

The easiest and most inexpensive filter to reduce the input sampling rate is a “Comb-Filter”, which can be realized without a multiplier due to the fact that the filter coefficients are all unity. The impulse response of that comb filter is identical to a rectangular window FIR filter. An important fact about comb filter is that it is not very efficient in eliminating the enhanced high-frequency out-of-band quantization noise generated by the Sigma-Delta modulators, and it is rarely used in practice without extra digital filters. Many applications are very sensitive to the increased magnitude drooping at the upper region of baseband spectral response of the comb filter. This suggests that the comb filter must be used in addition to one or more digital filter stages. The next stage is the Half-band FIR lowpass filter with symmetric coefficients to obtain a linear-phase response.

The half-band FIR filter is often designed so that the pass band attenuation is the complement of the stopband attenuation, thus implying that every even-indexed sample response is zero and also coefficients calculated to adjust the baseband frequency response to within +0.001dB of a unity magnitude frequency response. The last stage is simple droop correction FIR filter. The overall filter is designed to meet multi-standard GSM and DECT wireless standard [6-7]

The approach in this paper attempts to minimize the hardware requirements of the decimation filter. In that case, the problem is to find the filter coefficients to minimize the number of adders [8] for each filter coefficient.

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In a recent CMOS technology, the area utilization of an adder is not significant, but for some battery-operated systems such as cellular telephones and wireless networks, the power usage is of high importance. Therefore, designing filters having minimum number of adders is much needed. Sign digit code (SD code) is a useful representation of numbers, with three possible digits (1, -1 and 0) instead of (1, 0) as in the binary system. The SD representation often requires fewer non-zero digits resulting in a lower complexity for implementing multiplications. This new point of view towards low complexity implementation has evolved over three decades[9]. The idea was further developed by several authors [10]. The basic design methodologies are pattern based and graph based. The main disadvantage of these methods is their computational complexity. The major objective of this paper is to present an optimization algorithm that gives a fast solution by treating coefficient quantization effects in the frequency response and subexpression elimination problem separately for finding the optimum filter coefficients as against time consuming discrete optimization algorithm which does not always provide best solution.

A fourth-order oversampled A/D converter having a 6-bit data stream output is taken as example, with Over Sampling Ratios (OSR) specified by 64 (for GSM) and 32 (for DECT). It is possible to achieve 98 dB in case of GSM and 85 dB in case of DECT using these oversampling rates.

This paper is organized as follows. Section II concerned with zero-IF receiver. Filter design and its performance measures are explained in Section III. Emphasis on the hardware simplification is given in Section IV. Future developments and conclusions are provided in Section 5.

II.ZERO-IF RECEIVER CONSIDERATION

The most attractive Direct-Conversion Receivers (DCRs), which are known as zero-IF or homodyne receivers, Fig.1, are the best choice over classical heterodyne architecture and have gained importance in practice over the last decade. In DCRs, the desired RF spectrum is directly shifted back to the baseband by a Local Oscillator (LO) frequency which is exactly equal to the RF. With a trend toward low Q factor baseband filtering spurred by the advent of CMOS integrated chips, and consequently this receiver architecture permits the fabrication of analog and digital circuits on the same chip in contrast to the traditional bulky off-chip Surface Acoustic Wave (SAW) filter for IF separation. Another advantage of a DCR is that it can be used to eliminate the need of image filter to reject an undesired response to a spurious signal whose frequency is equal to twice the IF signal frequency. This advantage is offset, however, by the fact that a spurious local oscillator leakage in the radio frontend and DC offset are the serious problems for radio communication systems like GSM whose base band spectrum contains an important DC component. In order to utilize the full advantage of digital signal processing, digital channel selection using digital lowpass filters is retained for this work to accommodate the variable channel bandwidth. In digital signal processing, there is no limitation to use only a single sampling frequency throughout a system. It is essential that multiple sampling rates may be inevitable for some signal processing tasks or may be introduced intentionally to reduce the computational requirements.

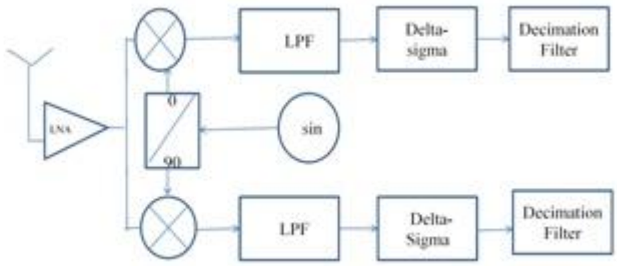

Figure 1. Homodyne Receiver

II.FILTER SPECIFICATIONS AND DESIGN

A cascaded multistage decimation filter structure for DCR receiver is shown in Fig.2. The filter can be realized in stages namely first stage by the comb filter, second stage by the Half-Band filter and the last stage by a droop correction FIR filter in which each stage performs part of filtering and is followed by downsampling. The requirements for a digital filter are normally specified in terms of normalized passband and stopband cutoff frequencies ω_p, ω_s and sampling frequency ω_{sa}. The permissible errors in the passband and in the stopband are δp and δs, respectively. To make it possible to approximate the desired function as close as possible, the specifications includes a transition band $\Delta\omega=\omega_s-\omega_p$

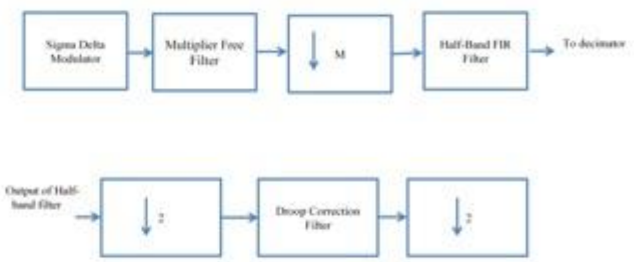

Figure 2. Multistage Decimation Filter Structure

A.Comb filter

Let us consider an L^{th} order sigma-delta modulator, which is cascaded with $K = L + 1$ comb filters whose transfer function is given in equation (1) to achieve zero quantization noise from the desired band. In the radio receiver application, L equals 4 corresponds to a fifth order comb filter and is considered with decimation ratio *M* of 8 for the DECT and M of 16 for the GSM. The sampling frequency *fsa* considered to be of 44800 kHz for DECT. The normalized magnitude response of comb filter shown is in Fig.

$$H(z) = \frac{1}{M^K}\left[\frac{1-z^{-M}}{1-z^{-1}}\right]^K \qquad (1)$$

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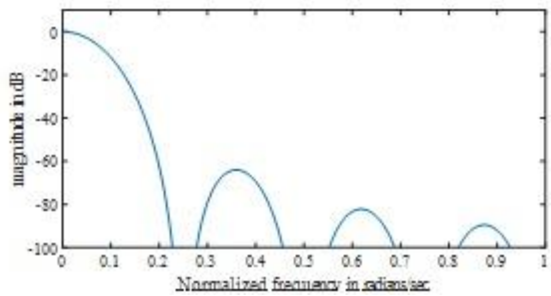

Figure 3. Comb Filter Magnitude Response

B. Half-Band filter

The channel pass-band frequency is set at f_p of 700 kHz and a sampling frequency f_{sa} of 2800 kHz for the DECT standard is used. The stop-band frequency *fs* is fixed by noting the symmetry to $f_{sa}/4$ (1400 kHz, −6 dB) of half-band filter. A 10 dB stop-band attenuation A_s is fixed to obtain a rejection of out-of band noise (−65 + A_{sx}) below received signal −73 dBm). Hence, the required filter attenuation A_{sx} is approximately to be -18 dB. Fig.4 shows the normalized magnitude response of Half-band filter

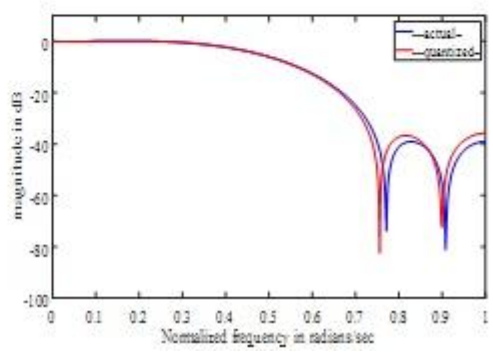

Figure 4. Half-Band Filter Magnitude Response

C. Droop correction filter Specification

For this filter, a pass-band frequency *fp* of 574 kHz which is equal to 82% of channel bandwidth and a sampling frequency of f_{sa} of 1400 kHz are considered for DECT standard. The transition band is from 574 to 700 kHz. According to blockers profiles, the stop-band attenuation *Asx* is calculated in order to obtain required Carrier to Noise Ratio (CNR). The CNR is defined by considering in-band signal power of −73 dBm with a frequency of 574 kHz. Hence the required stop band attenuation of the filter is to be -17dB.

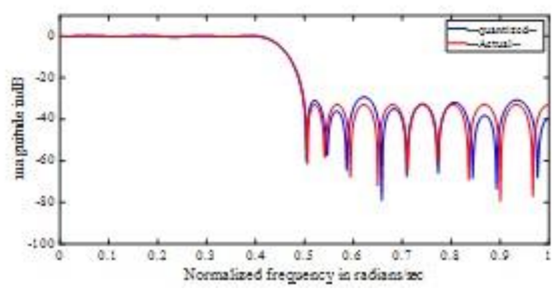

Figure 5. Droop correction Filter Magnitude Response

IV. FILTER OPTIMIZATION USING HEURISTIC METHOD

A heuristic method for designing the filters is to have low complexity coefficients, as measured by the total number of non-zeros digits in the binary or canonic signed digit (CSD) representations as used in this study. The CSD is an optimized signed digital code, which consists of the digits {-1, 0, 1}. The main property is no two consecutive digits are non-zero, which can successfully decrease the calculated shift operations and additions. Since coefficients of Comb filter are all one, it does not require quantization. This suggests a possible synthesis procedure in that a decimation filter can be constructed from a cascade of filter sections satisfying the minimum number of adders for each coefficient. The following are the design steps for the half-band filter

A.. Half-Band Filter

Step 1) The FIR half-band as shown in Fig. 2 is designed using the most efficient MPR algorithm described by D.J. Shpak *et al*. [13] for the specifications of ωp=0.25, ωs=0.75 and stop band attenuation of 41 dB. The filter is initially designed for 60dB, allowing a margin of 20 dB for quantization for filter coefficients.

Step 2) A list of 16 bits coefficients binary word with all possible combination is generated using a simple MATLAB program. Sixteen bits coefficients is divided in to slots, which corresponds to non-zero digits.

Table 1. Half-band Filter

Half-band filter coefficients Obtained through MPR Method from h (0) to h (6)	Quantized Coefficients	SHIFT/ ADD	No of Adders
-0.0506	-0.0547	$2^{-7}-2^{-4}$	1
0	0	0	0
0.2951	0.2966	$-2^{-12}+2^{-6}+2^{-5}+2^{-2}$	3
0.5000	0.5	2^{-1}	0
0.2951	0.2966	$2^{-12}+2^{-6}+2^{-5}+2^{-2}$	3
0	0	0	0
-0.0506	-0.0547	$2^{-7}-2^{-4}$	1

Step 3) If a magnitude function with rounded coefficients does not satisfy the tolerance scheme, it is possible to vary the coefficients by an optimization procedure. If the zeros of H (z) are tightly clustered, then their locations will be highly sensitive to quantization errors in the impulse response coefficients.

Step 4) It may be seen that number of adders to obtain each coefficient is reduced by expressing each filter coefficient in all possible sum of signed power of two combinations and selecting a one that has minimum number of ±1. For this reason, a slot of (16, 1) and a slot of (16, 2) are investigated because all of the non-quantized have magnitude less than or equal to 0.5.

Thus this step provides the coefficient that can be implemented with less number of adders. The quantized coefficients are shown in Table 1.

A count of adders to implement Half-band filter is 8. The normalized Half-band filter magnitude response is depicted in Fig.4

B.. Droop Correction Filter

The Droop correcting FIR filter equalizes the monotonic decrease in the pass band gain of Comb filter. Again, the filter is designed using MPR algorithm. Filter coefficients are quantized by the same procedure described in steps 1-4 for the stated FIR filter specifications. The normalized magnitude response is shown in Fig.5.

Table 2. Droop Correction Filter

FIR FILTERcoefficients from h (0) to h (17)	Quanti-zed coefficients	SHIFT/ADD	No of Adders
-0.0065	-0.0067	$2^{-14}+2^{-13}+2^{-10}-2^{-7}$	3
-0.0143	-0.0146	$2^{-14}-2^{-10}-2^{-9}+2^{-8}-2^{-6}$	4
0.0086	0.0085	$2^{-12}-2^{-10}-+2^{-7}-2^{-6}$	3
0.0103	0.0115	$-2^{-12}+2^{-8}+2^{-7}$	2
-0.0035	-0.0035	$-2^{-15-}2^{-14}+2^{-11}-2^{-8}$	3
-0.0173	-0.0171	$2^{-15}+2^{-11}-2^{-9}-2^{-6}$	3
-0.0002	-0.0002	$2^{-14}-2^{-12}$	1
0.0235	0.0234	$-2^{-7-}2^{-5}+2^{-4}$	2
0.0082	0.0081	$2^{-12}-2^{-7}+2^{-6}$	2
-0.03	-0.031	$2^{-12}-2^{-5}$	1
-0.0217	-0.0234	$2^{-15}+2^{-7}-2^{-5}$	2
0.036	0.0349	$-2^{-12}+2^{-8}+2^{-5}$	2
0.0451	0.0469	$2^{-6}-2^{-5}$	1
-0.0408	-0.0391	$-2^{-7}-2^{-5}$	1
-0.0943	-0.0953	$2^{-13}+2^{-12}-2^{-9}-2^{-5}-2^{-4}$	4
0.044	0.0469	$2^{-6}-2^{-5}$	1
0.3142	0.3134	$-2^{-14}+2^{-9}-2^{-4}+2^{-3}+2^{-2}$	4
0.4549	0.4551	$2^{-9}+2^{-6}-2^{-4}+2^{-1}$	3
0.3142	0.3134	$-2^{-14}+2^{-9}-2^{-4}+2^{-}+2^{-2}$	4

Table 3. Comparisons of the Hardware Components

Design	Filter Order	Adders for the coefficients	Total adders for filter
COMB	8	8	8
Half-Band	6	8	5
Droop correction Filter	35	47	35

Table 4. Comparison of Adder cost against Adder Depth

Filter	Algorithm	Adders/subtracts Cost		Adder Depth
		Before quantization	After quantization	
Half-band Filter 2	Hcub	3	3	3
	BHM	3	3	2
	RAG-n	3	3	2
Droop correction Filter 3	Hcub	18	15	3
	BHM	19	15	4

Table 5. Overall Comparison of Results

Filter	No of Adders in the Actual Design	No of Adders in Optimized Design	Adders Savings
Half-band	5	3	2
Droop correction	35	30	5

The desired and quantized symmetrical FIR filter coefficients from h (0) to h (17) are tabulated in Table 2. A count of adders to implement FIR filter coefficients is found to be 47. In real, however, all the coefficients are obtained using more number of adders, This approach allows one to select the coefficient in an easiest and fastest way which eventually reduces the time consuming discrete optimization method. With the advantage of reduced sampling rate, the designed filter gives the scope for low-power implementation, like in zero-IF receiver filter. The comparison for the filter design hardware components are shown in Table 3.

To validate the above procedure, series of experiments on the half-band filter and FIR coefficients using different algorithms such as Hcub [14], BHM [15] and RAG-n [12] were conducted and the adder/ subtractor costs against adder depth were measured. The results were tabulated in Table 4. Results show the performance improvement in terms of adder cost for quantized filter coefficients. From Table 4 it is observed that the proposed design requires 18 adders as against 21-22 adders by the same algorithms Hcub, BHM and RAG-n without co-efficient quantization. Table 5 provides the overall comparisons of results. It is noted that there is savings of 5 adders in the droop correction filter, whereas for the half-band it is 2.

V. CONCLUSION

In this paper, the objective is to present a simple and effective optimization algorithm for quick selection of decimation filter coefficients. Despite the simplicity of the approach used, the results presented in the previous section give reasonable guidelines for implementation. A systematic approach to obtain filter coefficients with less complexity is a time-consuming process. From the quantization point of view, the heuristic search method is beneficial. Due to the wide range of binary numbers used to represent each coefficient, one can easily select the coefficient based on number of adders needed. The quantization of filter coefficients begins with most inaccurate filter coefficient and ending with least inaccurate filter coefficients. This makes it easy to check the design with quantized coefficients meeting the specification. The hardware efficiency of the resulting decimation filter is observed by finding number of the adders in the filter. The proposed method takes less time to design and implement a digital filter and achieves percentage saving of adders 40 in Half-band filter stage and 14.1 in droop correction filter stage. The designed filter is aimed to meet the current radio communication standards specification while reducing the complexity. In addition to reduce number of add/subtract operations, effective implementations are achieved by considering the other performance metrics such as adder/subtracts cost and adder depth.

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