International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-8, Issue-1, May 2019

Analysis of Radhard Standard Cells using a Digital Processing Element Architecture as Test Bed

Siluveru Baktha Thukaram, Sneha Nandini Bolloju, Ameet Chavan

Abstract*: *Several methods have been proposed for the testing of Radhard cells by ground for commercial purposes. Here we build a design which tests the Radhard cells in a parallel architectural process which limits the power consumption and gains more speed. This paper gives an idea about the design of digital processing element and the testbed architecture to analyze any set of library cells (combinational and sequential logic gates), for the simple economical and easy to use to evaluate and validate any set of library cells. These cells will be validated in the Simulation Design Environment of Cadence using gpdk 90nm technology. The testbed architecture building blocks that are based on Radhard Cells will be evaluated for Functionality, Power Consumption, and Performance. The analysis of Radhard cells plays an important role to eradicate radiation effects. This method also increases the speed to test the of Radhard cells. In this, RDPP processor is used since power is a major factor in space. This RDPP processor reduces consumption of power in space and it helps the circuit to function for longer durations.

Index Terms*: *parallel architecture, digital processing element, Cadence, Radhard cells , RDPP processor

I. INTRODUCTION

For many years, various methods have been implemented to make different types of electronic circuits hardened to radiation effects in airspace applications and in defense military systems. The important factor of the system is Radiation tolerance. It is used for functioning of the electronic system and accuracy in their outputs [1].

The effects caused by Radiation are of mainly two types. They are cumulative effects and single event effects. If any CMOS circuit exposes for long duration to the Radiation it causes Cumulative effects. So these effects can be predictable since they expose for long time to the Radiation. These can be limited by taking the necessary steps and the another type of effects are Single Event Effects. Modern works in the field of integrated circuits mostly use sub-micron and deep micron technologies which are highly susceptible to the radiation effects most likely SEE effects (Single Event Effects), occurs when a spike of charged particle hits the sensitive volume of the Integrated Circuit. This charged particle when it hits changes the properties of the cell or the memory both combinational and sequential or even can damage the cell. These SEE effects are eccentric and can be considered only on the factual premise [2].

In this project, a digital processing element is going to be designed using the cadence tool. This processing element is used for the testing of any Radhard cells. In space, radiation effects cause most of the CMOS circuits are disturbed due to SEE effects. This processing element will test the Radhard cells so that the effect due to critical charge can be minimized.

To obtain this we analyze different types of Radhard cells using a digital processing element as testbed architecture. In space, the Power is available because of Batteries and it is also limited for a certain amount of time. So to minimize the Power usage and to run the application for longer durations we analyze the Radhard cells using RDPP Processor which consumes less power as it uses parallel processing for computations [3]. The motivation to choose RDPP processor rather than other methods like CPLD's (Complex Programmable Logic Devices), FPGA's (Field Programmable Logic Devices) since RDPP has fine-grained reconfigurable granularity which offers more flexibility whereas the other processors do not offer much flexibility and also for the logical purposes they consume very less amount of area and the remaining area is used for interconnects and for memory configuration [4].

The main part of the Reconfigurable Data Path Processor (RDPP) Architecture is the implementation of the Digital Processing element. RDPP has many applications, it is used for ultra-low power and radiation-tolerant processor in space applications. It consumes minimum power and gives maximum response i.e. high performance [5]. To avoid the disadvantages of FPGA's, new reconfigurable computing called PipeRench is used for Adaptive computing [6]. Using RDPP the author has developed a new chip called Image Signal multi-process (ISMP) which process 512x512 pixels at higher precision. It meets the execution rate up to 200 MOPS [7].

Revised Manuscript Received on 30 May 2019.
***** Correspondence Author
Siluveru Baktha Thukaram*, Electronics and Communication Engineering, Sreenidhi Institute of Science and Technology, Hyderabad, India.
Sneha Nandini Bolloju, Electronics and Communication Engineering, Sreenidhi Institute of Science and Technology, Hyderabad, India.
Dr. Ameet Chavan, Electronics and Communication Engineering, Sreenidhi Institute of Science and Technology, Hyderabad, India.

This paper is divided into five different parts. They are I. Introduction II. Background of Invention III. Design Methodology IV. Results V. Applications of RDPP VI. Conclusion

II. BACKGROUND OF INVENTION

[1] given the comparison between the Radhard cell and the conventional standard cell. These Radhard cells standard library was developed using basic rules of TSMC CMOS process. These Radhard cells have many advantages in the areas of density, power consumption, and transient response compared to previous generations.

[3] executed a design library for ultra-low power and radiation-tolerant (ULP/RT) in light of AMI CMOS procedure to actualize RDPP design for space applications. In this RDPP architecture, the author altogether decreased the Dynamic Power Consumption and furthermore, he connected the Low Power structure methods to standard CMOS which limited the switching activity since switching impact causes irrelevant power cost. The author likewise executed parallel architecture for data transfer to maximize the speed of the application.

[5] described the ways to improve the spacecraft applications by using adaptive computing methods. Here he used the adaptive computing techniques to expel the software issues in Field Programmable Gate Array (FPGA) Architectures since they are difficult to design using present days software tools. They are slower than the custom designs, slow to set up and wastes much amount of silicon area. He also mentioned that Adaptive computing can be utilized to achieve better resources, faster configuration, partial configuration, and self-healing techniques, and also adaptive computing process can be further extended to analog and physical domains.

[6] worked on Reconfigurable computing technique which is a part of the adaptive computing technique. He stated that the Reconfigurable computing technique is the changing face of customer hardware design. As an example, he stated reconfigurable computing uses custom design rather than general purpose in IDEA implementations for a specific key at runtime so that this level yields huge enhancements in its execution. These can fill numerous needs in numerous applications, as they likely turned out to be regular off-the-rack parts, consequently lessens the expense. In the following ages, Reconfigurable computation technique plays a prominent role in computation devices. By using this technique, he implemented an attached processor called PipeRench. In this implementation, he limited the bandwidth between the PipeRench, the main memory, and the processor and further he expanded the speed of the processor.

[7] implemented an ISMP process which is a digital image signal multiprocessor. It is a previous version of the real-time image signal processor (RISP) used for gray-level image processing. ISMP processor works on the method of Reconfigurable data processor as it has the modules like main controller and four processor elements (PE's). In this ISMP processor, multichip processing is achieved using parallelism which enhanced the processing power. In Image Processing this ISMP can wind up compelling in future likewise as it has the necessary execution and exactness.

III. DESIGN METHODOLOGY

There are many methods in designing and analyzing Radhard cells. In this paper, Radhard cells are analyzed using the RDPP architecture. RDPP architecture consists of six processing elements (PE's). Each Processing element consists of different sub-modules like multiplexers, data registers, padding modules. multiplier, shifters, ALU, round and clip modules and other different types of modules. Out of all these ALU plays a prominent role as it occupies the maximum amount of area since most of the Processing elements work on different computations. In this paper, RDPP architecture is implemented to analyze the Radhard cells.

A. Implementation Technology:

RDPP architecture is used to implement any circuit in Ultra-Low Power and tolerant to radiation of CMOS circuits. In conventional CMOS circuits, dynamic power is used as the dominant source of energy consumption, it implies the power is dispersed when the device is switching, it differs with the square of the supply voltage. Here in this, the ULP program accomplishes power reduction in the order of two over conventional CMOS (3.3V) operating at very fewer voltages, i.e., ½ volt. In this technology, the Dynamic bias techniques are controlled from switching threshold activity and also affect in design parameters also occurs. In conventional CMOS dynamic power dispersal is constrained by lessening the amount of switching activity. This type of technique improves memory-escalated, "vertical" plans, with little parallelism furthermore, no squandered exchanging occasions. A standard way to deal with low power CMOS configuration is to kill unused modules by obstructing the signs to them; clock gating, or hindering the clock signs to unused pieces of the chip, is a typical model. The ULP/RT innovation tries to accomplish an equalization between switching power and static power. While dynamic control is essentially diminished, static power scattering, due to spillage in parasitic source and channel diodes, is proportionally more signifying. Static power dissipation is not dependent on the measure of switching movement, yet is relative to the source and channel zone, thus increments with the number of transistors in the circuit. To amplify the power reserve funds in the ULP technology, we maintain a strategic distance from plans consolidating expansive quantities of inactive transistors, for example, memories. Or maybe, we search for performance through parallelism in the information way and try to keep each transistor involved in this technology.

B. Digital Processing Element (PE)

The digital processing element within the RDPP architecture performs many arithmetic and logical computations, which can be categorized as linear arithmetic operations (ex: signed multiplication, subtraction, addition, etc...), non-linear-arithmetic operations (max or min value) and bit control operations.

This RDPP architecture has a wide variety of 24-bit external data path (PE_INT) and also some of its internal data paths are 48 bit wide (PE_LONG). In this Processing Element designed contains many sub-modules. Each sub-module performs many arithmetic and logical operations. They execute the following operations outlined as 48-bit Arithmetic and Logic Unit, 24 bit signed multiplier, Shifter operations, Round -Clip operations and Switching operations. In addition to this, it also performs Conditional-Multiplexing operations, the control signal for this CMUX is 9 bit long. Pad modules are provided to widen the bit length from 24 bit to the 48 bit to the MUX and AL_SHIFT modules and data registers functions as a memory unit. Additionally, the data within the sub-modules either 24 bit or the 48 bit is routed to the other sub-modules using the Multiplexers.

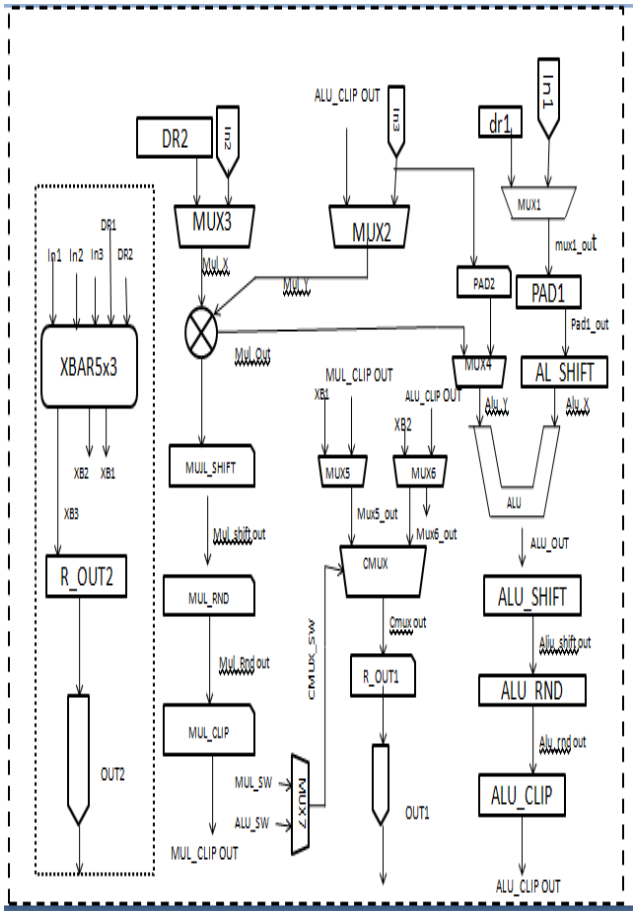

FIG 1: DIGITAL PROCESSING ELEMENT

C. RDPP Processor Architecture

The RDPP Architecture is designed based on the synchronized pipeline model which works on a different approach. In this RDPP Architecture, multiple Processing Elements are connected so that data flow and control information access between them. RDPP architecture performs conditional switching of data paths rather than conditional branching of data paths. So execution agility occurs through the conditional switching of data paths but not through the conditional branching of the execution path.

The figure shown below is an RDPP Architecture which consists of six Processing Elements (PE's), these are separated by the clock registers. In this RDPP architecture, the data transfer takes place from left to right. The Processing Elements PE2 and PE3 receive the same input data from PE1. The Processing Elements PE4 receive data from PE2 in a series way after a number of computations done on PE2 and PE4 also does a number of computations in it. Similarly, the Processing Element PE5 receives data from PE3 and PE6 receives data from PE5 in a series manner. Each Processing Element performs any number of different computations in it. The performance of this Architecture is high and its speed also increased as it contains a number of computations in it and these can be performed simultaneously at a time. A conditional switch which is focused in the architecture indicated by the question mark chooses which of the two outcomes i.e either from PE4 or from PE6 should pass through it on to the downstream. Thus, this RDPP architecture functions based on the concept of conditional switching of data paths but not through the conditional branching of data paths.

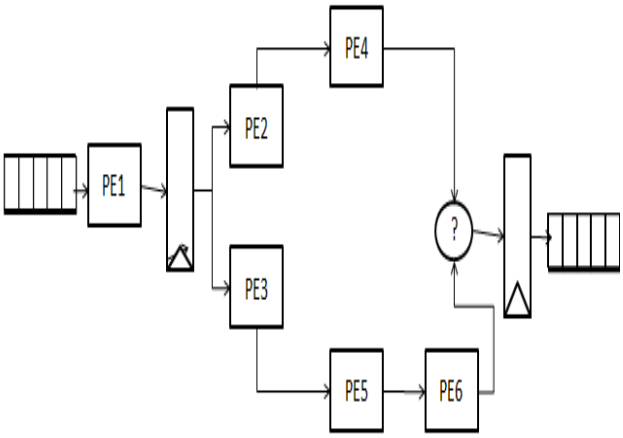

FIG2. RDPP ARCHITECTURE

IV. RESULTS

A. Simulation Results of Digital Processing Element

The simulation results of Processing Element (PE) is shown below. The PE is designed using the Verilog HDL (Hardware Description Language) code and it is implemented in the Cadence software using "NC launch" tool both at the code level and at the execution level. The technology used in this is gpdk 90nm.

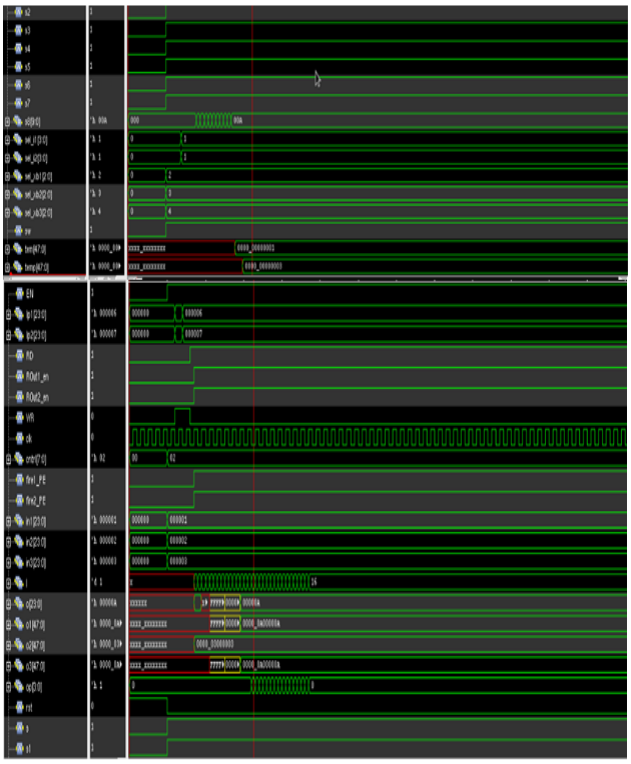

FIG3. SIMULATION RESULTS OF PE

B. Simulation Results of RDPP Architecture

The simulation results of RDPP Architecture is shown. This RDPP Architecture also designed using the Verilog HDL code and it is implemented in Cadence software using the NC launch tool at both the levels.

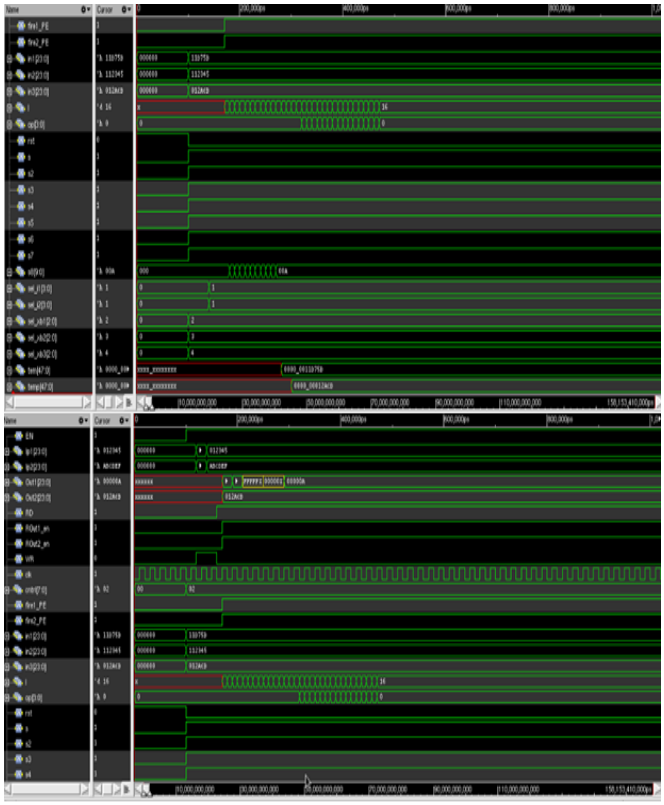

FIG4. SIMULATION RESULTS OF RDPP

C. Physical Design of RDPP

The Physical Design of RDPP Architecture is designed using the "Encounter" design in the Cadence tool. The technology used in developing the physical design is gpdk 90nm technology.

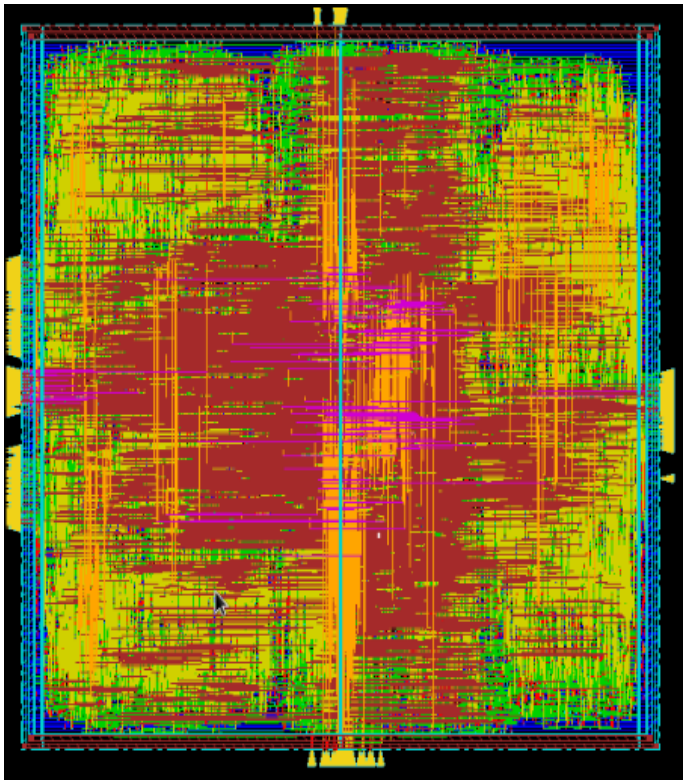

FIG5. PHYSICAL DESIGN OF RDPP

D. Calculation Results of RDPP

Name	Value
Technology	Gpdk 90nm
Power	22.6 mW
Cell Total Area	145032
Latency of PE	150 ns
Latency of RDPP	175 ns

TABLE1. RESULTS OF RDPP

V. APPLICATIONS OF RDPP

This RDPP Architecture can be utilized in an immense number of uses. It is reached out to numerous regions in the electronic science field. The fundamental feature of this RDPP Architecture is mostly used in airspace data-intensive spacecraft applications. In that a portion of the applications are recorded beneath: In Image Processing, it is utilized for pixel readout correction, spectral image data conversion. In Embedded systems it is utilized for article recognition and tracking. In the field of Communication systems, it is utilized in computerized channels like FIR filters.

VI. CONCLUSION

An Ultra Low Power, Radiation Tolerant (ULP/RT) design library has been implemented for space applications using RDPP Architecture based on AMI CMOS process. This RDPP Architecture delimited many challenge problems regarding the issues in software and hardware technologies. This RDPP Architecture is developed using the Verilog HDL modules and Radhard cell library is used in the RTL synthesis which is used for verification purpose and also for design alternatives. This design reduces many computational problems and consumes less power, achieves high speed and high performance. The design of Processing Element in this RDPP Architecture is additionally feasible, the data in regards to this Processing Element must be characterized alongside the interconnect plot, on-chip memory and the external interface. This ULP/RT technology changes the region of this low power structure. In this RDPP architecture, dynamic power utilization is altogether diminished. Low Power design methods are implemented to CMOS process circuits as there are no reproducible sources of power at space. This design technique seeks to minimize switching activity, provides less power reduction with ULP/RT. In this RDPP architecture switching activity conveys an immaterial power cost and this has exceptionally parallel structures dependent on conditional data transfer become more appealing. The RDPP is being created to eliminate the specific properties of the ULP/RT technology

REFERENCES

1. Diego Lunardini, Balaji Narasimham, Vishwa Ramachandran, Varadarajan Srinivasan, Ronald D.Schrimpf, and William H. Robinson Conference: 2004 Workshop on Radiation Effects on Components and Systems (RADECS 2004).
2. M. Benigni V. Liberali A. Stabile C. Calligaro "Design of Rad-Hard SRAM Cells: A Comparative Study" 27th International Conference on Microelectronics (MIEL2010) May 2010.
3. Donohoe et al., “Reconfigurable Data Path Processor for Space', Proceedings of the Military and AeroSpace Applications of Programmable Logic Devices 2000, Laurel, MD, Sep. 24–28, 2000.*
4. DeHon, André. "Reconfigurable Architectures for General-Purpose Computing", *Massachusetts Institute of Technology Artificial Intelligence Laboratory Report No. 1586*, sponsored under contract F30602-94-C-0252, October 1996.
5. Donohoe et al., “Adaptive Computing for Space', 42nd Midwest Symposium on Circuits and Systems, Aug. 8-11, 1999, vol. 1, pp. 126-129, IEEE.*.
6. Seth Copen Goldstein et al., “PipeRench: A Reconfigurable Architecture and Compiler, Apr. 2000 pp. 70-77.
7. Masakatsu Maruyama et al., “An Image Signal Multiprocessor on a Single Chip," IEEE Journal of Solid-State Circuits, vol. 25, No. 6, Dec. 1990, pp. 1476–1483.

AUTHORS PROFILE

Siluveru Baktha Thukaram is a PG scholar from sreenidhi institute of science and technology. He received B. Tech Degree from Electronics and Communication Engineering from JNTU Hyderabad in 2016. Presently he is pursuing M.Tech degree in digital systems and computer electronics from the same University. Currently he is working on analysis of radhard cells. His research interests include microelectronic circuit analysis and design, Challenges faced due to radiation in integrated circuits, specifically designing for security, Trusted computing in CMOS devices and modeling circuit-level soft errors.

Sneha Nandini Bolloju received her B.Tech (2016) in electrical and communication engineering from Sreyas Institute Of Engineering & Technology. and the M.Tech. (2019) in digital signals and computer engineering in digital systems and computer electronics from Sreenidhi Institute of Science and Technology. Hyderabad, India. She has also worked for Google Vendor in Hyderabad during the year (july 2016 – august 2017) after graduation and came back to pursue higher studies in 2017. Her research interests include microelectronic circuit analysis and design, Challenges faced in integrated circuits, specifically designing for security, Trusted computing in CMOS devices and modeling circuit-level soft errors.

Dr. Ameet Chavan has total 16 years of combined experience in industry and academia. Received his BE (Electronics) from Pune Univ., 1998, M.S. and Ph. D from University of Texas at El Paso (UTEP), USA in 2003 and 2010. Dr. Chavan worked as faculty for the ECE Department, UTEP, USA. Dr. Chavan has worked as a research engineer with Intel Corporation Inc., Advanced Micro Devices (AMD) Inc., and Echostar Technologies Ltd. He is presently working as Professor (ECE) and Dean (R&D) at the Sreenidhi Institute of Science and Technology, Hyderabad, INDIA