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Short Time Fourier Transform Implementation on FPGA

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Abstract*: Fourier transform gives us good localization of frequencies occurred in a signal. But the simultaneous time-frequency localization is a major problem in normal fourier transform. Also fourier transform fails in the case of non stationary signals and time invariant signals. As it only good in dealing frequency part, it is very poor in the context of time domain. This limitation of fourier transform has led to the new transform called as short time fourier transform(STFT) which can deal with both time and frequency domains simultaneously. STFT divides the signal in particular time intervals where we can find the non stationary signal as a stationary and can take the fourier transform for that interval by applying windowing technique.Short time fourier transform in image processing has many applications in medical fields,military purposes etc.The implementation of STFT is done by taking a image as input and the output transformed image is sent to the FPGA kit and the results were analysed using modelsim.Implementation on FPGA has many advantages as FPGA takes very few processing time and gives us accurate results when compared to DSPs.

***Index Terms*: Short Time Fourier Transform,FPGA,Image processing.**

I. INTRODUCTION

Now a days,most of the real time applications were based on the processing of signals either digital or analog especially digital.Due to its vast applications in the real time purposes the processing and anlaysing of the digital signal become necessary.Analysis of such digital data is very well performed by DSP(Digital Signal Processor).Now a days every video/audio is converted into digital form, the analysis of this digital signal is well performed by the DSP.It is a semiconductor device.These also includes the operations like Mathematical,modulation and amplification etc.These were performed to reduce the noise for the interaction and processing with other signals.Digital Signal Processor performs this operations very effectively and fastly.

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The features of DSP include that it is a 1Ghz device which can process upto 8000 million instructions per second.It supports embedded JTAG support via USB and have four 3.5mm audio jacks for microphones.It works with 5votls supply.While the other side FPGA is an integrated circuit which can be programmed at any time.FPGA comprises of CLBs(Combinational Logic Blocks) with programmable interconnects.The architecture of FPGA is different when compared to logical cells or PAL and CPLDs.CLB contains look up tables(LUTs).FPGA uses less power for processing the signals.The FPGA output voltage varies from 1.2v to 5v and current varies from mA to amperes.The user can program on on chip memory in FPGA.The FPGAs were manufactured by the different companies mainly by ALTERA,ACTEL,XILINX,LATTICE,ATMEL etc.These FPGAs were divided into families.They use different types of technologies like anti-fuse technology,flash technology etc.These devices have wide range of applications in aerospace and military applications.

A. FPGAs over DSPs:

Even though both FPGAs and DSPs have various adavnatges,FPGAs will take a edge over the DSPS in some aspects.FPGA devices are more flexible than the DSPs.Prallel architecture of a FPGA plays an important role in taking the edge over DSPs.Due to the parallel architecture power comsumption will be very low when compared to DSPs.Many DSPs based real time applications can be implemented through FPGA.Due to this advantages of FPGA ,STFT can be implemented on FPGA.The output wave transforms were analyzed in Cathode Ray Oscillioscope(CROs).

B. Short Time Fourier Transform(STFT):

At first,while studying about the short time fourier transform,basic knowledge of Discrete Fourier Transform(DFT) is needed.In DFT the signal is a total of sinusoidals.Hence the spectral resultant occurs over the total period of the time fails to identify when the spectral content occurs.Identification of spectral content is necessary for many of the limited or real time application signals.Short time fourier transform have overcome this limitation as it uses the windowing technique to identify the spectral content over the period of time.These windowing techniques helps in identifying the spectral content over the period of time.The STFT technique divides the input sinusoidal signal into small

blocks by multiplying with the window function.After applying the window, FFT(Fast Fourier Transfrom) operation is performed.Usage of window function decreases the loss of information.Different types of window functions were used for the STFT technique like rectangular window etc.

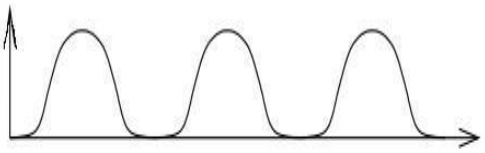

Fig 1: A window function

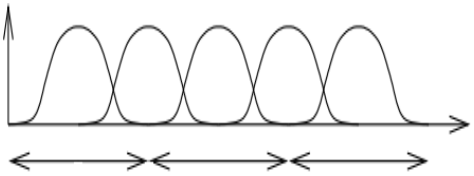

Fig 2: After overlapping using window function

The above images shows us the sinusoidal representation of an STFT singal after the overlapping with a window function.By the formation of the phase and magnitude time-frequency spectrums,analysis of both time and frequency spectrums becomes easier.

The time series short time fourier transform is defined as $X(n,\omega) = \sum_{t=-\infty}^{\infty} x(t)\omega(n-t)e^{-j\omega n}$.

In the above function ω represents the window function.The localization characteristics can be achieved by the window function.For better resolution in frequency domain long window and for better resolution in time domain short window were preffered.

II. RELATED WORK

K.R Liu [1] proposed a technique based on filter banks.This type of approach is widely used for implementation of STFT.The values were taken at each frequency independently.And this process is followed for all further frequencies.Although this technique is widely used it has certain limitations.Error rate is increasing at each and every frequency.This can be further corrected.Marrio garrido[2] proposes a feed forward technique for the implementation of STFT.This technique uses FFT.In this proposed architecture it reuses the STFT values for every time iteration hence it reduces the error rate and also reduces the hardware complexity.The hardware complexity and calculations can be further redcued. Shiqun zhang,Dunshan Yu,Shimin sheng[3] proposed a reduction of window calculations is the main goal of this architecture.It reduces the window calculations to N/2.The clock rate is 180Mhz.Even though it increases the clock rate,hardware is again a drawback.

K.Parhi and Manohar Ayinala[4] used welch method for the computation of power spectral density.Here N/2 FFT technique is used by 50% window overlapping.Their main goal is to reduce the power for computation upto certain extent.The power can be further reduced by using other techniques and error rate is high.

III. DESIGN IMPLEMENTATION

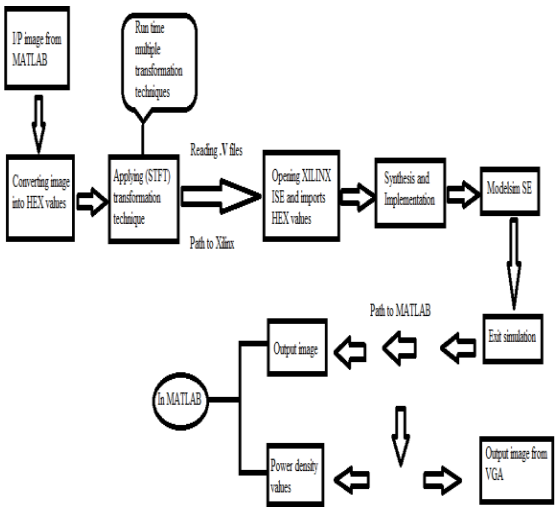

Fig 3: Design architecture of the proposed method

Since,images cannot be taken from Xilinx directly intially an input image is taken from matlab.The input image taken from matlab is converted into HEX values.The STFT is performed on HEX values later on.Path to Xilinx is provided from malab using specific matlab functions.The converted HEX values were imported to Xilinx.After the implementation and synthesis of the process,Modelsim software provides us the environment for hardware implementation of our code.FPGA implementation is perfomed on NEXYS2 board.The output image is generated to matlab and by using the power density values the output is analysed from VGA port.

Fig 4: An input image leena is given

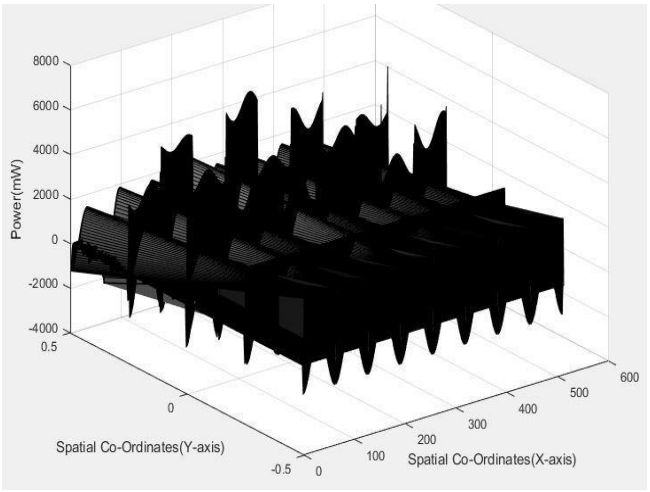

Fig 5: Transformed output image through Matlab

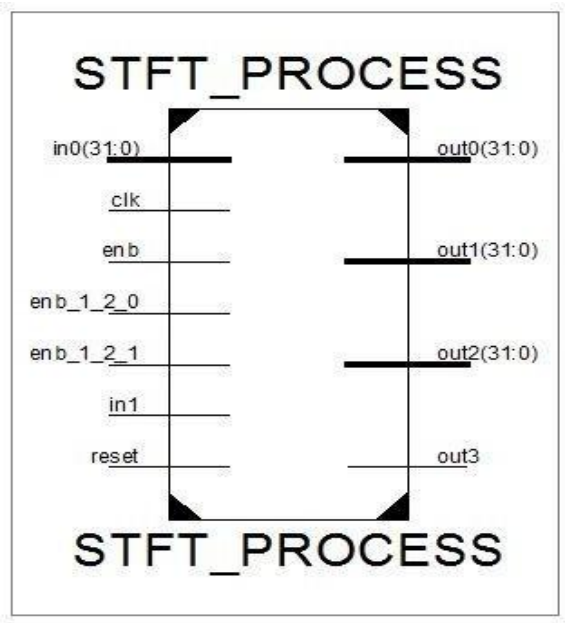

Fig 6:RTL schematic of STFT architecture

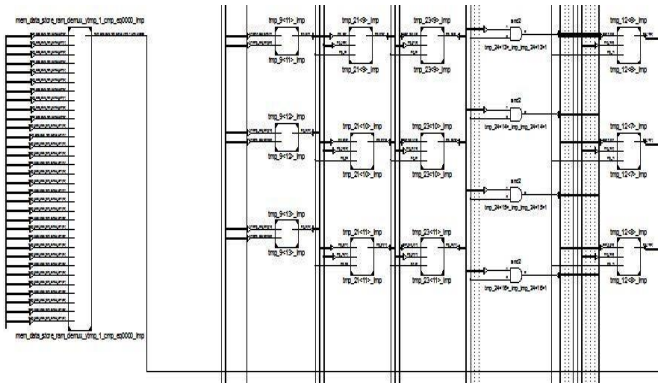

Fig 7: Sample part of architecture

IV. SIMULATION RESULTS AND DISCUSSIONS

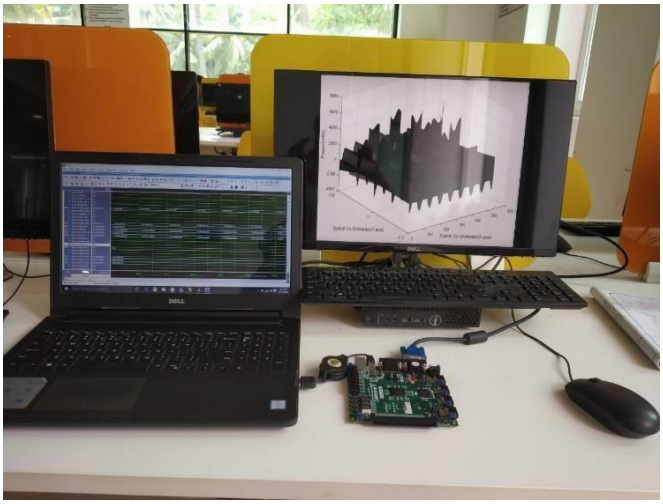

Fig 8: Hardware implementation of STFT using NEXYS 2 FPGA board

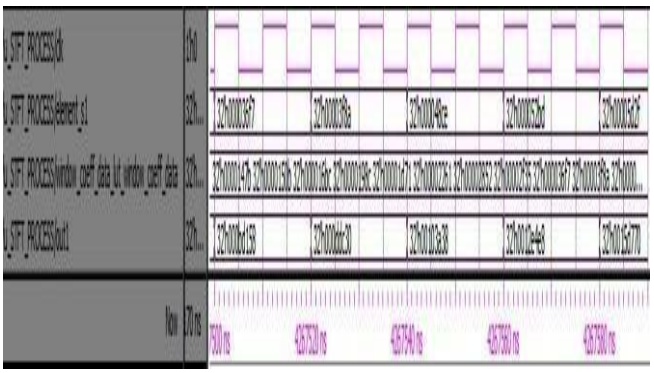

Fig 9:Xilinx results of STFT

V. DEVICE UTILIZATION

Logic utilization	NEXYS2FPGA	DSP kit
IOBS	135	174
Flip Flops	166	196
LUTs	284	368
Fan out	2.31	3.1
Power	2.1	3.3

Table 1: Comparision of device utilization between FPGA and DSP

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	271	18224	1%
Number of Slice LUTs	284	9112	3%
Number of fully used LUT-FF pairs	166	389	42%
Number of bonded IOBs	135	232	58%
Number of Block RAM/FIFO	1	32	3%
Number of BUFG/BUFGCTRLs	1	16	6%
Number of DSP48A1s	4	32	12%

Fig 10: Device utilization summary in Xilinx

VI. CONCLUSUON

The normal fourier transform gives only the frequency analysis of the signal.It is very poor in dealing with time domain.This limitation leads to new transformation called short time fourier transform which can gives us the simultaneous time and frequency analysis of the signal.The implementation of Short time fourier transform(STFT) is done by using Verilog coding.This design is very fast as it is using FPGAs over DSPs for real time applications.The execution is done using NEXYS2 FPGA kit and it is verified in matlab and Xilinx software.

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