

Design Analysis of Mutually Coupled Low Power UWB LNA using Noise Cancellation Technique

Manish Kumar, Vinay Kumar Deolia

Abstract: This paper comprises a design analysis of a low power (LP) Low noise amplifier(LNA) for UWB applications. Proposed LNA consists of two parallel path, one is the mutually coupled CS stage and second is CG path. The Mutually coupled path in the CS stage is beneficial for improving transconductance as well as input impedance matching. Since CS path provides high power gain and the CG path provides a wide bane matching. A noise cancellation technique is also used to reduce the noise of CG path, thus reducing the overall noise and increasing the gain in the UWB range. The proposed LNA successfully simulated in 90-nm CMOS technology. The results of proposed work indicate optimization(NF) at frequency 7.68 GHz with 3dB bandwidth of 1.4-7.8 GHz. All simulation has been done for a range of frequency 01-11 GHz in Cadence virtuoso software. The results quoted 2.72dB NF at frequency 7.686GHz, -16.389.1dB S_{11} , 12.87dB S_{21} , at frequency 4.8 GHz, maximum GP and GA is 10.26 dB,10.76dB at frequency 9.6GHz, with 1.2V, 1.96mW broad band LNA.

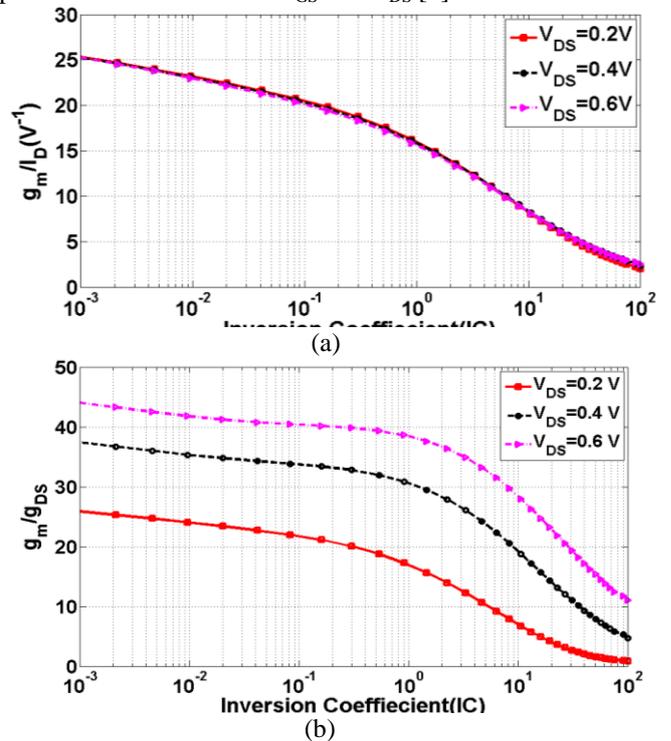
Index Terms: Low-noise Amplifier (LNA), Mutually Coupled Common Source (MCCS), Noise Figure (NF), Ultra Wide Band (UWB).

I. INTRODUCTION

In the span of a decade, the rapid development of wireless network applications is in demand in various fields such as medicine, agriculture, industrial settings and emerging fields such as IoT. The nature of these applications always requires low noise wideband modules, characterized by low power consumption and chip compactness. The functionality improves with each update version of CMOS technology file, however it causes a shiver impact on circuitry performance in terms of speed, bandwidth and use of existing topologies. It is therefore important to make a tradeoff between power consumption and other performance parameters below supply voltage (V_{DD})<0.6V [1]-[4].

In order to address these issues, variations in transconductance efficiency (TE), intrinsic voltage gain(g_m/g_{DS}), Transit frequency(f_t) and noise figure(NF) were shown in Figure.1(a), (b), (c), (d) for different value of V_{DS} with respect to the inversion coefficient(IC) = $\frac{I_D}{I_{D0}} = \ln^2(1 +$

$\frac{V_{GS}-V_{TH}}{2nUT}$), where $I_{D0} = 2n\mu_0c_{ox}U_T^2(\frac{W}{L})$, all symbols have its as usual meaning. IC is the function of V_{GS} , a strong parameter to defined the different region of MOS, if $IC < 0.1$ MOS operates in Weak Inversion(WI), for $0.1 < IC < 10$ in Moderate Inversion(MI) and in Strong inversion(SI) for a value of $IC > 10$. TE is the ratio of transconductance to drain current, continually decreases with IC and become half in the MI region. Since reduction in V_{DS} reduces g_m and I_D by the same ratio, hence all graphs coincide for $V_{DS}=0.2V, 0.4V$ and $0.6V$, as shown in Fig.1(a). A significant drop in g_m/g_{DS} with reduction in V_{DS} can be explained through channel length modulation(CLM) and shown in fig.1(b). Fig.1(c) represents f_t , short circuit current gain of Common Source(CS) MOS and the key characteristic to defined the speed. It is interesting to note with reduction in V_{DS} , the peak point of f_t shift in the left side and desirable for LP implementation. NF with IC is as shown in fig.1(d), NF increases with reduction in V_{DS} validate its inverse relationship with g_m . Focusing on these issues always requires a tradeoff to optimize the bias point and set the value of V_{GS} and V_{DS} [5].



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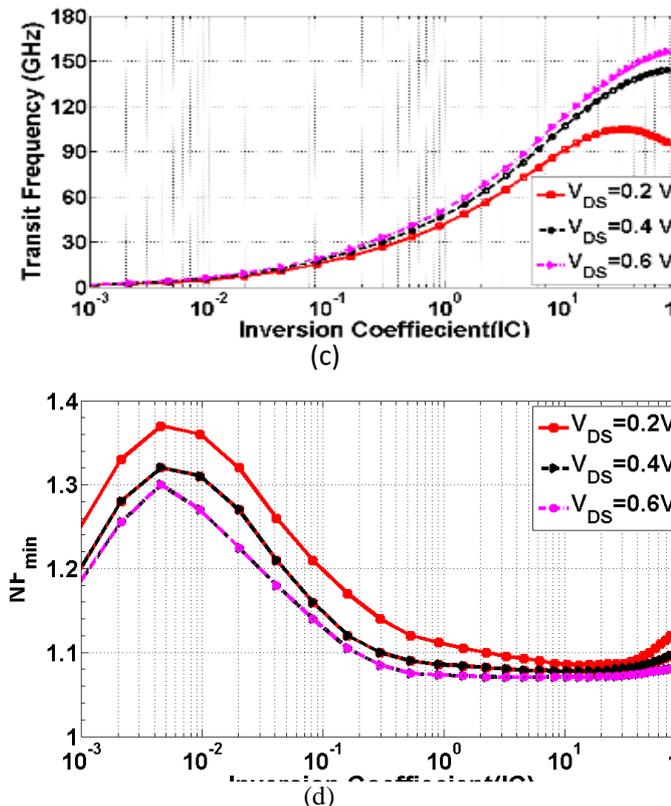


Fig.1 Low power design parameters of a NMOS transistor for different value of V_{DS} in 45nm CMOS Technology (a). Transconductance efficiency. (b) Intrinsic Voltage gain. (c) Transit frequency. (d) NF of an NMOS Transistor

Since LNA is the first active block of the receiver chain and receives a very weak signal from the antenna, it is therefore important to emphasize the low power design in such a way that added noise by LNA is as little bit, as possible, to improve the SNR. As reflections at high frequency become so significantly high, therefore input matching is another area in LNA design consideration, to maximize power transfer with minimum NF. A viable noise cancellation technique is specified with low power in literature review. In Fig.2(a) [6], Chang et al. deliberate a T-match self-body bias common gate LNA, good in ULP application (0.99mW) but suffer with the problem of low gain(7.8dB) and large area(0.73mm²) restricted it in area sensitive application operation. Since inductor consume a large on-chip area, Mahdi et al. [7], presented an inductor less tunable active shunt feedback ULP LNA. Paper depicted in fig.2(b), in which an active feedback(A_v) exists between the drain and the source terminal, gm without feedback reduced by a factor of $1+A_v$ at same matching condition (millers effect). It is desirable to ULP(0.4mW) and very less chip area (0.0052 mm²), but poor NF(4.9dB) and IIP3(-10dBm).NF can be optimized with high gain, Gm-boost CG LNA shown in Fig.(2c) but linearity (IIP3= -13dBm) is not yet satisfactory [8]. A highly linear with noise cancellation LNA proposed by Bruccoleri et al [9] as shown in fig. 2(d), but it consumes high power (35mW). A several noise cancellation has been proposed in literature, but all suffer either high non linearity or high power consumption [10]-[12]. Mutual advantage of CS and CG stage can be used on each other to improve the NF, gain and linearity. Therefore, this paper deals with the mutually coupled feedback CG-CS LNA with

noise cancellation for wide band application. Section-2 represent design analysis of the proposed LNA, Section-3 deal with simulation result, discussion and comparison with other popular work, while conclusion of proposed LNA in Section-4.

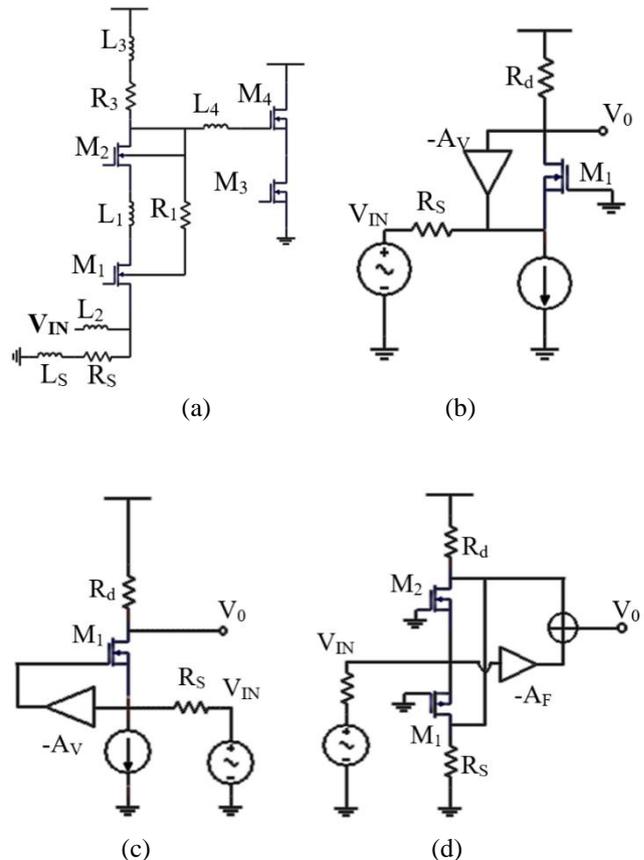


Fig. 2 Schematic of ULP LNA in state of art (a) Input T-matched wideband CG LNA. (b) Shunt feedback LNA. (c) Gm boost CG LNA (d) Block diagram of noise cancellation of LNA

II. DESIGN ANALYSIS OF PROPOSED LNA

A. Gain Analysis

Fig. 3 shows the Schematic of the proposed LNA, consisting of the mutually coupled feedback in the CS path and the CG path that links up with the summer. The CG path provides a broadband match with low NF and a mutually coupled feedback CS path is used to provide high gain. The CG stage not only reduced the noise of the CS path, but also plays an important role in reducing the overall noise. The equivalent of proposed LNA as shown in Fig. 4.

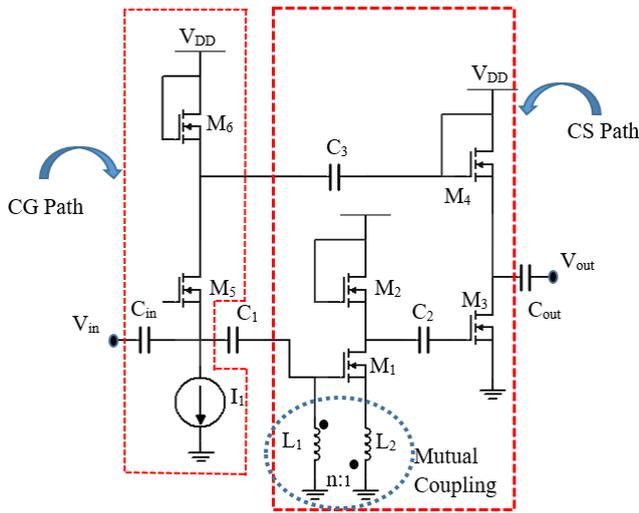


Fig.3 Schematic of proposed LNA.

In mutually coupled CS path polarity of primary coil L_1 and secondary L_2 is in opposite nature provide negative feedback. The transconductance and input admittance at input terminal of CS path mathematically given by [13].

$$G_{m1} \approx (1 + \frac{1}{n})g_{m1} \quad (1)$$

$$Y_{in} = \frac{1}{sL_1} + \frac{1}{n}(1 + \frac{1}{n})g_{m1} + sC_{gs}(1 + \frac{1}{n})^2 \quad (2)$$

where n is the turn ratio between L_1 and L_2 , since in Eq.(1) transconductance increases by a factor $1+1/n$, help a lot to improve in NF and Eq.(2) can be used for wideband matching at high operating frequency. Apart from coupling feedback CS path consist of M_1 with active load M_2 followed by a cascading of M_3 and M_4 . Overall gain of CS path is given by

$$G_V^{CS} \approx \frac{1}{2} (\frac{G_{m1}}{g_{m2}}) (\frac{g_{m3}}{g_{m4}}) \quad (3)$$

Where g_{mi} is the transconductance of respective M_i transistor. The CG path consists of M_5 with an active M_6 transistor load. Since minimum impedance is always marked when viewed from the source terminal, so at the input terminal $Z_{in} \cong 1/g_{m5}$. Thus size $(W/L)_5$ play decisive role for input terminal matching (R_S). The gain of CG path at the output terminal given by

$$G_V^{CG} \approx \frac{1}{2} (\frac{g_{m5}(r_{03} || r_{04})}{1 + g_{m5}(r_{03} || r_{04})}) (g_{m5} / g_{m6}) \quad (6)$$

Since total output voltage gain is the sum of CS and CG path and can be represent as

$$G_V^T = G_V^{CS} + G_V^{CG} \quad (7)$$

$$G_V^T \approx \frac{1}{2} (\frac{G_{m1}}{g_{m2}}) (\frac{g_{m3}}{g_{m4}}) + \frac{1}{2} (\frac{g_{m5}(r_{03} || r_{04})}{1 + g_{m5}(r_{03} || r_{04})}) (g_{m5} / g_{m6}) \quad (8)$$

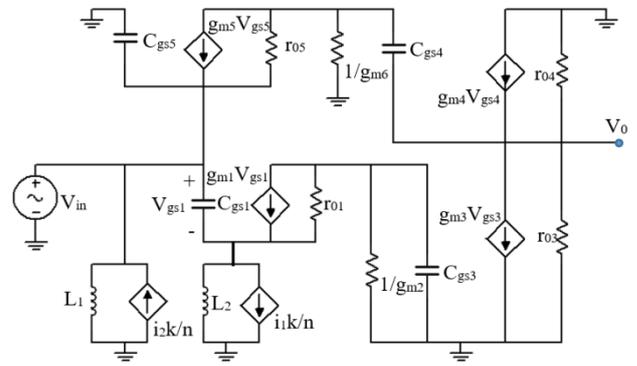


Fig. 4 Equivalent model of proposed LNA.

B. Noise Analysis

This total voltage gain defined as above plays an important role in reducing noise or improving SNR. CS path noise factor (f_{CS}) and overall noise factor (f_T) can be defined as

$$(f_{CS}) = 1 + \frac{\overline{v_{CS,n}^2}}{(\overline{v_{S,n}^2})(G_V^{CS})^2} \quad (9)$$

Over all noise factor

$$(f_T) = 1 + \frac{\overline{v_{CS,n}^2}}{(\overline{v_{S,n}^2})(G_V^{CS} + G_V^{CG})^2} \quad (10)$$

Where $\overline{v_{CS,n}^2}$ and $\overline{v_{S,n}^2}$ is the noise power of CS amplifier and source resistance power. It can be directly observed from Eq. (10), a significant decrease in the overall noise factor compared to the CS path alone, and mathematically the ratio can be defined as

$$\frac{f_T - 1}{f_{CS} - 1} = \frac{1}{(1 + \delta)^2} \quad (11)$$

Where δ represent the ratio of CG path gain to CS path gain, $\delta = G_V^{CG} / G_V^{CS}$. So common gate path not only provide to achieve the target of wide band matching but also play active role in reduction in overall noise.

III. RESULTS AND DISCUSSION

A. S Parameter

Different s parameters of the proposed LNA as shown in Fig. 5, all parameters cover UWB band range and are drawn for a frequency range of 1GHz–11GHz. Power gain(S_{21}) is positive throughout the band and the maximum value is 12.78dB at frequency 4.8GHz. The input reflection coefficient(S_{11}) is negative as desire and its minimum value is -16.36dB at 7.4GHz frequency. In the same frequency interval value of S_{22} and S_{12} is negative also shown in the same Fig. 5.

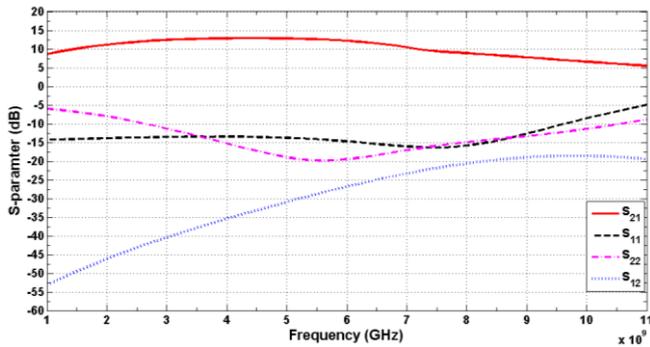


Fig.5 S-parameters (S_{11} , S_{21} , S_{12} , S_{22}) of proposed LNA.

B. Noise Figure

The noise performance of the proposed LNA was simulated for a frequency range of 1GHz–11GHz in Fig.6. The noise figure for the entire UWB band is less than 4 dB and quoted a minimum value of 2.72GHz at 3.8GHz frequency. A decrease in NF with an increase value validates its mathematics for the technique of noise cancellation.

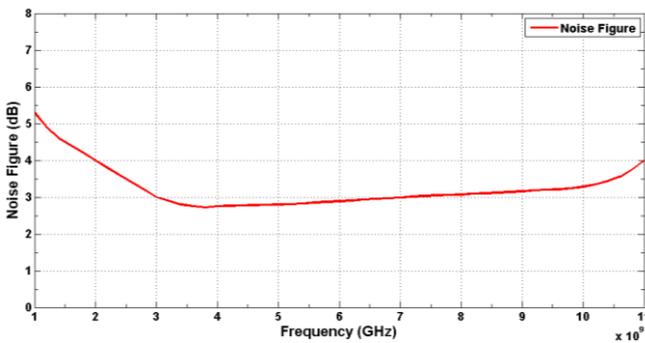


Fig.6 NF of proposed LNA.

C. Power Gain

Operating power gain (GP), which can be defined as the ratio of average output to input power and available power gain (GA), defined as the ratio of maximum output to input power and displayed in. Fig.7. Both gains are positive throughout the UWB band with a quoted maximum value of 10.26dB and 10.76dB at 9.6GHz frequency.

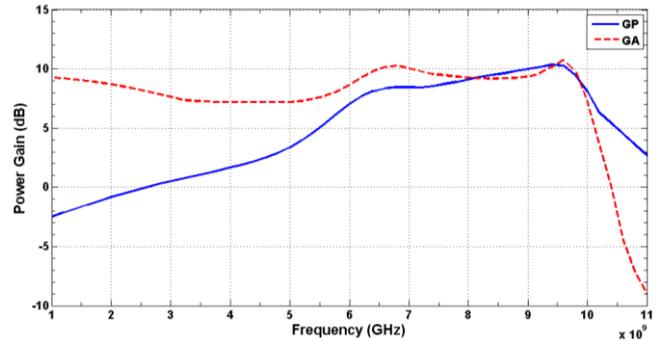


Fig.7 GP, GA of proposed LNA.

The figure of merit used as a single platform for comparison in various parameters and technologies, Equation (12) is used for the comparison of different results of the proposed LNA with the state of the art [14] and different parameters comparison is shown in Table 1.

$$FoM I = 20 \log_{10} \left(\frac{S_{21av.[lin]} \times BW_{[GHz]}}{P_{dc[mW]} \times (F_{av.[lin]} - 1)} \right) \quad (12)$$

In Table 1 it is observed that proposed LNA shows a good strength in term of input reflection coefficient noise figure and power dissipation. The bandwidth of proposed LNA is 1.4-7.8GHz. and power gain is positive throughout the band. The overall performance is better and can be observe by FoM I as compared with state-of-art.

Table 1. Performance summary of state of art with proposed work

Parameters	[20] TCAS	[15] IMS	[18] MWCL	[17] JSSC	[16] TMTT	[05] TMTT	[19] TMTT	Proposed work
3dB bandwidth (GHz)	0.2-3.8	DC-5	0.0-1.4	1.2-11.9	1.05-3.0 5	0.1-2.2	0.1-2.0	1.4-7.8
Peak Gain (dB)	19	13.9	16.4	9.7	16.9	12.3	7.6	12.87
S_{11} (dB)	<-9	<-10	<- 10	<-11	<-11	<-9	<-10	<-14.8
NF (dB)	2.8-3.4	2.76	3.0	4.5-5.1	2.57	4.9-6	3.8	2.72
P_{DC} (mW)	5.7	10.4	12.8	29	12.6	0.4	3	1.96
Supply (V)	1	1.8	1.2	1.8	1.8	1	1.2	1.2
No. of Inductors	0	2	0	5	4	0	0	2
Technique	Noise cancellation	Dual feedback	Shunt feedback	Noise cancellation	Dual negative feedback	Tunable active feedback	Feedback	Mutually coupled CG-CS
FOM I	22	-5.9	-9.2	-9	12	8.9	12	13.2
Technology	130nm	180nm	180nm	130nm	180nm	130nm	130nm	90nm

IV. CONCLUSION

The proposed LNA was simulated for a 0–11GHz wideband consisting of two stages. The first stage consists of a mutually coupled CS path used to deliver high power gain and a CG path used for wideband matching. Mathematics used for CG path noise cancellation, validate by simulation results. A bandwidth of 6.4GHz (1.4GHz–7.8GHz) is obtained in the simulation of the proposed LNA with minimum NF of 2.72 dB, Maximum and minimum values of S_{21} and S_{11} are 12.87dB, –16.38dB respectively at frequency 4.8 GHz and show a good strength, consume very less power of dissipation 1.96 mW. The Maximum value of GP and GA is 12.27dB, 10.76dB simultaneously. FoM I represent the good result as compared with other popular techniques.

REFERENCES

- Chen, Hsiao-Chin, et al. "0.5-V 5.6-GHz CMOS receiver subsystem." *IEEE Transactions on Microwave Theory and Techniques* 57.2 (2009): 329-335.
- Balankutty, Ajay, et al. "A 0.6-V zero-IF/low-IF receiver with integrated fractional-N synthesizer for 2.4-GHz ISM-band applications." *IEEE Journal of Solid-State Circuits* 45.3 (2010): 538-553.
- Balankutty, Ajay, and Peter R. Kinget. "An ultra-low voltage, low-noise, high linearity 900-MHz receiver with digitally calibrated in-band feed-forward interferer cancellation in 65-nm CMOS." *IEEE Journal of Solid-State Circuits* 46.10 (2011): 2268-2283.
- Shameli, Amin, and PayamHeydari. "A novel power optimization technique for ultra-low power RFICs." *Proceedings of the 2006 international symposium on Low power electronics and design*. ACM, 2006.
- Parvizi, Mahdi, Karim Allidina, and Mourad N. El-Gamal. "A sub-mW, ultra-low-voltage, wideband low-noise amplifier design technique." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 23.6 (2015): 1111-1122.
- Chang, J-F., and Y-S. Lin. "0.99 mW 3–10 GHz common-gate CMOS UWB LNA using T-match input network and self-body-bias technique." *Electronics Letters* 47.11 (2011): 658-659.
- Parvizi, Mahdi, Karim Allidina, and Mourad N. El-Gamal. "An ultra-low-power wideband inductorless CMOS LNA with tunable active shunt-feedback." *IEEE Transactions on Microwave Theory and Techniques* 64.6 (2016): 1843-1853.
- Belmas, François, FrédéricHameau, and Jean-Michel Fournier. "A Low Power Inductorless LNA With Double G_{m} Enhancement in 130 nm CMOS." *IEEE Journal of Solid-State Circuits* 47.5 (2012): 1094-1103.
- Bruccoleri, Federico, Eric AM Klumperink, and Bram Nauta. "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling." *IEEE Journal of Solid-State Circuits* 39.2 (2004): 275-282.
- Chen, Wei-Hung, et al. "A highly linear broadband CMOS LNA employing noise and distortion cancellation." *2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*. IEEE, 2007.
- Shim, Jaemin, Taejun Yang, and JichaiJeong. "Design of low power CMOS ultra wide band low noise amplifier using noise canceling technique." *Microelectronics Journal* 44.9 (2013): 821-826.
- Blaakmeer, Stephan C., et al. "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling." *IEEE Journal of Solid-State Circuits* 43.6 (2008): 1341-1350.
- Wu, Liang, Hiu Fai Leung, and Howard C. Luong. "Design and analysis of CMOS LNAs with transformer feedback for wideband input matching and noise cancellation." *IEEE Transactions on Circuits and Systems I: Regular Papers* 64.6 (2017): 1626-1635.
- Kumar, Manish, and Vinay Kumar Deolia. "A wideband design analysis of LNA utilizing complimentary common gate stage with mutually coupled common source stage." *Analog Integrated Circuits and Signal Processing* 98.3 (2019): 575-585.
- Chou, Hung-Ting, Shin-Wei Chen, and Hwann-KaoChiou. "A low-power wideband dual-feedback LNA exploiting the gate-inductive bandwidth/gain-enhancement technique." *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*. IEEE, 2013.
- Kim, Jusung, Sebastian Hoyos, and Jose Silva-Martinez. "Wideband common-gate CMOS LNA employing dual negative feedback with simultaneous noise, gain, and bandwidth optimization." *IEEE Transactions on Microwave Theory and Techniques* 58.9 (2010): 2340-2351.
- Liao, Chih-Fan, and Shen-Iuan Liu. "A broadband noise-canceling CMOS LNA for 3.1–10.6-GHz UWB receivers." *IEEE Journal of Solid-State Circuits* 42.2 (2007): 329-339.
- Liu, Jenny Yi-Chun, et al. "A Wideband Inductorless Single-to-Differential LNA in $0.18\mu\text{m}$ CMOS Technology for Digital TV Receivers." *IEEE Microwave and Wireless Components Letters* 24.7 (2014): 472-474.
- Kim, Jusung, and Jose Silva-Martinez. "Wideband inductorless balun-LNA employing feedback for low-power low-voltage applications." *IEEE Transactions on Microwave Theory and Techniques* 60.9 (2012): 2833-2842.
- Wang, Hongrui, Li Zhang, and Zhiping Yu. "A wideband inductorless LNA with local feedback and noise cancelling for low-power low-voltage applications." *IEEE Transactions on Circuits and Systems I: Regular Papers* 57.8 (2010): 1993-2005.
- Borremans, Jonathan, et al. "Low-area active-feedback low-noise amplifier design in scaled digital CMOS." *IEEE Journal of Solid-State Circuits* 43.11 (2008): 2422-2433.

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