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VLSI Implementation of 2-D Discrete Wavelet Transformation using Reversible Logic Gates

P. Kowsalya, S. M. Sakthivel

Abstract: ***The two dimensional Discrete Wavelet Transform (DWT) has received much attention over the last two decades in many multimedia applications such as MPEG-4 processing, JPEG2000 based compression, information retrieval systems and digital image watermarking. Therefore in the present work rather than implementing the DWT using conventional convolution based methodology, a Lifting and Haar wavelet based realization is incorporated to reduce the storage of algorithm and computational complexity. Furthermore the delay, power and efficiency of the DWT architecture are reduced and increased respectively by implementing the proposed architecture using reversible logic gates. Also the implementation of reversible logic gates based DWT structure preserves the data integrity without any loss of information during image processing adding together a parallel & pipelined architecture of the Haar wavelet DWT is implemented in this paper work using " gpdk 180nm" technology. The overall ASIC implementation of reversible DWT using cadence EDA tool consumes an area of 406.45.5 sq.µm , delay of 2.169ns & power of 14808.103nW.***

Index Terms: ***Reversible logic gates, 2-D DWT, Haar wavelet, lifting scheme, ASIC & Cadence EDA ® tools.***

I. INTRODUCTION

The two dimension discrete wavelet transform is one of the widely used image transformation techniques in the image processing applications such as human face detection, feature extraction of an object, processing of medical images for various needs of patient monitoring and also in the field of remote sensing. For many years the image processing algorithms are implemented using discrete cosine transform (DCT) and fast Fourier transform (FFT) [28]. Few researchers have addressed the problems of DCT and FFT in terms of computational complexity and memory requirement. To overcome such issues of DCT and FFT, the discrete wavelet transform is established. Traditionally the DWTs are implemented using convolution technique and it required complex FIR filter based architectures for its performance. As the traditional DWT based architecture involves more complex structure and computational intense operation an efficient architecture is developed to reduce the Computational complexity that can be used for image processing applications. Therefore in DWT the lifting Haar wavelet transforms based realization is carried out in this research work. Firstly we have developed architecture for irreversible logic gate based DWT and IDWT using Haar wavelet transform.

In 1961 Rolf Landeaur et al proposed a technique in which reversible logic gate based realization concept is used. [8]. Due to the use of reversible logic realization, the information loss is associated with loss of energy and heat dissipation [1] & [2]. Due to the aforesaid reason the today's technology of digital circuit faces a lot of problems in the field of the area, input power, power dissipation and speed with respect to the number of transistors per chip and reduction in the size of the device. The reversible logic gate based circuits can reduce the problems faced by irreversible logic circuits [3].

The theoretical based analysis states of reversible logic illustrates that there is no loss of information in reversible logic circuits and can be obtained zero power dissipation [1]. This primarily due to the fact that the reversible logic gate has a number of inputs which are equal to the number of outputs Due to this one to one mapping of input and [6]&[15] the physical process is logically reversible which makes the circuit to work with less power. Therefore to reduce power, in the digital circuits the reversible logic realization is considered to be one of the most efficient and accepted methodology. [20],[22],[24]&[25].

The low power VLSI design based DWT and IDWT architectures need area and power efficient circuits for its operation this can be possible only using reversible logic and promising results also established efficient computational platforms [34]&[36]. Secondly we have developed architecture for reversible logic gate based DWT and IDWT using Haar wavelet transform. In addition to that, the lifting based DWT is suitable for all types signal that has low-frequency and high-frequency components for long duration and short durations respectively.(i.e. Images and Video frames[11],[12,[13],[14]&[16]). Thirdly parallel and pipelined architecture for irreversible and reversible logic gates have been designed using lifting scheme.

II. LIFTING SCHEME

The lifting scheme for bi-orthogonal wavelets is introduced by Sweldens. All of the constructions of discrete wavelets can be carried out in the spatial domain. The lifting based DWT is different from convolution and it is also called second generation wavelet.

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***** Correspondence Author
P. Kowsalya, SENSE, VIT University, Chennai, (TN) India.
S. M. Sakthivel, SENSE, VIT University, Chennai, (TN) India.

The DWT using lifting has less computational complexity. The integer numbers based sequence is known as a digital signal (Image). The application of convolution discrete wavelet transform on digital signals yields floating point results and this can be eliminated using lifting based algorithms with logic shifters. The integer to integer results can be produced by the application of lifting scheme on digital signals and reversing of the original digital is possible without any loss of information.

The lifting based DWT construction involves in the following three steps. They are split, predict and update. In this paper, we are using lifting based Haar wavelet transform for DWT and IDWT implementations. The Haar transform produces wavelet coefficients by performing average and difference on the adjacent samples. The results of average and difference shifted to get the details and edges of a digital image. The following figure 2.1 explains the basic operation of lifting scheme in Haar DWT and IDWT mode.

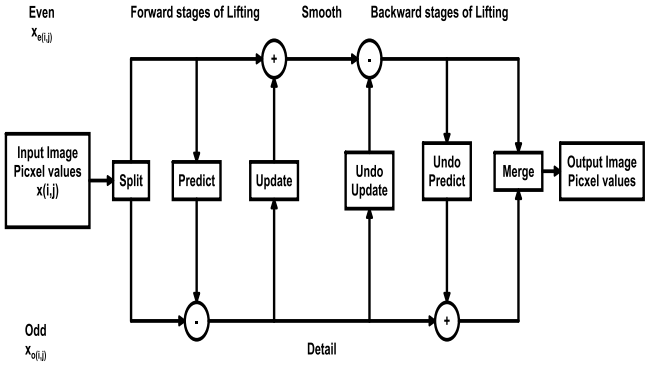

Fig.2.1. Basic Operation of two dimension lifting schemes based Haar DWT and IDWT operations

Let us consider an digital image signal $x_{(i,j)}$ with 2^j samples.

A. Forward stage of lifting

Split: This is the first stage of lifting based Haar wavelet transform. The considered image $x_{(i,j)}$ is split into odd and even samples and it is known as lazy wavelet transform.

$$(x_{e(i,j)}, x_{o(i,j)}) = \text{Split}(x_{(i,j)})$$

Predict: The Haar prediction is simple and it uses even samples to predict the odd samples.

$$D_{j-1} = x_{o(i,j)} - P(x_{e(i,j)})$$

Update: In this stage updates the difference value for the average calculation.

$$S_{j-1} = x_{o(i,j)} + U(x_{e(i,j)})$$

B. Backward stage of lifting

The lifting based Haar based inverse discrete wavelet transform involves reversing the predict and update operations of DWT and merging of the odd and even samples.

Undo update: This is the first stage of IDWT, in this, we will subtract the updated information from the sample and produce even samples.

$$x_{e(i,j)} = S_{j-1} - U(D_{j-1})$$

Undo predict: we will just add the predicted information with difference and average to get odd samples.

$$x_{e(i,j)} = S_{j-1} + P(D_{j-1})$$

Merge: To get the $x_{(i,j)}$ of the image signal we will just merge even and odd sample. The lifting is very efficient because of integer to integer mapping.

The two dimensional DWT is generated by the row and column wise processing of two 1D DWT on the sample values of the digital image signal. The L and H samples can be produced by row-wise application of 1D- DWT. The column-wise application of 1D-DWT produces LL, HL, LH, HH samples of the digital image signal and which results in the 2D-DWT. The following figure 2.2 illustrates the working of 2-D DWT.

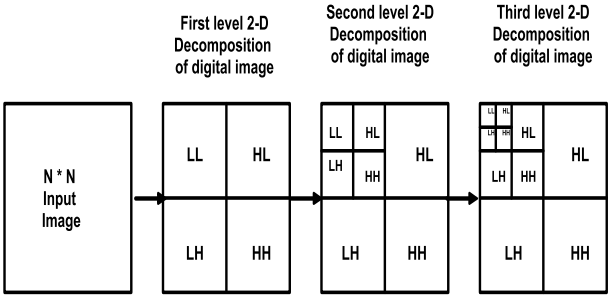

Fig.2.2. The illustration of two dimensional DWT

The lifting DWT can be implemented without any involvement of multiplication operations so which reduces the computation time of the system and hardware complexity. Moreover the memory requirement is also very less compared to other mode of realization. The lifting mode of Haar DWT system can be implemented without any filters. We have proposed irreversible and reversible logic gates based discrete wavelet and inverse discrete wavelet transform using parallel and pipelined architectures and proved that system based on reversible logic can be implemented with less delay when compared to irreversible logic gates based design system.

III. REVERSIBLE LOGIC GATES

As mentioned above the heat generation caused by the power dissipation in digital circuits is the major problem in irreversible logic gates based module design. The power dissipation of reversible logic circuits under ideal circumstance is zero. There is no unavoidable energy consumption in reversible logic computers. Therefore lot gates has been proposed and used using reversible logic style which could play a vital role in the digital circuit implementation. From the reported researchers we have identified a few reversible gates such as Fredkin gate, Feynman gate or CNOT gate, Perese gate and Toffoil gate. In digital circuit design, the loss of heat in circuit is considered as the information loss. Therefore the data bit loss is calculated using the of information lost formal K T ln 2, Where K represents *Boltzmann' constant* and T is the temperature of the system. The reversible computation makes the system to work with higher density and speed. The reversible computation follows three basic rules for the realization of any reversible logic circuits. They are all required operations of the implementation of reversible logic based circuit could be reversible without heat dissipation. The input could be uniquely revertible from the output and this is known as logically reversible. The reversible logic should follow the working principle of thermodynamics second law and guarantees no heat dissipation. The reversible gate based system has a number of input equal to the number of outputs and the inputs of the gate can be retrieved from the outputs of the same system so there is no loss of information.

The reversible gates based device can be powered by itself without any additional power supply. The practical implementation of DWT requires information lossless system for its proper function. The image processing in the real time should be clear and if there is any functional failure in the system based on the previous blocks output we can predict the input and perform the upcoming operations. The proposed design consists of Reversible TR Gate, Reversible R gate and Reversible D flipflop in the DWT and IDWT design.

A. FEYNMAN GATE

The Feynman gate or (CNOT gate) has 2 inputs 2 outputs. They are A, B as input and P=A, Q=(A⊕B) as output. The quantum of the Feynman gate is 1. The following figure 3.1 is the gate diagram of Feynman Gate

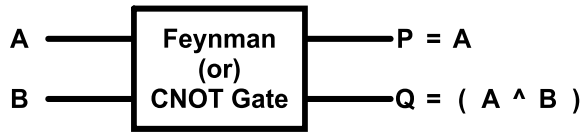

Fig.3.1. Feynman Gate

B. FREDKIN GATE

The Fredkin gate has 3 inputs 3 outputs. They are A, B,C as input and P=A, Q=(((~A)&B)|(A&C)) , R = ((A&B) |((~A)&C)) as output. The quantum of the Fredkin gate is 5[36]. The following figure 3.2 is the gate diagram of Fredkin Gate

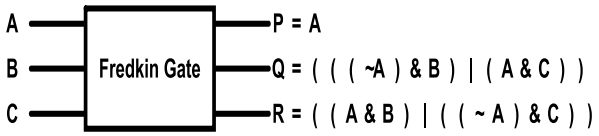

Fig. 3.2. Fredkin Gate

C. REVERSIBLE TR GATE

The TR gate has 3 inputs and 3 outputs. They are A, B, C as input and P= A, Q= (A ⊕B), R = ((A&(~B))⊕C) as output. The quantum cost of the TR gate is derived from reversible gates like Toffoli gate, NOT gate and CNOT gate. The TR gate can be derived by using the two NOT gate, one Toffoli gate, and one CNOT gate. The quantum cost of the Toffoli gate is five. The quantum cost of the NOT gate is zero and the CNOT gate is one. The quantum cost of the TR gates is 5 +1 = 6. The subtractor design of the proposed reversible DWT has been proposed using the TR gate [36]. The following figure 3.3 is the gate diagram of TR Gate.

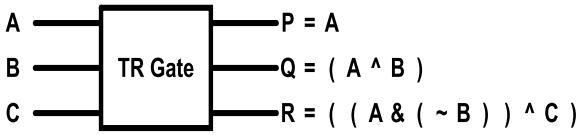

Fig.3.3. TR Gate

D. REVERSIBLE R GATE

The R gate has 3 inputs and 3 outputs. They are A, B, C as input and P= (A⊕B), Q= A, R = ((~C) ⊕ (A&B)) as output. The quantum cost of the R gate also can be derived from reversible gates like Toffoli gate, NOT gate and CNOT gate as like TR gate quantum cost calculation. The R gate can be derived by using the two NOT gate, one Toffoli gate, and one CNOT gate. The quantum cost of the Toffoli gate is five. The quantum cost of the NOT gate is zero and the CNOT gate is one. The quantum cost of the R gates is 5 +1 = 6. The Adder design of the proposed reversible DWT has been proposed using the R gate. The following figure 3.4 is the gate diagram of R Gate.

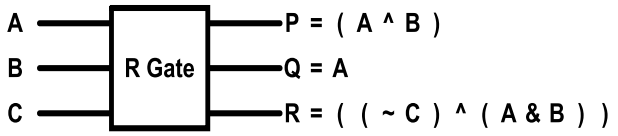

Fig.3.4. R Gate

E. D FLIPFLOP:

The reversible D flipflop has been designed using Fredkin and Feynman gates. The inputs of the D flipflop are D and clk and the outputs are Q and Qbar. The operation of D flipflop can be characterized as when the clock is high the Q= D and when the clock is zero the Q just holds the previous state output. The quantum cost of the D flip flop is 7 and has two garbage outputs. The following figure 3.5 is the circuit diagram of reversible D flipflop.

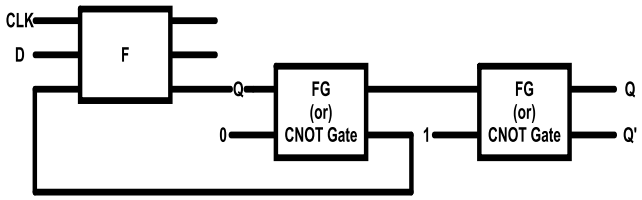

Fig. 3.5. Circuit diagram of reversible D Flipflop.

IV. PROPOSED ARCHITECTURE

There are number of architecture are available for implementation of DWT using irreversible logic gates. In this paper, we have proposed reversible logic based architecture for 2-D DWT using Haar Wavelet transform. At the starting stage of the active clock edge, the DWT system receives N x N inputs and the outputs are available before the active clock edge deactivates.

The detailed explanation of proposed architectural of DWT & IDWT operations are presented with the corresponding block diagram in the below sub sections.

A. THE PARALLEL ARCHITECTURE OF DWT AND IDWT USING REVERSIBLE AND IRREVERSIBLE LOGIC GATES

In this section, the parallel mode of architecture for lifting based 2-D DWT using irreversible as well as reversible logic gates is proposed and discussed. The reversible DWT design consists of reversible logic gates based modules for its operation. In particular, the reversible R gate is used for the adder design.

The reversible TR gate is used for the subtractor design. The Feynman gate, Fredkin gate are used for the basic reversible D flip flop design based on Himanshu Thapliyal's research paper works. The irreversible DWT design consists of normal logic gates for its operation. The 2-D DWT operation is carried out by row and column-wise 1-D DWT operations. The row-wise 1-D DWT is performed on the odd and even samples of an image and then the column-wise 1-D DWT is performed on the resultants of the row wise operation. The lifting based Haar wavelet system works as three stages for performing the 1-D DWT. At the first stage, the inputs of an image are split as odd and even sample and read by an array of the proposed memory unit. For instance, the odd and even sample stored in the memory which is fed as input to the low nd high pass filter unit for alternative sample elimination process and this is carried out in the update and predicts stages of the DWT system. The update and predict values of the sample are calculated by the simple addition and subtraction operations.

Let us consider $X_{(i,j)}$ as input samples of an image. The split odd and even sample of a digital image are $Xo_{(i,j)}$ and $Xe_{(i,j)}$. The difference calculation between the odd and even samples work as the high pass filter $d_{(i,j)}$ and the average calculation between the odd and even samples works as the low pass filter $s_{(i,j)}$ in Haar based DWT. The split signals of the digital image are captured by the predictor unit to predict the odd samples and this is the second stage of the lifting. We are using even sample to predict the odd sample for further process. The output of the predictor unit inputs is taken as the input for the update unit. This update-unit simply calculates the average between the predicted samples and even samples and this is known as the 3rd stage of lifting. Then the results are shifted to perform the up-sampling. To get the original pixel values of the image back, the output of the DWT are taken as the input and down-sampled. The even samples can be obtained by undoing the update operation and the odd samples are obtained by undoing the predict operation. The retrieved odd and even samples are merged together to get the original image back. The Haar wavelet transform can work without any multiplication process. So the elimination of multiplier makes the system work faster. In this paper, we have designed the parallel architecture of DWT using both irreversible and reversible logic gates. The delay of the reversible logic gates based DWT design is lesser than the irreversible logic based DWT design and this has been proved in this paper. The performance of the reversible logic based DWT can be increased further using pipelining. The proposed parallel architecture takes N clock cycles to perform one pair of odd and even sample addition this can be reduced by the application of pipelining techniques. The following figure 4.1 illustrates the parallel architecture of the reversible DWT & IDWT operations.

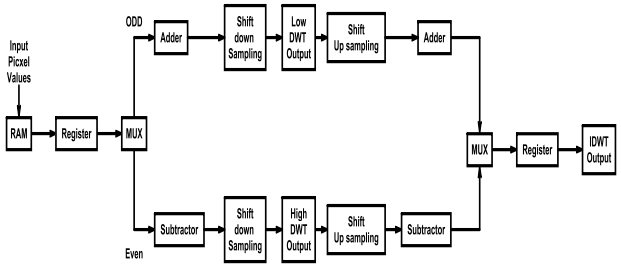

Fig. 4.1. Parallel Architecture of reversible DWT &IDWT

B. THE PIPELINED ARCHITECTURE OF DWT AND IDWT USING REVERSIBLE AND IRREVERSIBLE LOGIC GATES

The pipelined architecture fof lifting based two dimension DWT using irreversible and reversible logic gates has been proposed to improve the architecture performance (i.e increase the speed of operation with low power consumption). The reversible pipelined DWT & IDWT architecture also consists of reversible logic gates based modules for its operation. As like the parallel reversible DWT, the reversible R gate is used for the adder design. The reversible TR gate is used for the subtractor design. The Feynman Gate, Fredkin gate is used for the basic reversible D flip flop design. The operation of pipelined 2-D DWT is performed by the row and column wise application of the pipelined 1-D DWT. The row-wise pipelined 1-D DWT is performed on the odd and even samples of an image and then the column-wise pipelined 1-D DWT is performed on the resultants of the row wise operation.

The 1-D DWT has 3 stages. They are split, predict and update after each stages the output are stored in the additional registers. At the first stage, the inputs of an image are split as odd and even sample and read by an array of proposed memory unit the same as the parallel operation. The odd and even samples stored in the separate additional memory are fed to update and predict stages of the pipelined DWT system tp eliminate the alternate samples. The update and predict values of the sample are calculated by the simple addition and subtraction operations and the results are stored in the intermediate small registers. Here the 3 stages pipelining is used to implement the lifting based reversible pipelined architecture of DWT and IDWT using Haar wavelet transform. The following figure 4.2 illustrates the 3 stage pipelining operation of the developed system.

As we know, there are three stages in 3 stage pipelining system. Such as fetch, execute and write. In particular, during the fetch cycle the discrete image samples are fetched in to the input register. The fetched samples are executed and write back to the corresponding output register during execute and write cycles.

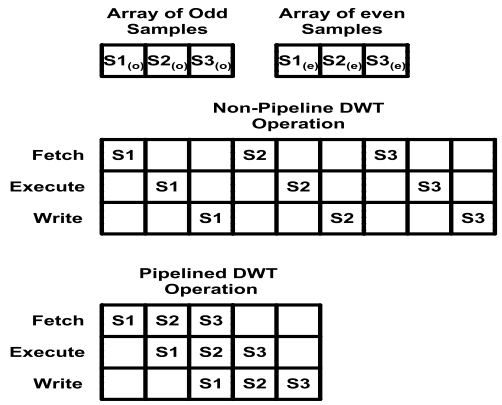

Fig.4.2. Non-Pipelined and Pipelined DWT Operation Flow Diagram

Let us consider $XSPipe_{(i,j)}$ as input samples of an image. The split odd and even sample of a digital image are $XSPipee_{(i,j)}$ and $XSPipeo_{(i,j)}$. The difference calculation between the odd and even samples work as the high pass filter $dpipe_{(i,j)}$ and the average calculation between the odd and even samples works as the low pass filter $sPipe_{(i,j)}$ in Haar based DWT. The split signals of the digital image are captured by the predicting unit to predict the odd samples and this is the second stage of the lifting. The results of the predictor unit are stored in the register A. We are always using even sample to predict the odd sample for further process. The output of the predictor unit inputs is taken as the input for the update unit. This update unit simply calculates the average between the predicted samples and even samples and this is known as the 3rd stage of lifting and the results are stored in the B register. Then the results are shifted to perform the up sampling and the results are stored using intermediate registers. To perform the inverse discrete wavelet transform and get the original pixel values of the image back the output of the DWT are taken as the input and down sampled. The even samples can be obtained by undoing the update operation and the odd samples are obtained by undoing the predict operation. The retrieved odd and even samples are merged together to get the original image back.

The delay of the proposed pipelined architecture of the reversible DWT is lower than the proposed parallel reversible DWT. The number of clock cycles per addition also reduced and circuit efficiency also has been increased using reversible logic gates. The following figure 4.3 illustrates the Pipelined architecture of reversible DWT & IDWT operations.

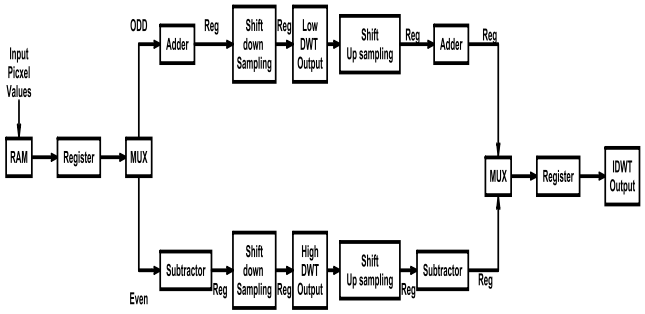

Fig. 4.3.Pipelined Architecture of reversible DWT & IDWT

V. RESULTS AND DISCUSSION

In this section, the simulation results of the proposed DWT and IDWT architectures have been discussed and effective comparisons are given in the following tables. The latency or Delay of the circuit determines the overall efficiency of the proposed system. As we know the adder present in the circuit takes one unit time for its operation. To increase the performance of the DWT and IDWT system the adder and subtractor design should be efficient. The different adders have been designed using irreversible and reversible logic gates. The following table 1 shows the delay comparison of different adders. The following table 2& 3 shows the results of the reversible and irreversible DWT& IDWT using different adders. The delay of the Irreversible and reversible, DWT and IDWT architectures using different adders have been calculated in nano-seconds. The carry look ahead adder and the ripple carry adder based DWT & IDWT design have a lesser delay than the other adders based design.

Table 1 Delay comparison of reversible and irreversible adders

S.No.	Adder type	Irreversible adders delay in (ns)	Reversible adders delay in (ns)
1.	Ripple carry adder	2.830	1.058
2.	Carry look ahead adder	2.959	1.978
3.	Carry skip adder	4.641	1.989
4.	Carry select adder	2.830	1.058
5.	Carry save adder	4.221	1.869
6.	Carry bypass adder	3.583	1.561
7.	Carry increment adder	3.451	2.640

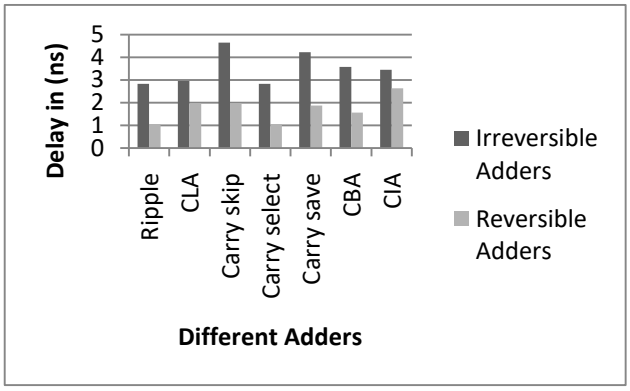

Fig. 5.1. Delay comparison of adders

This above graph is drawn between different adders and produce delay by adders in nano-seconds. Furthermore the above graph shows that the adders design using reversible logic produces lesser delay than irreversible logic based design.

Table 2 Delay calculation results of reversible and irreversible logic based Parallel DWT using Different adders

S.No.	Parallel Dwt + Adder type	Irreversible Parallel dwt+ adders delay in (ns)	Reversible Parallel dwt+ adders delay in (ns)
1.	Dwt using Ripple carry adder	2.901	2.635
2.	Dwt using Carry look ahead adder	2.641	2.415
3.	Dwt using Carry skip adder	3.032	2.635
4.	Dwt using Carry select adder	2.901	2.635
5.	Dwt using Carry save adder	3.872	2.635
6.	Dwt using Carry bypass adder	2.646	2.457
7.	Dwt using Carry increment adder	2.783	2.551

This below graph is drawn between DWT implementation using different adders and produce delay by DWT in nano-seconds.

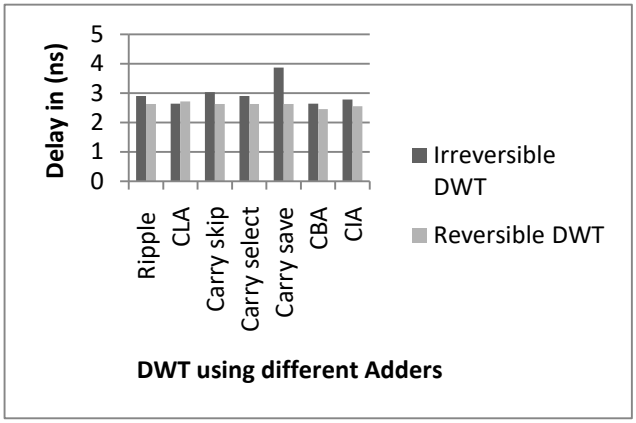

Fig.5.2. Delay comparison of DWT

Table 3 Delay calculation results of reversible and irreversible logic based Parallel IDWT using Different adders

S.No	Parallel IDwt + Adder type	Irreversible Parallel Idwt+ adders delay in (ns)	Reversible Parallel Idwt+ adders delay in (ns)
1.	IDwt using Ripple carry adder	2.901	2.709
2.	IDwt using Carry look ahead adder	2.905	2.709
3.	IDwt using Carry skip adder	3.032	2.729
4.	IDwt using Carry select adder	2.901	2.709
5.	IDwt using Carry save adder	3.872	2.899
6.	IDwt using Carry bypass adder	2.934	2.9031
7.	IDwt using Carry increment adder	2.899	2.899

This below graph is drawn between IDWT implementation using different adders and produce delay by IDWT in nano-seconds. Furthermore the above graph shows that the IDWT design using reversible logic produces lesser delay than irreversible logic based design.

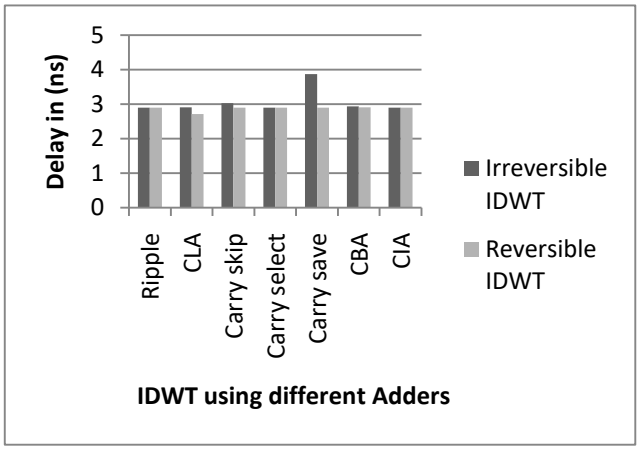

Fig.5.3. Delay comparison of IDWT

The system performance and the speed can be increased using the proposed pipelined architecture. The delay of the pipelined architecture for reversible and irreversible logic based DWT and IDWT has been calculated in nano-seconds. The proposed pipelined design of the DWT and IDWT using reversible logic has a lesser delay than the architectures based on the irreversible logic gates. The number of clock cycles per addition and subtraction has been reduced. The following table 4 shows the results of the pipelined reversible and irreversible DWT& IDWT. The proposed reversible logic-based design can be operated with low power and high speed. The overall efficiency of the DWT and IDWT system has been increased.

Table 4 Delay calculation results of reversible and irreversible logic based Pipelined DWT & IDWT

S.No.	Type	Delay in (ns)
1.	Pipelined Irreversible Dwt	2.169(min)
2.	Pipelined Irreversible iDwt	2.169ns(min)
3.	Pipelined Reversible-Dwt	1.807ns(max)
4.	Pipelined Reversible-iDwt	1.552ns(max)

The following table 5 shows power and area calculations of the pipelined reversible and irreversible DWT& IDWT. The proposed reversible logic-based design can be implemented with low power and with less area. The overall efficiency of the DWT and IDWT system has been increased with reduction in power. The entire analysis has been carried out using cadence EDA tool.

Table 5 Power and Area calculation of Proposed DWT & IDWT Architecture

S.No.	Type	Area in Square Milli-Meter(Sq.µm)	Power in Nano-Watt(nW)
1.	Reversible parallel DWT	406.455	14808.103
2.	Reversible parallel IDWT	425.378	15559.519
3.	Reversible pipeline DWT	466.250	18306.703
4.	Reversible pipeline IDWT	466.250	18211.742

Fig. 5.4. 2D-DWT outputs of Gray-scale image

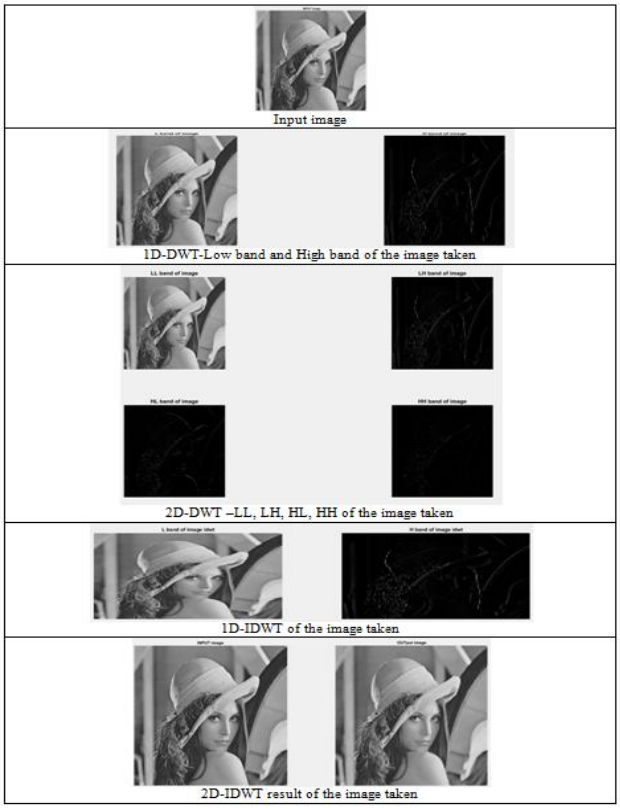

Fig.5.5. 2D and 3D level decomposition outputs of Gray-scale image

Fig.5.6. Color bands of input image

Fig.5.7. 2D level decomposition output of color image

Table 6 Image Quality Measures calculation result for different gray-scale images

S.No.	Different Gray images	Average Difference (AD) B/W before and after DWT and IDWT	Maximum Difference (MD) before and after DWT and IDWT	Mean Square Error (MSE)before and after DWT and IDWT	Normalized Absolute Error (NAE)before and after DWT and IDWT	Normalized Cross Co-relation (NK) before and after DWT and IDWT	Peak Signal to Noise Ratio (PSNR)before and after DWT and IDWT	Structural Content (sc)before and after DWT and IDWT
1.	Barbara	0	127	259.7166	0.0764	1.0251	23.9858	0.9381
2.	Fruit	0	184	827.6603	0.0842	1.0224	18.9523	0.9350
3.	Cat	0	123	166.7756	0.1006	1.0373	25.9095	0.9122
4.	Aeroplane	0	127	288.6172	0.0416	1.0132	23.5276	0.9663
5.	Fish	0	186	502.7903	0.1331	1.0303	21.1169	0.9097
6.	Owl	0	104	322.5709	0.1343	1.0435	23.0446	0.8921
7.	Monkey	0	120	488.0555	0.1043	1.0348	21.6175	0.9139

The image quality measures are used to measure the quality of the retrieved image from DWT. The average difference between the input and the output images are null and from this we can understand that there is no difference between the original and the processed image. The normalized absolute error between the input and the output images are less than one by this we can understand that the transmitted input image can be recovered from the DWT unit without loss of any information.

The following table shows the result of image quality measures between the input and output images.

VI. CONCLUSION

The simulation result of proposed DWT & IDWT structure using various adders have been evaluated and effective comparison is given. In order to verify the proposed DWT & IDWT architecture, the functional simulation has been carried out using Xilinx 14.7. the ASIC implementation of proposed design has been carried out using cadence EDA tool. The synthesis and design for testing is realized using "cadence genus" & the physical design implemented using "cadence innovus". In order to justify the proposed functionality we simulated the same algorithm using matlab. For the matlab simulation the standard test image lenna of size 1024 *1024 has been studied. The input and output of the image during simulation is tabulated. Further the efficiency of the algorithm is evaluated using the image quality metrics AD, MD, PSNR, NCC, SC, NAE and MSE. The corresponding values of each image quality measures are also tabulated. The average difference of the original and output images are zero and mean square error is less. The proposed design of DWT and IDWT architectures are synthesised and tested using design for testing. The lifting and Haar wavelet transform based DWT & IDWT architectures using reversible and irreversible logic gates have been proposed in this paper, in which the comparison between the reversible and irreversible architectures of the DWT & IDWT have been made. The DWT architecture using reversible logic has a lesser delay than the irreversible logic gates based DWT architectures and it has been proven with results. The tested image quality of the output image is equal to the input image.

The scaling of the proposed architecture is possible. The N*N high-quality images also can be processed using the proposed architecture with high efficiency. The watermarking using proposed DWT & IDWT also implemented and verified. Based on the entire contribution of our work, proposed architecture requires dataflow control units for its efficiency. The clock performance should be improved.

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AUTHORS PROFILE

P. Kowsalya currently pursuing her MTECH VLSI in VIT Chennai, Interested especially in Front end Custom design & functional verification.