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Floor Planning of 256 tap FIR filter using Flip-chip Technology for IR Drop and EM Effect Avoidance

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Abstract -- Flip chip ICs are one of the emerging packaging technology that offers high integration density with an increase in the number of IO pads. Voltage drop in the power/Ground network of these designs has becomes a serious concern in the design of modern chips. This paper presents a co-synthesis process to determine the optimal mesh network in order to achieve the power constraints. Given a fixed locality of P/G pin, the proposed method performs incremental floorplanning to effectively reduce the IR drop and EM violations. First, a 256 tap FIR filter is implemented in flipchip package operating with multiple supply voltages and then it performs the proposed methodology to accomplish the power constraints. Simulation results on 256 tap FIR filter circuit shows that the presented algorithm successfully eliminates the IR drop and EM violations at the floorplanning stage while preserving the floorplan quality and P/G network.

Index – Floorplanning, P/G network, IR aware incremental floorplan, IR drop, Multiple supply voltage.

I. INTRODUCTION

Due to technological advancements, there is continuous scaling down in feature size of the layout, thereby making the power planning stage more complex. IR drop comes out as a serious concern when power delivery network is looked upon and it may even induce EM violations degrading the performance of chip [1]. Generally, the IR drop in the design layout is determined using different two ways, namely static and dynamic. Static IR methodology uses design operating frequency and gives voltage drop in the layout. Dynamic methodology determines the voltage drop in the layout for all possible scenarios under a timing constraint. In this analysis, the physical designer performs refinement in the layout within a tolerable drop limit. Generally, the threshold limit for IR drop is set as 10% for supply voltage. For example if the operating voltage is 1.0V, 0.9V is considered as maximum IR budget.

The authors in [2,3] show that IR drop using static flow gives optimistic or pessimistic results based on the complexity of circuit. Different from these articles, this paper uses static IR drop approach in early stages of physical design process to determine the IR drop in the layout. IR drop is mainly due to the excessive voltage across the resistance in the power grid mesh.

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Hence, the early research focus on determination of mesh width and sizing of mesh to reduce this IR drop [4,5]. Some of the research works use mathematical tools such as Conjugate-gradient method [6], Sequential LP method [7], Incomplete Cholesky Decomposition Conjugate Gradient method [8], Multigrid-based method [9], and tree structures [10] to solve this IR drop problem.

In this paper, a floorplanning methodology is presented to reduce IR in the flip chip based layout consisting of voltage islands. After extensive studies, it is understood that most research works exist in the literature to provide solution to IR drop reduction in flip chip designs having one VDD [11]. Even though flip chip packaging gives better solution to this IR drop problem, the complexities in I/O pad bonding in the layout with multiple supply rails adds more challenges in the physical design process.

The contributions in this paper are summarized as follows

- Layout implementation of 256 tap FIR filter using flip chip technology.
- Using the work presented in article [12], this work performs voltage island floorplanning and satisfy the power constraints.
- Determines the optimal mesh structure considering wirelength and number of optimal wirelength.

This article is organized as follows: Section 2 presents the power mesh structure incorporated and its parameters evaluated in this paper. Section 3 describes flip chip design of FIR filter and design flow involved in construction of its layout. The section 4 presents the simulation results and determination of optimal mesh structure.

II. BACKGROUNDS

In flip-chip design with multiple supply voltage, supply voltage is delivered to the chip through power and ground pins. The power network is shown in the Fig.1 where power pad refers to I/O pad which data signals into the chip, core rings are the power lines enclosing the floorplan, power trunks are the branches from a core rings to a module, a P/G node is intersection of horizontal and vertical power lines. In a power mesh structure, the pitch is interpreted as the gap between the wires and width represents thickness of wire. In this article, the power rings and stripes in the layout are modelled using different metal layers to geometric and other performance related issues. Each block acts as a current source and the current flows from the block through the power grid and hence ir drop occurs due to the resistance of the power grids. So in order to reduce the ir drop, the modules are kept in close proximity to P/G pins, but this might increase the wirelength and metal coverage of power wires in the chip.

If IR drop is high, the modules in chip cannot operate properly, hence in the proposed design the maximum allowed IR drop is constraint to 10% of the voltage supply of P/G pin.Thus, this article present a methodology to reduce the IR drop in layout through effective floorplanning of modules in the design. Metal coverage points out what percentage of the total area of the power wire is occupied by total power delivery network. It can be obtained by the ratio of area of power delivery network to total of the power wire. Metalcoverage = Apower/ Achip Apower denotes the area of power delivery network and Achip refers to the total chip area. Metal coverage also plays an important role in IR drop constraints. It should be in a range wherein it enables to supply more power to the chip as well as keeping routing congestion in check, thereby not degrading the chip.Hence the IR drop violations can also be reduced by using the routing resources optimally.

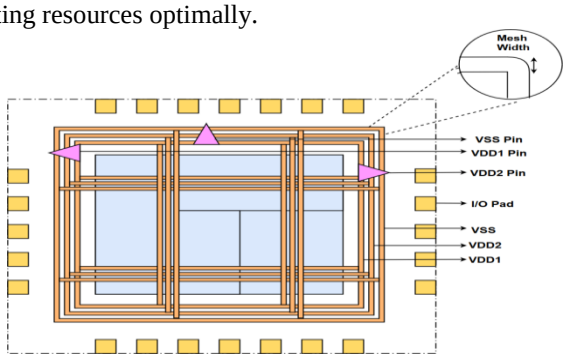
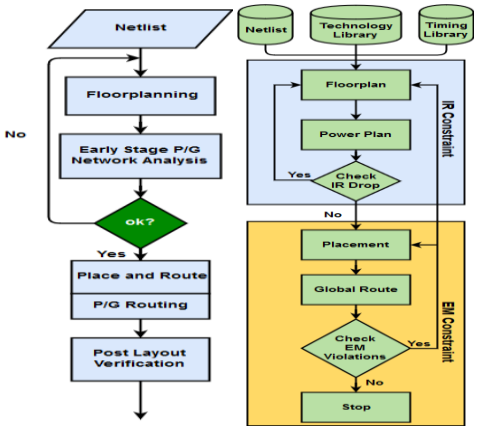


Fig. 1.Power Delivery Network

Electron migration(EM) effect is another important parameter which needs to be analysed if a design passes the IR violations. Even though the proposed techniques floorplans for reduced IR drop, the excess current signals flowing from or in the interconnects lying between the features in the layout makes its ions to drift and cause electrons to flow with high velocity. The result is the gradual displacement of metal atoms in a semiconductor, potentially causing open and short circuits. Hence this paper also verifies layout for reduction of EM violations and adds a methodology in addition to the proposed algorithm in the early stages of the design flow.

III. PROPOSED FLOORPLANNING METHODOLOGY

A. Overview



(a) (b)

Fig. 2.Design Flow (a) conventional(b) proposed

Figure 2 shows the conventional[13] and proposed design flow for identifying the IR drop in the layout. Different from the conventional design flow in 2(a), this paper implements the proposed floorplanning methodology on flip-chip layout designed with multiple supply voltage and satisfies the power constraints. The figure 2(b) depicts the customized design flow used in this paper. Firstly, the design is loaded with all the necessary libraries and RTL descriptions in an commercial EDA tool. Secondly, two different analysis is performed on the initial layout they are, (1) IR drop analysis, and (2) Determination of Electron migration affected net.

IR drop analysis is performed on initial floorplan with various P/G pin location. This paper implements a 256 tap FIR filter using the flip chip technology with two supply rails excluding GND pins. The initial floorplan of this design is analysed for various P/G pin locations to determine the optimal co-ordinates of DC source that reduces IR drop in the layout. After identifying the IR drop affected modules in the layout, the proposed methodology is implemented to reduce the IR violations in the design.The resulting floorplan is further allowed to mature with placement of required standard cells of the design; this routes the design and helps to identify the EM affected nets. To reduce the EM violations this paper follows two methods, (1) refining the positions of standard cells and (2) floorplanning the EM affected modules. Method 1: During process of fine tuning the positions of standard cells, the sizing methods like insertion of buffers and changing the drive strength of logic cells are implemented to meet the timing constraint. Thus, this paper also performs static timing analysis bound to a timing constraint.Method 2: The layout consist of some nets belong to modules in the floorplan which suffers from the EM violation. Hence to reduce the EM violation due to those modules, the proposed algorithm performed iteratively to satisfy the EM current limit specific to technology.

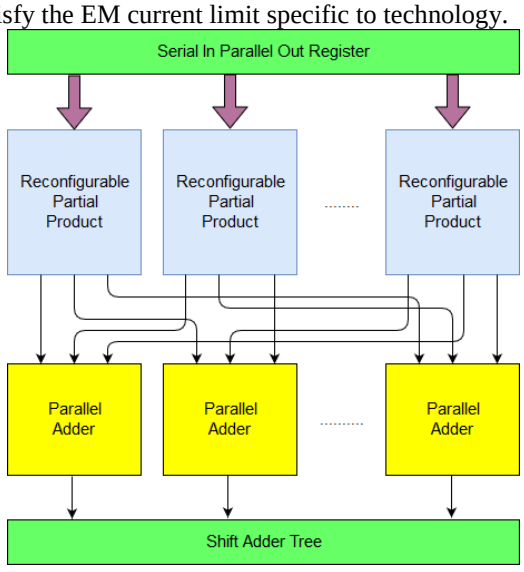


Fig. 3.Block diagram of 256 FIR Filter

B. Design of 256 tap FIR filter layout

In this project a re-configurable 256 tap FIR Filter is implemented with the flip chip design.

The architecture of FIR Filter consists of four main blocks, Serial In Parallel Out Shift Register (SIPOSR), Re-configurable Partial Product Generators (RPPGs), Parallel adders and Shift adders. Instead of memory based LUT, the register array is preferred so as to access the LUT values concurrently and also the contents of this LUT can be updated in parallel to get the required FIR filter. The figure 3 show the block diagram of 256 tap FIR filter. Table 1 shows the experimental results of 256 tap FIR filter. In this table, #VI denote the number of voltage islands. The results show that 17.74% reduction in power after implementation of the flip chip design with MSV methodology , 21.6% reduction in delay. From the table 1, it is observed that increase in voltage island ,increases wirelength to 23.7%. This is due to complexity in placement of standard cells in the layout of the chip. Also, in this table 1, the flip chip results are compared with designs obtained from [14]. It is observed that flip chip design of 256 tap FIR filter shows efficient power saving comparatively. This is due to iterative improvement of the layout and voltage assignment.

Table 1:Experimental results of 256 tap FIR filter using MSV design

#VI	Delay (ns)	Power (mW)	Wirelength (nm)
1	5.801	0.2795	13399.6195
2	4.768	0.1199	16575.8005
2[14]	-	0.2932	-

C. Designing a Flip chip layout

This section assumes that the foot print of design is known, as well as core to die dimension, IO pad dimension, and partition of block in the design.

Assume that an optimal placer exists capable of handling timing optimization, routing, CTS, etc. Now, take this placement of module in the pre-defined layout of flip chip package. The idea behind this paper is to perform this process for low power, less delay, and manage skew in the design with short interconnects. To perform this process for a flip chip requires,

1. Design of bump ball according to the layout of the chip.
2. Topology: Distribution of bump balls in the layout.
3. Introduce redistribution layer between bump ball and IO pads.

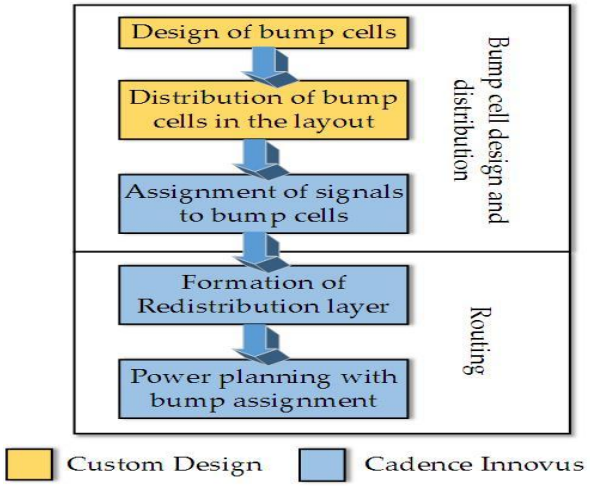


Fig. 4.Flip-chip design flow

The overall design flow is shown in figure 4. Several technology files are required to point (1) above, which is discussed in following subsection . The design consists of more number of IO pads, and two VDD and GND rails. Once this is done, the commercial EDA tool (Cadence Innovus) can be run on this to perform signal assignment(both IO and power lines) on this bump balls based on the location of IO pads. The challenges and technique followed in this paper to solve those problems will be discussed in subsection named RDL routing. This is followed by conventional multiple supply voltage design and result is obtained after a clean a DRC sign-off quality design.

- *Design of bump cell*

For insertion of bump cell as in the figure 5(a), the commercial tool (Cadence) requires script in its library exchange format(LEF) library. Since this paper performs placement of bump cells inside the core area of the layout and number of bump cell depends on number of IOs and V_{dd}, design of suitable size bump cell is a challenge that need to be overcome.

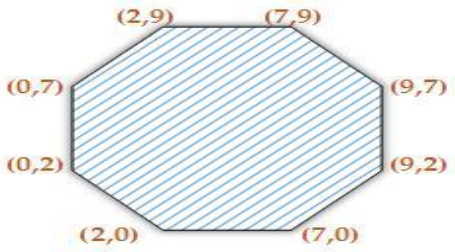
In this paper, through trail and error procedure the bump cells size is customized based on design requirement and its description is written in LEF file. This script is imported during the design import. Figure 5(b) shows the distribution of bump cell used in layout of 256 tap FIR fliter.

- *Topology: Distribution of bump balls in the layout*

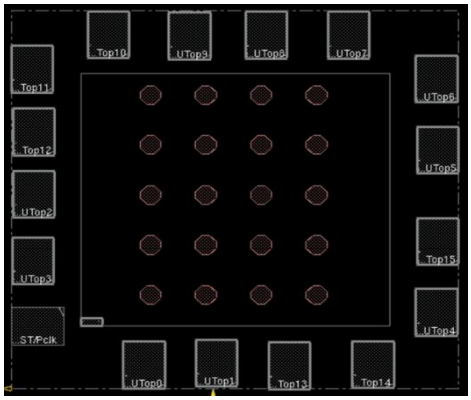
After defining the size of bump cells, it is necessary to distribute these cells according to the number of IO pads and power pins. Usually, bump cells are arranged either in the periphery or core area of the chip. Figure 5(c) show the layout with bump cells distributed in the core area of the chip after signal assignment. In this paper, peripheral IO methodology is used for the distribution of bump cells and arranged in a array fashion.

- *RDL routing*

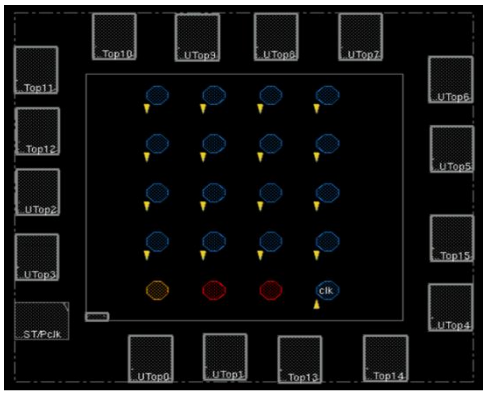
After distribution of bump cells and signal assignments , IO pads present in the periphery are routed to the bump cells using a redistribution layer (RDL). To avoid geometrical violations, cross talk and noise, different metal layers are chosen. The most commonly used routing methods are a) routing at 45°, and b) Manhattan distance. In this paper, both two routing methods are used for efficient routing between the IO pads and bump cells. In addition to these routing methods, to avoid overlap between the metal layers river routing is used in this work. After various iterations, appropriate routing is performed which results in overlap free floorplan. The figure 5(d) and 5(e) shows the 256 tap FIR filter layout with redistribution layer routing and after special routing.



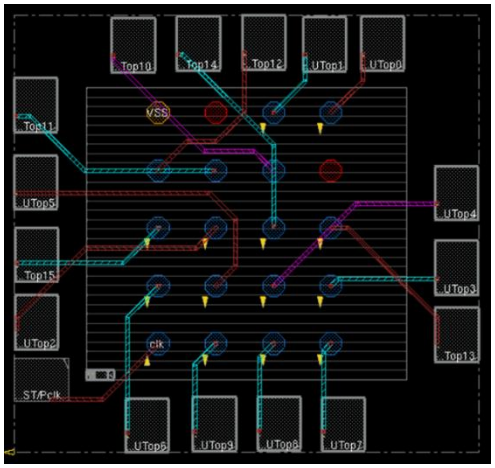
(a) Bump cell structure in flip-chip layout



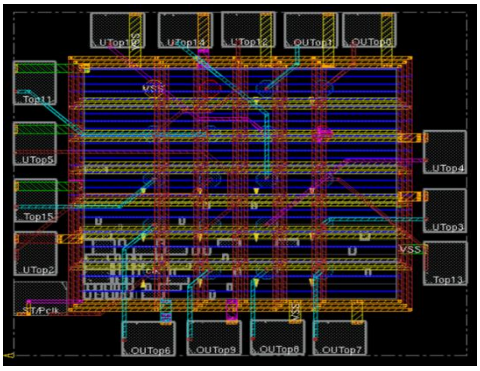
(b) Bump cell in the layout of 256 FIR filter



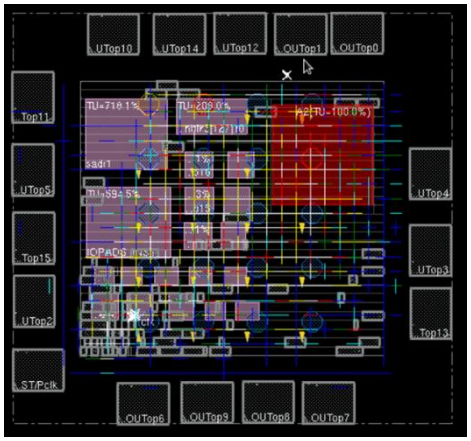
(c) Layout of 256 FIR filter after signal assignment



(d) Redistribution Layer routing in the layout of 256 tap FIR filter



(e) Layout of 256 tap FIR filter after special routing



(f) Initial floorplan of 256 tap FIR filter

Fig. 5.Layout of 256 tap FIR filter with bump cell structure

D. P/G Mesh Generation and network analysis

In modern VLSI chips, mesh structure is widely used for analyzing the P/G network, in order to reduce IR drop effects. Figure 6 shows a power ground network modelled by using resistors and currentsources.

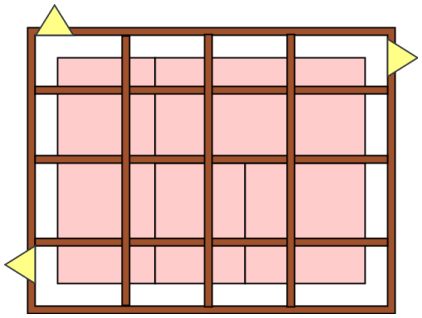


Fig. 6. Power Grid Structure

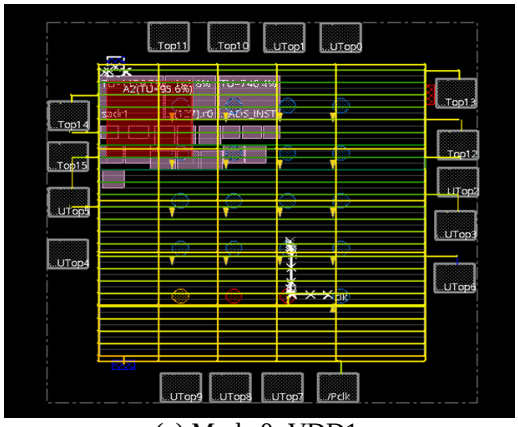
In this paper, commercial tool is used to determine the ir drop of the power grid.Where the ir drop incurs due to the resistance, when the current flows from the modules, thus modules act as a current source.

However, in order to decrease the ir drop, the modules are placed nearer to their corresponding P/G pin. Also the above mentioned task is difficult when it comes to designs with multiple supply voltages. But our method determines the ir drop and updates the location of modules thereby lowering the ir drop and EM violations.

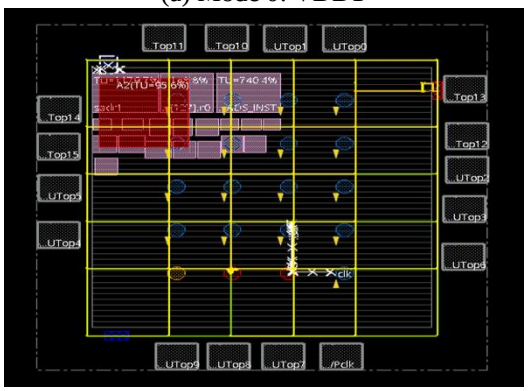
Table 2: Position of P/G Pins

Mode	VDD1	VDD2	VSS
Mode 0	L	R	T
Mode 1	R	T	L
Mode 2	T	L	R

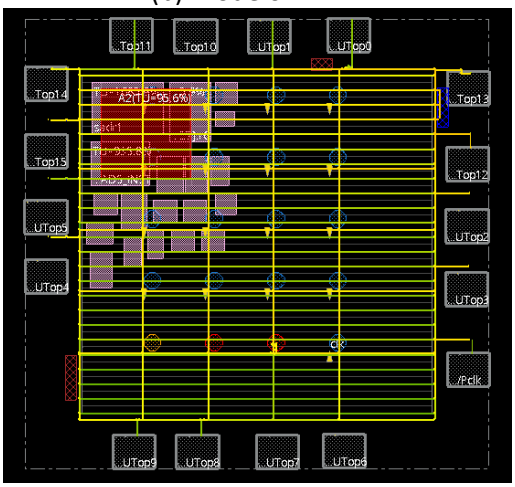
Table 2 describes three modes based on the positioning of P/G pins namely VDD1,VDD2 and VSS, where L,R and T are left, right and top positions respectively. From this, the overall performance of the chip design is checked. The restive networks ofof 256 FIR filter layout for mode 0 and mode 1 are shown in figure 7.



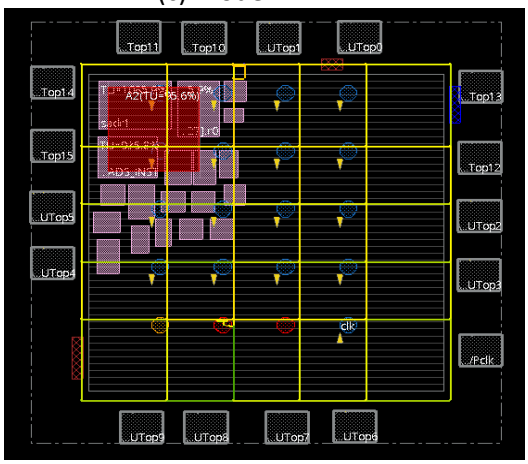
(a) Mode 0: VDD1



(b) Mode 0: VDD2



(c) Mode 1: VDD1



(d) Mode 1: VDD2

Fig. 7.Resistive Network of various Power Mesh

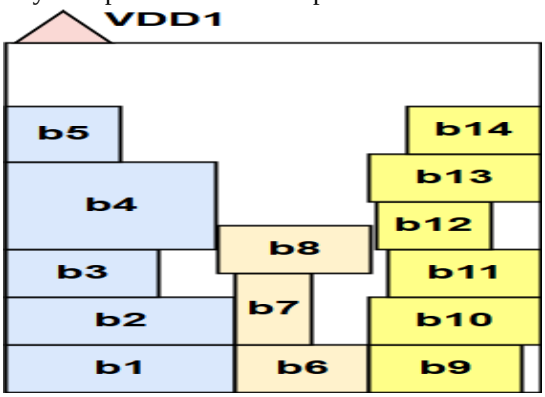
E. Proposed Incremental Floorplanning Methodology

After the signal assignment to the bump cell present in the core area of the layout, modules in the design are floorplanned contiguously based on its voltage assignment. Meanwhile, the proposed methodology in this paper has assumptions over arrangement of modules in the core area of the ICs namely,

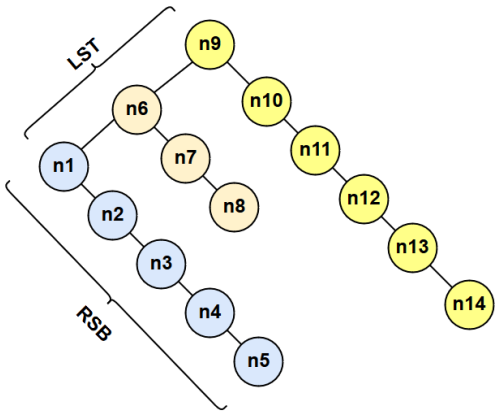
1) P/G pin supplies the required voltage to the modules in the floorplan. To determine the optimal P/G pin location this article assumes a fixed P/G pin location and performs floorplanning to reduce IR drop in the layout.
2) Different from existing works, the 256 tap FIR filter design is implemented on flip chip technology using commercial EDA software. Hence, this paper assumes that EDA software process its intellectual algorithms at the time of calculating wirelength, IR drop affected modules and reporting parameters after routing the design.

- *IR drop reduction methodology*

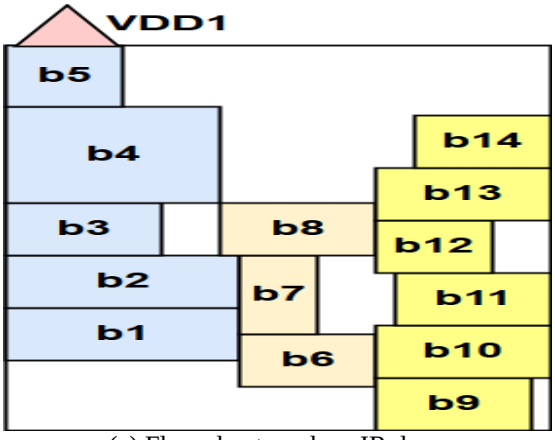
First, the initial floorplan shown in figure 5 is represented using the SKB tree as shown in figure 8(b). An SKB tree is a skewed binary tree, where the root corresponds to the module in bottom left corner. For admissible placement of modules this tree considers a recursive fashion. The IR affected module is identified using efficient algorithm in the EDA software. Generally, the EDA tool models the power plan structure into a resistive network and uses the equivalent resistance of the metal layers in the power plan. Then, uses modified Kirchhoff current law(KCL) to determine the IR drop in the layout. Since this paper aims to reduce the IR drop in early stages after floorplanning, the rail analysis is performed in static power mode.



(a) Initial Floorplanning



(b) Floorplan representation



(c) Floorplan to reduce IR drop

Fig. 8.Proposed Methodology

Basically, the IR drop is mainly due to the effective resistance present between the module and P/G pin. In this article, proposed approach places the IR affected module close to P/G pin as shown in figure 8(c). Analogously, this placement increases the wirelength and power routing resource. The aforementioned ideology is iteratively repeated to achieve the most favorable result that gives effective reduction in wirelength with the objective of reducing IR drop and improving the performance of the design.

- *Electron migration avoidance*

Following the implementation of presented technique, it is certain to mature the design layout for the placement of standard cells in its synthesized structural netlist. The design undergoes global routing in early mode to verify the presence of Electron migration(EM) affecting nets. As discussed previously, this paper follows a two stage process in reducing these EM violations. They are

First stage: This process evaluates the EM effected nets that are due to placement of standard cells in the layout. Then, it refines the placement through widening the width of net or shortening the long wires in the layout; thus it reduces the EM violations in the layout.

Second stage: This process is based on the EM effect emerging from the modules in the design. This paper repeats the proposed mechanism to reduce these violations due to the modules in the floorplan.

During the iterative positioning in satisfying the power constraints, the modules in the tree structure undergoes basic perturbations essentially,

(a) exchange in the order of module in tree structure, and (b) rotating the module in accordance to position to remove deadspace.

IV.SIMULATION RESULTS

Simulations were implemented on 256 tap FIR filter design with multiple supply voltage using flip-chip methodology in Cadence Innovus. Since the design is synthesized on 90nm technology, voltage assignment is made to the modules in the layout with 1.1V (worst case) and 0.9V (best case). The proposed algorithm and the customized design flow for implementing the design is programmed using TCL script. The following section explains the procedure followed in designing the flipchip for 256 tap FIR filter.

A. A Complete flip chip design

After performing routing with redistribution layer, the commercial tool performs special routing to connect VDD and GND globally across the layout. Followed by special routing, the conventional ASIC design flow for the MSV layout is performed. The following procedures are incorporated in the layout to be the complete flip chip design.

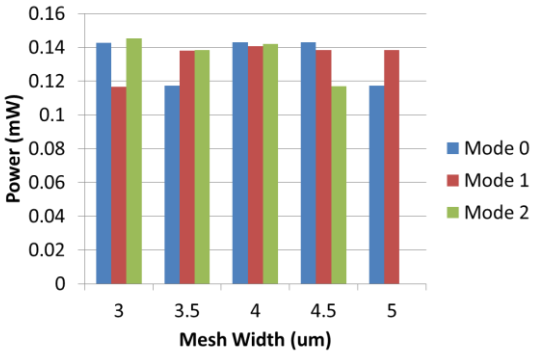
- Step 1: A netlist consisting of macros and standard cells of the design along with technology and timing libraries are loaded to obtain the floorplan for user specific aspect ratio. This gives initial floorplan with modules placed outside the core area of the chip.
- Step 2: Based on the operating voltage levels of the modules, the floorplan follows a tree representation to perform voltage island floorplanning. Using depth first search algorithm (DFS), modules of voltage island are positioned in the core area of the chip within the pre-estimated width.
- Step 3: A Common Power Format (CPF) file is committed which elaborates the operating voltages of the modules in the design. Figure 5(f) shows the floorplan after CPF for the 256 tap FIR filter.
- Step 4: Standard cells present in the design are placed in the layout. Then trail route is performed for analysis of timing.
- Step 5: Static timing analysis is performed to avoid negative slack time. Buffers of required driving strength are inserted for positive slack time.

B. Result for determining optimal mesh structure in 256 tap FIR filter layout

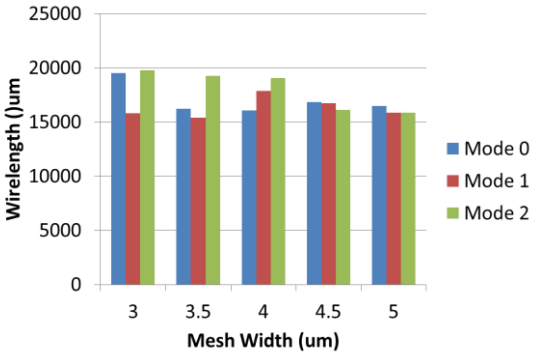
In this section, an experiment is performed to determine the optimal mesh structure satisfying the power constraints. Given a mesh width, the P/G pins of the designs are located in three different modes as discussed in the sub section III (d) and the proposed methodology is implemented on the layout. The fixed mesh width are 3.0 um, 3.5um, 4.0um, 4.5um, and 5.0um respectively. The parameters like IR drop, EM violations, wirelength and metal coverage are evaluated through simulation using commercial EDA tool. The table 3 shows the simulation results for various mesh width with different mode of operations.

Table 3: Simulation Results of proposed algorithm on 256 tap FIR Filter using flip-chip technology consisting of two voltage islands

Mesh Width	Mode	#IR Drop	#EM Viol.	Power (mW)	WL (um)	%M_{cov}
3.0 um	0	0	23	0.1425	19524.86	0.2760
	1	0	0	0.1166	15795.3925	0.2776
	2	0	0	0.1452	19766.5559	0.2771
3.5 um	0	0	19	0.11732	16192.99	0.3189
	1	0	0	0.138	15399.231	0.3250
	2	0	17	0.1384	19228.16	0.3392
4.0 um	0	0	39	0.1431	16052.83	0.3563
	1	0	32	0.1407	17841.1125	0.3540
	2	0	0	0.1420	19037.27	0.3575
4.5 um	0	0	0	0.1431	16836.96	0.3934
	1	0	0	0.1384	16745.77	0.3983
	2	0	0	0.1168	16108.55	0.3969
5 um	0	0	37	0.1172	16456.43	0.1172
	1	0	0	0.1384	15861.04	0.1384
	2	0	0	0.1425	15861.042	0.1425



(a)

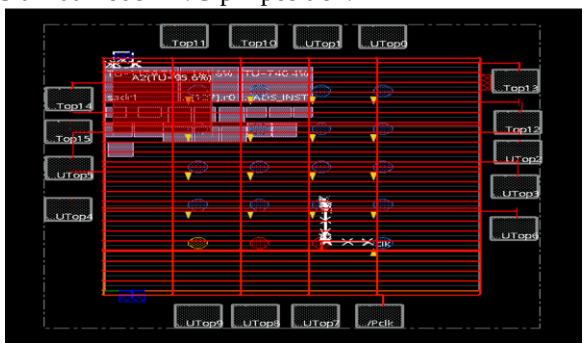


(b)

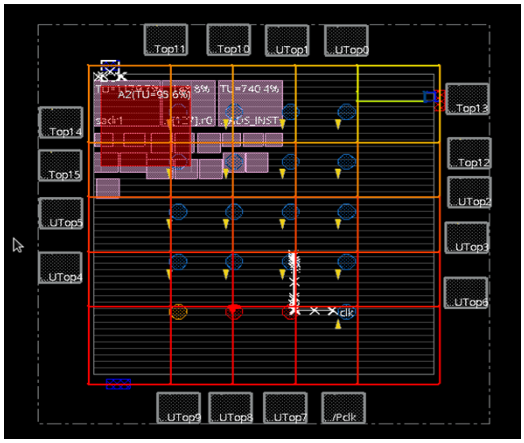
Fig. 9.Effects on Variation of mesh width in (a) power (b) wirelength

Finally this article determines the optimal mesh structure from the table 3 based on the mesh width that gives low power and wirelength along with objective of fulfillment of power constraints.

Theplots in figure 9 helps to determine this optimal solution. It shows the variations on wirelengthand power in the layout for different power mesh width during power planning. It is evident that the mesh width of 5 um in mode 2 P/G pin assignment provides reduction in power and wirelength, in addition to minimizing the IR drop and EM violations. The figure 10, 11 and 12 shows locations of IR drop and EM violations in layout of 256 tap FIR filter operated at different modes. Even though, the proposed floorplanning methodology reduces IR drop and EM violations on different P/G pin positions , it gives optimal performance on 5 um at mode 2 P/G pin position.

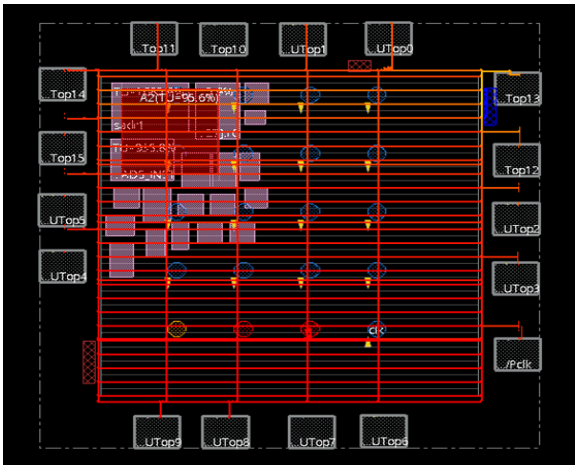


(a) VDD1

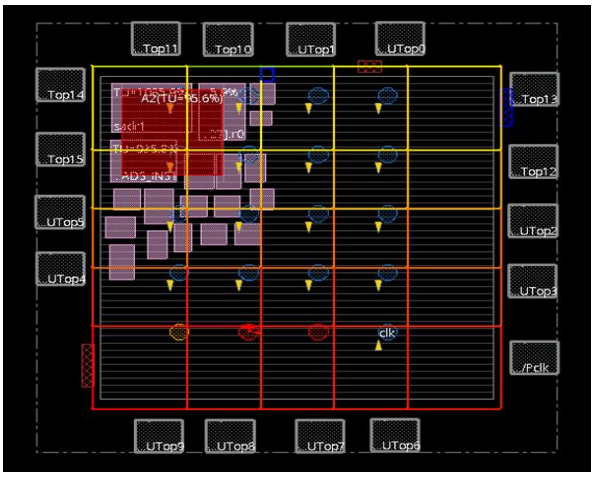


(b) VDD2

Fig. 10. Mode 0 IR Drop

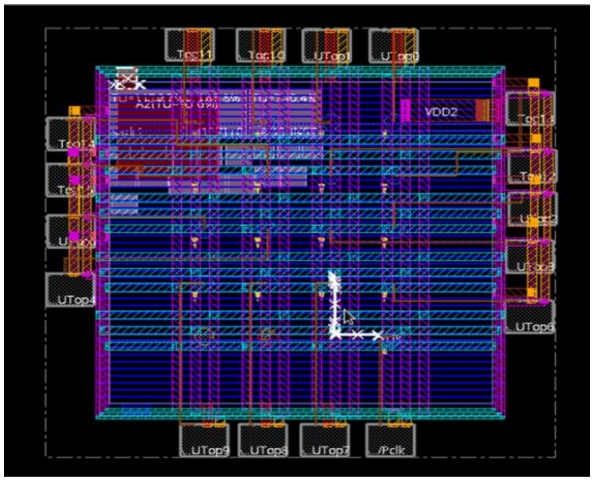


(a) VDD1

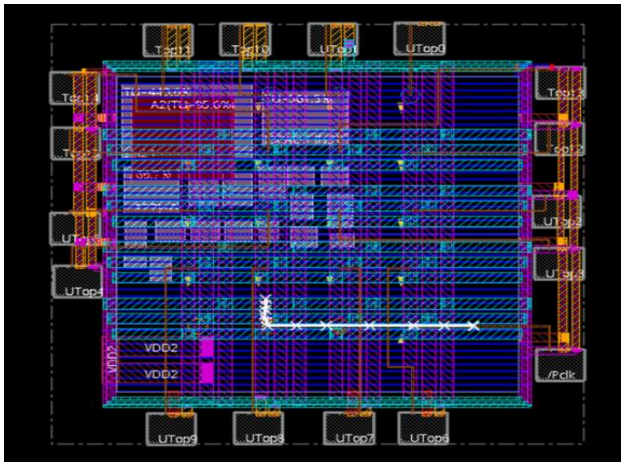


(b) VDD2

Fig. 11. Mode 1 IR Drop



(a) Mode 0



(b) Mode 2

Fig. 12. EM Violations

V.CONCLUSION

This work presents a floorplanning technique in satisfying the power constraints in multiple supply voltage designs. The proposed approach is implemented on flip chip design layout which functions as FIR filter. To determine the optimal power mesh width with the objective of reducing IR drop and EM violations, simulations were performed on the layout for various P/G pin locations for different sizes of power mesh. Simulation results conclude that the proposed ideology gives optimal P/G position along with accomplishment of the necessary power constraints.

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