OPEN ACCESS
International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-8, Issue-1, May 2019

Ordinary and Extraordinary Leakage Suppression Techniques for the Designing of SRAM Sense Amplifiers

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Abstract: In present paper ordinary and extra ordinary techniques have been implemented in 180nm technology gpdk using Cadence virtuoso tool. Current century, the development of microprocessors is a challenging issue due to high power consumption. This high power consumption generally depends on static power and dynamic power consumption but in today scenario leakage power dissipation participate an important role in high power consumption. Memory contains a wide area of microprocessor that means leakage power consumption will be more in memory. In proposed work, it has been observed that the current sense amplifier consume 79% less power as compare to charge transfer and 56% less power as compare to the high speed sense amplifier. Furthermore, it has been found that Row by Row Voltage Approach for Leakage Power Reduction technique reduces the leakage power dissipation up to 99 percent in current sense amplifier and high speed sense amplifier. In charge transfer sense amplifier triple stack technique reduces the leakage power dissipation up-to 99 percent. In Extraordinary leakage power reduction technique leakage current can be measure using leakage sensor in the range of 10 nA to 1µA. Due to this technique required area of memory reduces up to eight percent.

Index Terms: Extraordinary Leakage Power Reduction Technique (ELPRT), Footer Stack Technique (FST), Modified Body Biasing Technique (MBBT), Power Gating Techniques, Row by Row Voltage Approach for Leakage Power Reduction (RRVALPR), SRAM System With Proposed Adiabatic Driver Circuit (SSWPADC).

I. INTRODUCTION

Highlight Now a day's for VLSI circuit designer's leakage power dissipation become an important issue due to small feature size of transistor [1]. Memory contains an almost 70 to 80 percent area of a microprocessor which results in utilization of more number of transistors and therefore leakage power dissipation is proportionally increase with number of transistors count. Basically, there are two types of power dissipation in digital circuit the first one is known as dynamic power and second one is static power [2]

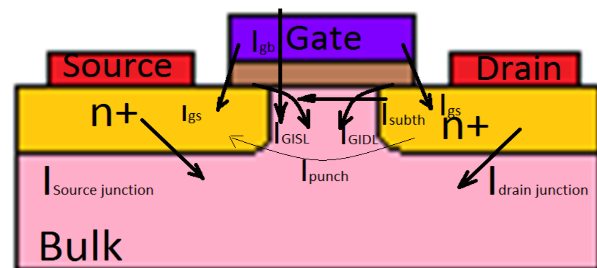

Fig.1. Conventional MOSFET with Leakage Current paths

The dynamic power dissipation occurs due to charging and discharging of capacitor in the circuit which is almost 50 to 90 percent or more for a single chip power dissipation. Static power dissipation or also called leakage power dissipation is of various types such as channel punch through, sub threshold leakage and gate oxide leakage. Sub threshold leakage occurs between the drain and source in MOSFET when the applied voltage is slightly smaller than threshold voltage which result the flow of unwanted small leakage current in channel. For high performance devices the thickness of insulating layer between the channel and gate reduces which results to decrease in insulating barrier potential of the transistor. In this case, when positive voltage applied at gate side of MOSFET some electrons penetrate the insulating layer which provides the current in the oxide layer called tunnelling current. In Punch through effect depletion layer between the source and drain merge to each other which result a high current flows which is undesirable due to increasing drain to source voltage V_{DS}. Leakage power consumption can be minimized by using ordinary leakage reduction techniques such as power gating which do not provide a direct connection between power supplies V_{DD} to ground [3]. There are other types of leakage power dissipation occurs in digital circuits due to random connection between the supply voltage V_{DD} and ground. These types of leakage power dissipation cannot be reduced by ordinary power gating techniques. Therefore, author proposed two new techniques named as extraordinary Leakage power reduction technique and row by row supply voltage technique or column by column supply voltage technique for the minimization of leakage power.

Revised Manuscript Received on 30 May 2019.
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II. PROBLEM STATEMENT

In proposed work, ordinary and extra ordinary leakage suppression techniques have been implemented in SRAM sense amplifier circuit to minimize the leakage power dissipation. Sleep transistor approach [3] is one of the common approaches for leakage power reduction but it increases the delay and area. It also destroys the state when the transistor is in inactive mode. Forced stack technique [3] is another approach which saves the state but increases the dynamic power consumption. Sleepy stack technique [6] proposed by combining these two a previous technique which saves the logic state and minimizes leakage power dissipation but it is slower approach with area trade-off. In Sleepy keeper approaches [6] propagation delay and static power performances are comparatively better than previous approaches. However, this approach has some trade off in terms of area and dynamic power dissipation. Therefore, it's a major challenge to minimize power dissipation with minimum possible delay and area trade off. Author proposed new methods to achieve an excellent trade off in terms of area, power and delay [5].

III. LITERATURE SURVEY

In this section previously mentioned approaches have been closely examined. Leakage power reduction techniques can be categorized into two groups named as state destructive and state saving.

a) Sleep Transistor Approach:

It is the state damaging technique which cut off the pull up or pull down or both the transistors from supply voltage and ground using pull up and pull down side sleep transistors approach. Sleepy transistor inverter circuit is shown in fig. 2

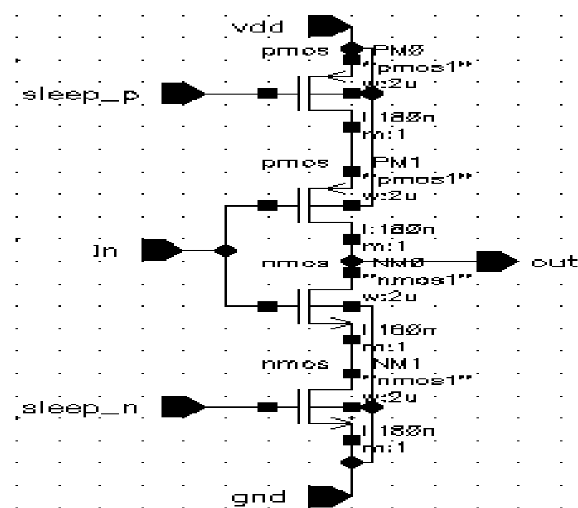


Fig.2. Sleep Transistor Approach with inverter circuit

In this approach we gated the supply voltage V_{DD} called as gated V_{DD} or gated the ground called as gated ground. In this case logic circuits use the low threshold voltage transistors to maintain the fast switching speed. When the logic circuits are not in use at that time sleep transistors remains turned off. During the sleep mode sleep transistor technique drastically reduces the leakage power dissipation by isolating the logic circuits from supply and ground. But at that time it lose the state during sleep mode because pull up and pull down network have floating values which affects the wake up time and energy dissipation of the sleep transistor. Also the sleep transistor trade off the area and delay [9].

a) Forced Stack Approach:

In this technique by stacking the transistor sub threshold leakage current can be reduce. Two or more transistors can be turned off together by the impact of stacking the transistor. Forced stack inverter circuit is shown in fig. 3.

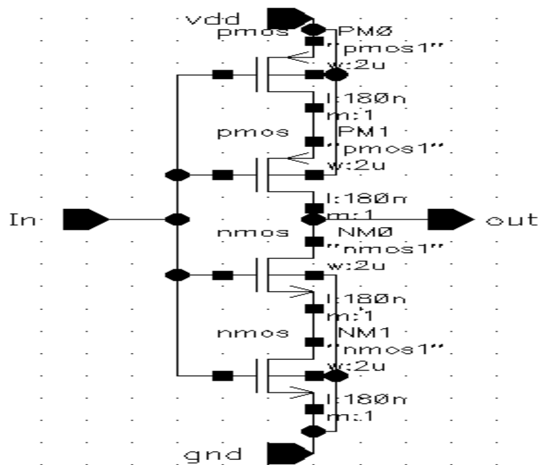


Fig.3. Forced Stack Approach with inverter circuit

Two pull up transistors and two pull down transistors are used in the case of forced stack inverter. In the forced stack circuits all inputs share the same input. If the input is '1' then both NMOS transistors are turned on together and at the same time both PMOS transistors are turned off together. V_A is the intermediate voltage between the two PMOS transistors and V_B is the intermediate voltage between the two NMOS transistors. PM0 and NM1 transistor has its internal resistor so due to this resistance V_A is less than supply voltage and V_B is greater than ground voltage. These voltages V_A and V_B reduces the drain to source voltage (V_{DS}) so due to this effect drain induced barrier lowering (DIBL) effect reduces. Forced stack approach saves the current state when the circuit is in off mode because all transistors get the same input. In forced stack inverter we cannot use the high V_{TH} transistor because its increases the delay in the circuit [8].

b) Sleepy Stack Approach

In Sleepy Stack approach sleep transistor approach and forced stack approach both are combining together. So this approach named as sleepy stack approach. Sleepy stack inverter circuit is shown in fig. 4.

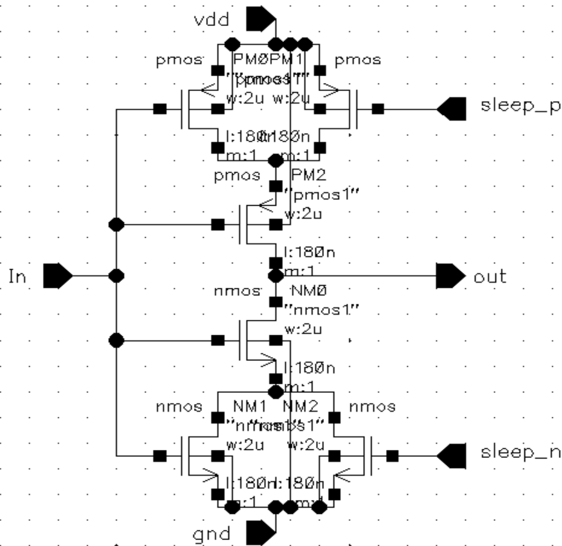


Fig.4. Sleepy Stack Approach with inverter circuit

The sleep transistor and stacked transistor are parallel to each other in each circuit. In sleepy stack approach the working of sleep transistor is same as the working of the sleep transistor in the sleep transistor approach. In active mode sleep transistor remains turned on while in sleep mode sleep transistor becomes turned off. The circuit delay can be reduced by using sleepy stack approach [4]. There is always current flow in the circuit because of sleep transistor is turned on. So its switching speed will be faster as compare to the forced stack approach. For the sleep transistor and its parallel transistor high V_{TH} transistor can be used without incurring the higher delay in the circuit. The delay time is little bit increases but it reduces the leakage. Both the sleep transistors remains turned off but the exact logic state is maintained by the sleepy stack approach. Both the high V_{TH} transistors and stacked transistors reduce the leakage power dissipation. So the sleepy stack approach maintain the exact logic state with low leakage power consumption but it also results to increase in area trade off [11].

c) Sleepy Keeper Approach

In CMOS design, PMOS transistors are placed at the pull up network and NMOS transistors are placed at the pull down network. PMOS transistors are not efficient to passing ground and NMOS are not efficient to passing the V_{DD}. So in sleepy keeper approach one NMOS is connected at the pull up and its gate is connected with the output. In addition to that one sleep transistor is also connected in parallel. Same as one PMOS is connected at pull down side and its gate is connected with the output. One NMOS sleep transistor is connected in parallel with the PMOS transistor. Sleepy Keeper inverter circuit is shown in fig. 5.

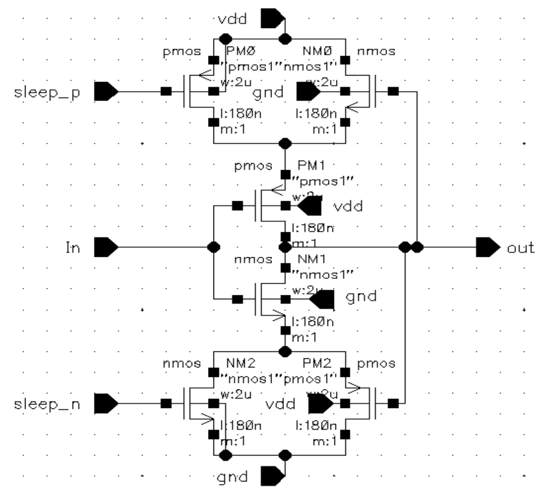


Fig 5. Sleepy Keeper Approach with inverter circuit

To maintain the logic '1' in sleep mode and assuming this value has already calculated. The sleepy Keeper circuit shown in fig 5 use this output value. So the NMOS transistor maintains output value of '1' at the time of sleep mode because in pull up network the NMOS transistor is the only source of supply voltage V_{DD}. Same as in pull down circuit PMOS maintain the output '0' when the assumed output voltage is '0'. In this approach delay is less than the sleepy stack approach. This approach save the state and its leakage power dissipation is also less. However, this approach has comparatively more dynamic power dissipation.

d) Dual Sleep Approach

In this approach one NMOS transistor used in pull up side and one PMOS transistor used in pull down side. Dual sleep approach based inverter circuit is shown in fig.6.

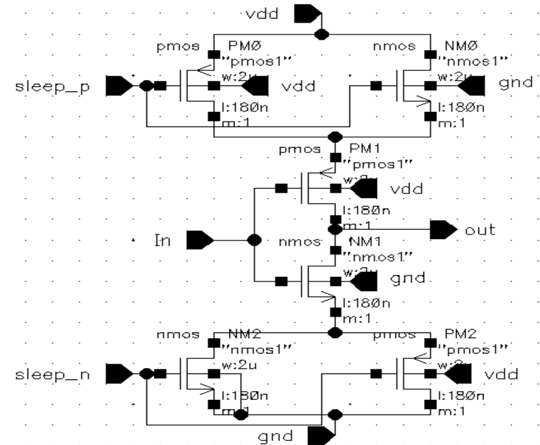


Fig.6. Dual Sleep Approach with Inverter Circuit

One of the sleep transistor will be turn on i.e. either NMOS or PMOS for on the state. Both PMOS and NMOS reduce the leakage power dissipation in off state. In this approach leakage power dissipation reduces by dual threshold voltage. It also reduces the delay and saves the state. [9]

Proposed Approaches

a) Modified Body Biasing Approach

In proposed approach two sleep transistors have been used in both pull up and pull down side as shown in fig 7. Both the transistors are in parallel. In pull up network, first PMOS transistor body is connected with the body of the second PMOS transistor. So the body biasing effect is created in first transistor. This effect increases the threshold voltage V_{TH}. Same as in the pull down network due to NMOS transistors this effect is created. So due to modified body biasing approach leakage power reduces due to sleep transistors and body biasing effect. For maintaining the logic state one NMOS is connected in pull up side and one PMOS is connected in pull down side. These transistors are connected with the output.

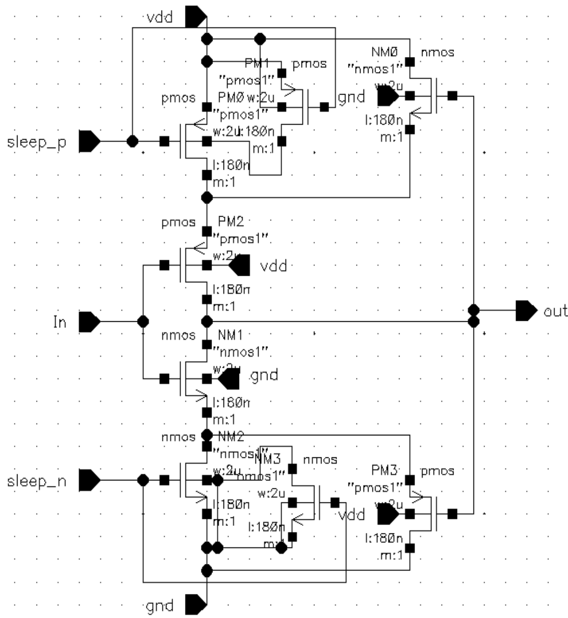


Fig.7. Modified Body biasing technique with Inverter Circuit

a) Single (One PMOS or One NMOS), Dual and Triple Stack Technique

In this proposed approach only one PMOS transistor is applied in footer side in place of dual stack approach. It reduces the leakage power drastically as compare to dual stack approach and also requires less area. One another approach is dual stack approaches in which replace transistor the stack gate one PMOS transistor to one NMOS and remaining part of the circuit remains same. In this approach operating speed of the circuit is more and its area is also less compare to the dual stack approach.

b) Extraordinary Leakage Power Reduction Technique

In microprocessor the main components are main memory, cache memory and buffer memories. Power consumption is almost negligible in off state of MOSFET circuits in standby mode so it improves the life of the battery. But in memories standby current increases exponentially because the defect creates due to dust and process variation in the circuit. This type of leakage power dissipation is called extraordinary leakage power dissipation. Many approaches are available for repairing device defects but no existing technique was reported to eliminate such device defects. SRAM memory cell with different paths and defects in standby mode called extraordinary leakage which is shown in fig.8.

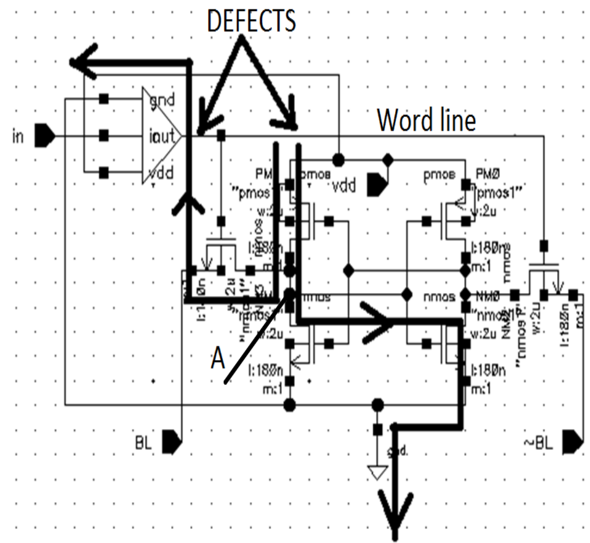


Fig:8 Diagram of Extraordinary leakage current path from a V_{DD} line to ground

In this circuit leakage current flows due to node A and word line which are shortly connected due to gate oxide defect. Extraordinary leakage power reduction technique (ELPRT) is introduced for eliminating these types of defects. This approach or technique is divided into three parts which is shown in fig 9.

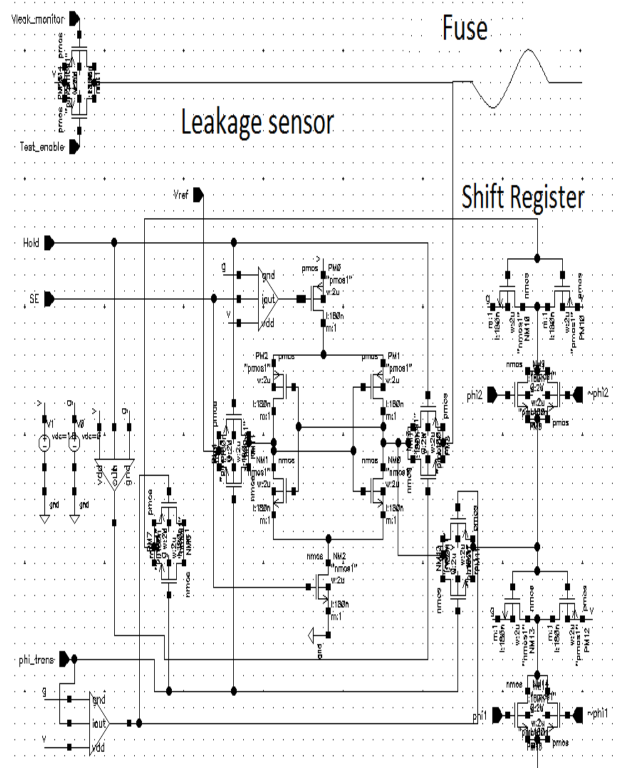


Fig:9. Diagram of Extraordinary leakage shift register and current sensors

First part is use as leakage current sensor for supervising the quantity of leakage current of V_{DD} line pair and each cell bit line. According to amount of leakage current each sensor senses either the output zero or one. If the sensor output is high that means the extraordinary leakage current is in line of sensor. Using V_{REF} and $V_{LEAK_MONITOR}$ sensitivity of leakage sensor can supervise and tune. Second part of circuit consist of two shift registers which are used for detecting the location of rows and columns on which path extraordinary leakage current has to be measured. One shift register is placed in row direction and one shift register is placed in column direction. The accompaniment output from sensor is transfer to shift register and subsequently transfers to the external tester. Fuses are used in third part of the circuit for disconnecting the leakage current path. A fuse is applied in each cell bit line and V_{DD} line. When the fuse fluttered which disconnect the supply voltage V_{DD} from bit line. Hence the supply voltage V_{DD} isolates from memory. Bit cells with standby leakage error and blown fuses error can be improve by extraordinary leakage power reduction fuses. These blown rows and columns are replaced by spare connected rows and columns.

c) Row by Row Voltage Approach for Leakage Power Reduction

DIBL effect is the one of the important phenomenon in short channel MOSFET. Leakage power can be eliminate by using this effect. In this case decrease in drain to source voltage V_{DS} result increase in potential barrier near to source. So in this case compare to high V_{DS} the leakage current decreases almost 10 percent. In CMOS circuits when the supply voltage V_{DD} decreases irrespective of change in V_{TH} voltage that result to decrease in leakage power due to this DIBL effect. A row by row voltage approach for Leakage power reduction is proposed which is shown in fig.10. Both V_{DD} line and word line are activated when the one row is access. One design consideration has taken under consideration i.e. if pass gate of the cell turned on those two nodes store the data in the cell. So in this condition memory cell behave as load resistor.

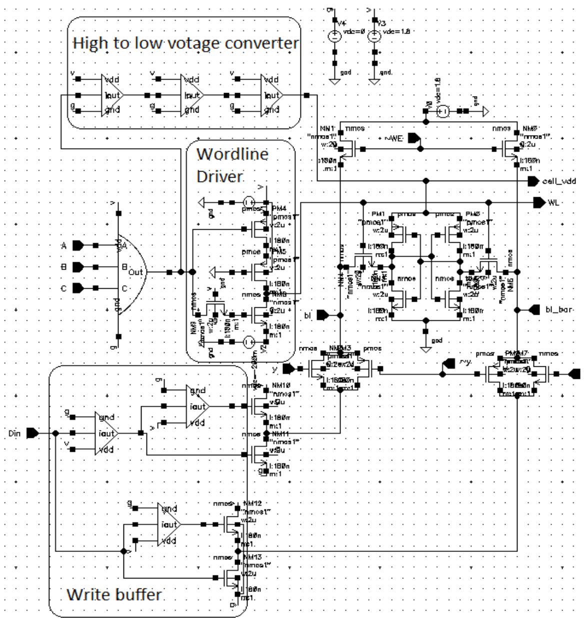


Fig: 10. Diagram of Row by Row Voltage Approach for Leakage Power Reduction.

d) SRAM System With Proposed Adiabatic Driver Circuit

Energy loss occurs due to charging and discharging of bit lines during write operation is considerable. In write operation for 1 to 0 transitions corresponding bit line discharges to ground. This energy loss can be minimized by reducing the discharge time with controlling the bit line voltage.

For this purpose new proposed adiabatic driver circuit is shown in fig 11.

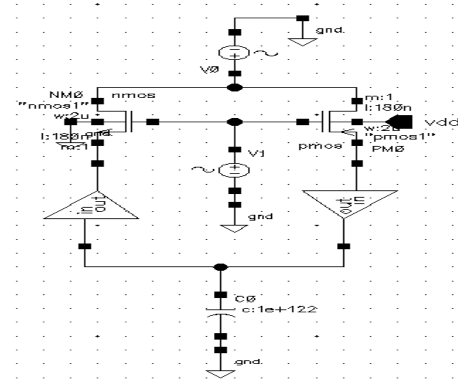


Fig.11. Proposed Adiabatic driver circuit

In proposed driver circuit two supply voltages and two inverters are used which are connected in back to back position.

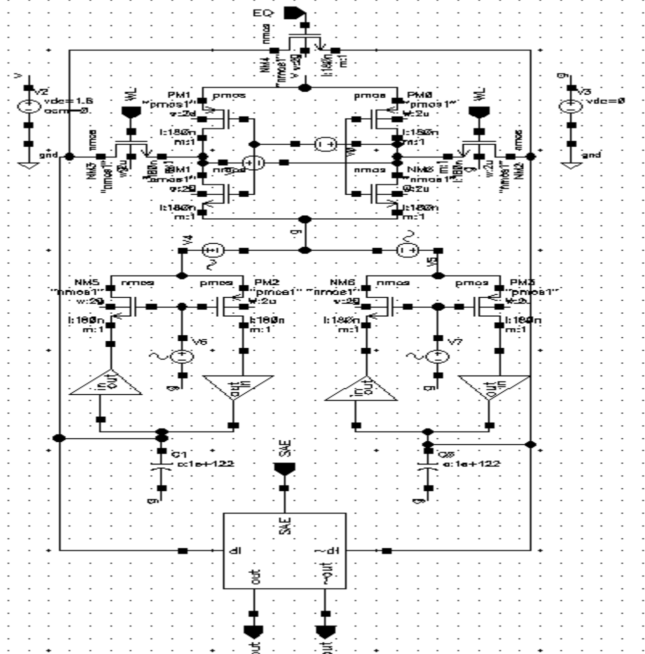


Fig: 12. SRAM system with proposed Adiabatic driver circuit

Design Approaches

The existing techniques and proposed techniques have been implemented in three different types of sense amplifiers for reducing the various types of leakage current in sense amplifier circuits.

a) Current Sense Amplifier

In current sense amplifier bit bar line and bit line are pre-charge to V_{DD}. Due to SAEN connect to V_{DD} output of sense amplifier is also pre-charge to V_{DD}. Before generates the full swing differential voltage output nodes SAOUT and SAOUT bar are initially pre-charge. Current sense amplifier circuit diagram shown in fig 13. [12].

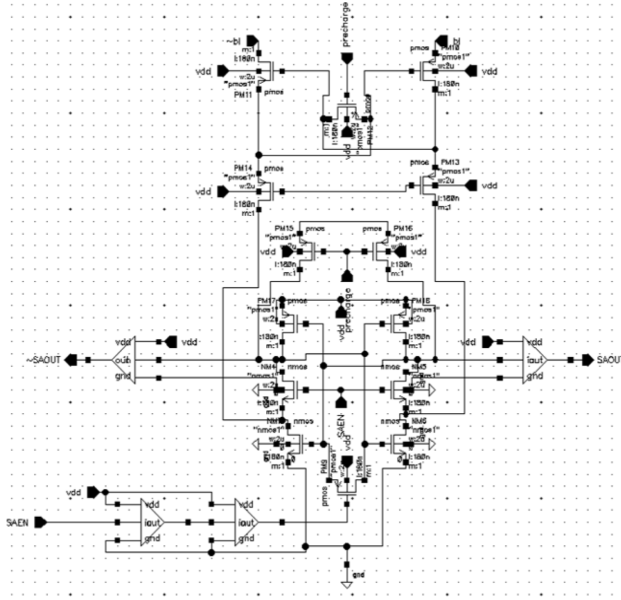


Fig:13. Current Sense Amplifier Circuit Diagram

b) Charge Transfer Sense Amplifier

In charge transfer sense amplifier bit bar line and bit line and Y_{SELECT} are pull up to V_{DD} and pre-charge pull down to V_{SS} and this input is applied for pre-charge phase. Charge transfer sense amplifier circuit diagram shown in fig 14. [12].

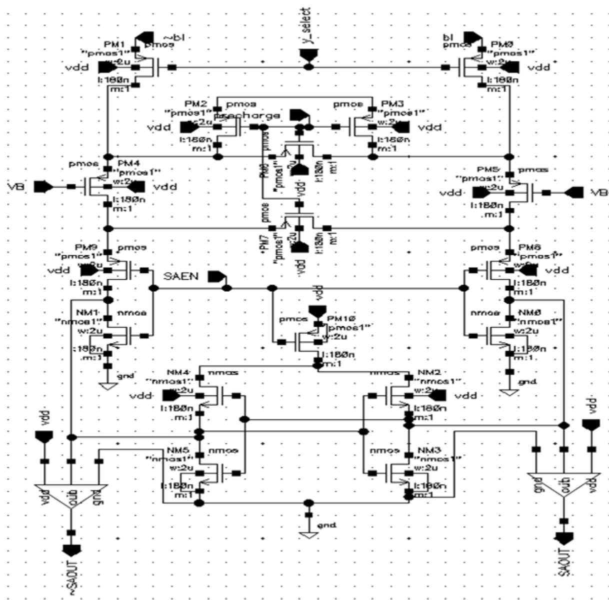


Fig:14. Charge Transfer Sense Amplifier Circuit Diagram

c) High Speed Sense Amplifier

OUT and OUT BAR set to V_{DD} and pre-charge phase SAEN pull down to V_{SS} in high speed sense amplifier. SAEN input pin pull up to V_{DD} for sensing mode of operation. High speed sense amplifier circuit diagram shown in fig. 15.

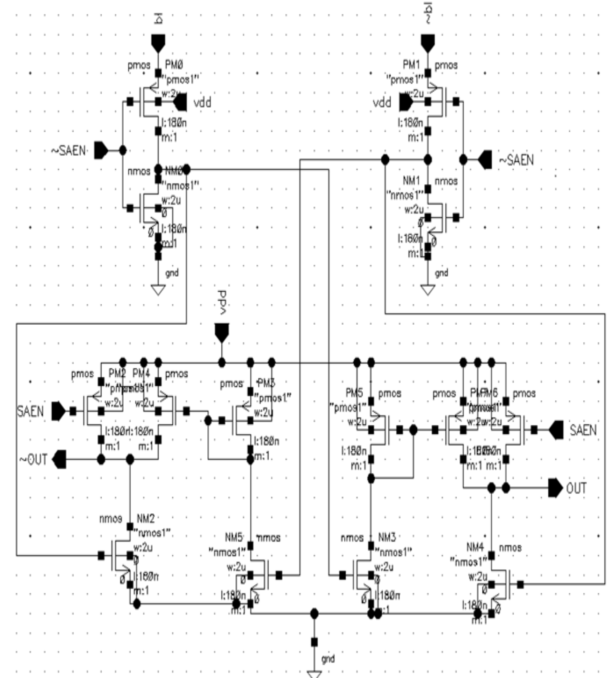


Fig: 15. High Speed Sense Amplifier Circuit Diagram

IV. RESULT ANALYSIS

In proposed work current sense amplifier, charge transfer amplifier and high speed sense amplifier have been implemented and analysed in terms of power dissipation. Current sense amplifier has been kept in active mode which provides less power dissipation as compare to in saturation mode.

I. SENSE AMPLIFIERS AND ITS POWER CONSUMPTION

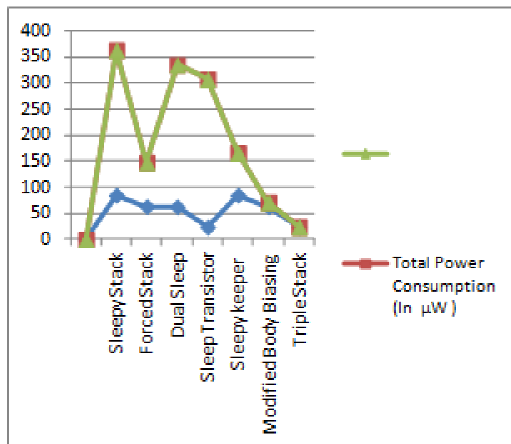
Different Sense Amplifiers	Power Consumption (In µW)
Charge Transfer Sense Amplifier	***2397***
Current Sense Amplifier	***379.6***
High Speed Sense Amplifier	***911***

It has been observed that power consumption in current sense amplifier is 79% and 56% less as compare to the charge transfer and high speed sense amplifier respectively [12-14].

V. Total Power And Leakage Power Consumption For Current Sense Amplifier

Approaches	Leakage Power consumption (In pW)	Total Power Consumption (In µW)
Sleepy Stack	*85.27*	*278.51*
Forced Stack	*63.56*	*84.50*
Dual Sleep	*63.08*	*272.29*
Sleep Transistor	*24.07*	*284.01*
Sleepy keeper	*85.30*	*81.6*
Modified Body Biasing	*63.08*	*8.05*
RRVALPR	*0.4332*	*5.11*
Triple Stack	*23.2*	*0.0666*

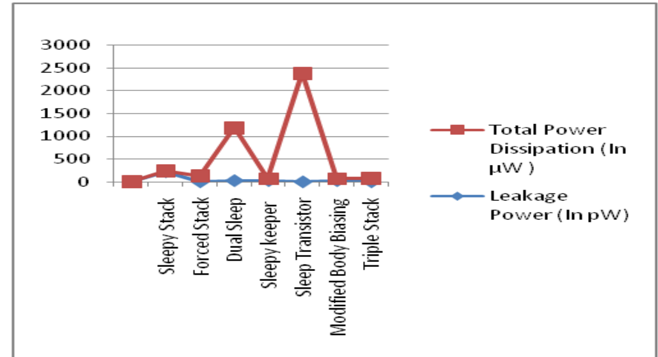
All the previously reported techniques and proposed techniques have been implemented in current sense amplifier. The obtained results are summarized in the form of table II. It has been found that modified body biasing technique consume less leakage power i.e. 26% and 0.75% as compare to sleepy stack and forced stack approaches respectively. However, it is 61% higher than sleep transistor approach. Furthermore, it is interesting to note that triple stack approach have 60.2%, 61.9% and 72% less leakage power consumption compare to modified body biasing, sleepy stack and forced stack approach respectively. Total power dissipation in modified body biasing technique is 90% to 95% less compare to forced stack, sleepy stack, dual sleep, sleep transistor approaches respectively. Moreover, RRVALPR approach reduces the leakage power dissipation 95 to 98% as compare to above existing techniques.



VI. TOTAL POWER AND LEAKAGE POWER CALCULATION FOR CHARGE TRANSFER SENSE AMPLIFIER

Approaches	Leakage Power (In pW)	Total Power Dissipation (In µW)
Sleepy Stack	**218.29**	**26.1**
Forced Stack	**0.0007536**	**133.42**
Dual Sleep	**25.9**	**1161**
Sleepy keeper	**25.9**	**44.49**
Sleep Transistor	**.01447**	**2390.2**
Modified Body Biasing	**27.07**	**44.49**
Triple Stack	**0.00003907**	**79.80**
RRVALPR	**3.929**	**0.468**

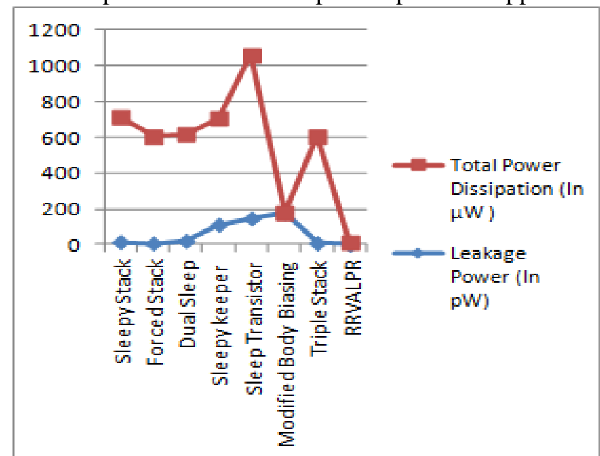
Table III shows the estimated values of power dissipation for all the techniques implemented in charge transfer sense amplifier. Proposed modified body biasing technique leakage power dissipation is 87.6 % less than sleepy stack. Total power dissipation in modified body biasing technique is 98.13%, 66.62%, 90.138% and 96.16% smaller as compare to sleep transistor and forced stack, sleepy keeper approach and dual sleep approach respectively.



VII. TOTAL POWER AND LEAKAGE POWER CALCULATION FOR HIGH SPEED SENSE AMPLIFIER

Approaches	Leakage Power (In pW)	Total Power Dissipation (In µW)
Sleepy Stack	**16.0**	**697**
Forced Stack	**7.877**	**596.11**
Dual Sleep	**21.512**	**596.11**
Sleepy keeper	**112.11**	**596.12**
Sleep Transistor	**147.01**	**912.02**
Modified Body Biasing	**179.12**	**0.325**
Triple Stack	**8.755**	**596.11**
RRVALPR	**0.288**	**12.55**

Estimated values of power dissipation for all the techniques implemented in high speed sense amplifier have shown in table IV. Proposed triples stack technique leakage power dissipation is 94.04%, 46% and 91% less as compare to sleep transistor, sleepy stack and sleepy keeper approach respectively. So proposed modified body biasing technique is much more power efficient compare to previous approaches.



In row by row voltage approach for leakage power reduction (RRVALPR) successfully initially measure and then reduces the leakage by using the DIBL effect.

At 1.8 supply voltage RRVALPR measures the leakage power around 99% percent and reduces the leakage up to the 98.2%. Extraordinary leakage current sensor senses the leakage current and shift register provides the output which is used for removing leakage current path by using fuses. A fuse is used in each cell V_{DD} line and bit line pair. Voltage V_{DD} cut-off from bit line and V_{DD} lines when the fuse blasts which separates the memory from $V_{DD.}$ To minimize the total power dissipation adiabatic driver circuit has proposed in SRAM System. Its power consumption is 386mW which is 3 times lesser than the old driver circuit [15]. It happens due to the driver capacitor charges continuously and drives the bit line and remaining power get back to the supply. This driver circuit power recovery is 19.32nW.

VIII. Conclusion

In present work, main focus has been paid on implementation and analysis of modified and proposed low power reduction techniques such as modified body biasing, extra ordinary leakage power reduction technique, row by row voltage approach for leakage power reduction and triple stack reduction approach in different sense amplifier circuits. it has been observed that the current sense amplifier consume 79% less power as compare to charge transfer and 56% less power as compare to the high speed sense amplifier. Furthermore, it has been found that row by row voltage Approach for Leakage Power Reduction technique reduces the leakage power dissipation up to 99 percent in current sense amplifier and high speed sense amplifier. In charge transfer sense amplifier triple stack technique reduces the leakage power up to 99 percent. Moreover, extraordinary leakage power reduction technique can be applied also in other types of memory circuits. In this approach leakage sensor can measure the current in range of 10nA to 1µA by using voltage comparator. So memory capacity increases due to leakage reduction and required area of memory reduces up to 8%.

REFERENCES

1. Sivaneswaran Sankar, Student Member, IEEE, Ulayil Sajesh Kumar, Mayank Goel, Maryam Shojaei Baghini, Senior Member, IEEE, " Considerations for Static Energy Reduction in Digital CMOS ICs using NEMS Power Gating", IEEE Transaction on Electron Devices, VOL 64,No.3, MARCH 2017.
2. Alberto Macii, Senior Member, IEEE, Enrico Macii, Fellow, IEEE, and Massimo Poncino, Member IEEE, Andrea Calimera, Student Member, IEEE, "Design Techniques and Architectures for Low-Leakage SRAMs", IEEE Transaction on Circuits and Systems, Vol. 59, NO. 9, September 2012.
3. Deepak Mittal and Vigneswaran T. "Leakage Reduction Using Power Gating Techniques in SRAM Sense Amplifiers", ARPN Journal of Engineering and Applied Sciences, VOL. 10, NO. 7, page no. 2994, APRIL 2015.
4. Narendra S, S. Borkar, V. D Antoniadis, and Chandrakasan A. "Scaling of Stack Effect and its Application for Leakage Reduction," Proceedings ofthe International Symposium on Low Power Electronics and Design, pp. 195–200, August 2001.
5. HanwoolJeong, Student Member, IEEE, TaewonKim, Kyoman Kang, TaejoongSong, Gyuhong Kim, Hyo-sig Won, and Seong-Ook Jung, SeniorMember,IEEE, "Switching pMOS Sense Amplifier for High-Density Low-Voltage Single-Ended SRAM" IEEE Transaction on Circuits and Systems—I: Regular Papers, Vol. 62, No. 6, June 2015.
6. J. C. Park, V. J. Mooney and P. Pfeiffenberger, "Sleepy Stack Reduction in Leakage Power," Proceedings of the International Workshop on Power and Timing Modelling,Optimization and Simulation (PATMOS'04), pp.148-158, September 2004.
7. Chris Hyung-il Kim, Jae-Joon Kim, Student Member, IEEE, SaibalMukhopadhyay, Student Member, IEEE and Kaushik Roy, Fellow, IEEE, "A Forward Body-Biased Low-Leakage SRAM Cache Device, Circuit and Architecture Considerations",IEEE Transaction on Very Large Scale Integration (VLSI) Systems , Vol. 13, NO.3, pp. 349–357, March 2005.
8. DavideBaccarin, David Esseni, Senior Member, IEEE, and Massimo Alioto, Senior Member, IEEE, "Mixed FBB/RBB: A Novel Low-Leakage Technique for FinFET Forced Stacks" IEEETransactionsonveryLargeIntegrations(VLSI)Systems,VOL.20,NO.8,AUGUST2012
9. NittaranjanKarmakar, Mehdi Z. Sadi, Md. KhorshedAlam and M. S. Islam1, "A Novel Dual Sleep Approach to Low Leakage and Area Efficient VLSI Design" IEEE-RSM Proc. 2009, Kota Bahru, Malaysia.
10. Johnson, M. Somasekhar, D. Chiou, L.-Y., and K.Roy, "Leakage Control with Efficient Use of Transistor Stacks in Single Threshold CMOS," IEEE Transactions on VLSI Systems, vol. 10, no. 1, pp. 1–5, February 2002.
11. K. Roy, S. Mukhopadhyay, and H. Mahmoodi, "Leakage Current Mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," Proc. IEEE, vol. 91, no. 2, pp. 305–327, Sep. 2003.
12. Manoj Sinha, Steven Hsu, Atila Alvandpour, Wayne Burleson, Ram Krishnamurthy, Shekhar Borhr, "High-Performance and Low-Voltage Sense-Amplifier Techniques for sub-90nm SRAM", *SOC Conference 2003. Proceedings. IEEE International [Systems-on-Chip]*
13. Sampath Kumar, Sanjay Kr Singh, Arti Noor, D. S. Chauhan & B.K. Kaushik, "Comparative Study of Different Sense Amplifiers in Submicron CMOS Technology" International Journal of Advances in Engineering & Technology, Nov 2011.
14. Geeta Pattnaik, Sweta Padma Dash, Komal Priyadarshini, Adyasa Samantaray, Adyasha Rath " Review of Different Sense Amplifiers For SRAM in 180nm Technology" International Journal of Science, Engineering and Technology Research (IJSETR), Volume 3, Issue 5, May 2014.
15. Jianping Hu, Weiqiang Zhang, Yinshui Xia "A Novel Low-Power Adiabatic SRAM with an Energy-Efficient Line Driver" International Conference on Communications, Circuits and Systems (IEEE Cat. No. 04EX914).

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