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Design of New Tester Circuit for Fault Detection

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Abstract: Fault detection plays an important role in detecting faults and helps to reduces the yield loss in manufacturing process of ICs. Due to the smaller size and process variations, IC chips become more sensitive. Thus there is thriving necessity for fault tolerance which can be obtained by an efficient fault detection concept. In this paper, new tester circuit is designed for fault detection using different tester circuits that are existed. This design has been simulated in 180nm, 65nm CMOS technology using cadence Virtuoso tool. By using transmission gates instead of pass transistors the modified circuit provides full swing voltage at output.

Index Terms: Fault Detection, Fault Diagnosis, Fault Isolation, Redundancy Allocation, Tester circuit.

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I. INTRODUCTION

Due to the advancement in VLSI technology billions of transistors are fabricated on a single IC. It becomes difficult to detect the faults. So, the International Technology Roadmap of Semiconductor industries introduce a "self-repair" process as one of the specification in coming years. In this paper, the tester circuit is modified for fault detection.Block diagram of self repair process is shown in Fig.1.The self-repair process contains mainly four steps. In the first step i.e. the fault detection, if faults occurs then the output of the tester becomes "1" and in the fault free condition the output of the tester becomes "0".After the fault detection the second step is fault diagnosis, in this the location of the fault is identified and the output values of the tester toggles from "0" to "1" or "1" to "0". In Fault isolation these faulty cells are isolated. The final step is redundancy allocation, in this the faulty cells are replaced by a redundant one [1].

Fig.2 shows that system diagram of Sensor Instrumentation System-on-Chip (SOC) [2]-[4], which is a Mega gray total ionization dose radiation[5] tolerant system used as an convergence in nuclear applications.In sensor instrumentation system-on-chip the sensors output voltage can be amplify by eight gain instrumentation amplifiers (IAs).To digitalize the output of IAs there are eight delta-sigma ADCs , a clock reference, and voltage reference. The on-chip silicon temperature sensor and thermocouple are used to monitor/control the temperature of SOC.

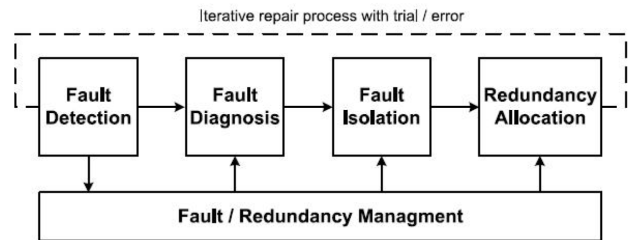


Fig. 1 Self repair process [1]

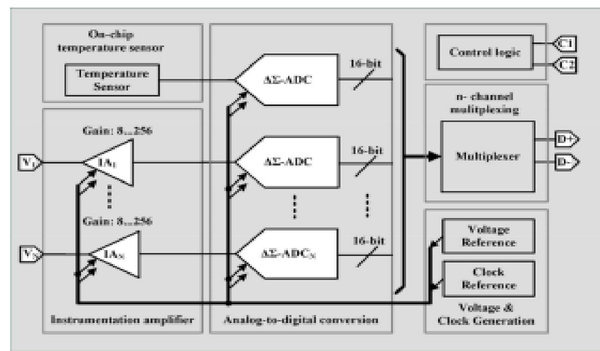
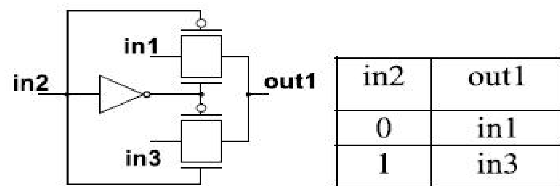


Fig. 2 Sensor instrumentation SOC system diagram [1]

There are different techniques that are used to enhance the constancy of the sensor instrumentation SOC.

A new radiation tolerant delta sigma (ADC) i.e. analog-to-digital-converter was proposed. In this paper existing tester architecture is modified to enhance the constancy [6] of sensor instrumentation SOC in crude environments [7]-[9].



in2	out1
0	in1
1	in3

Fig. 3 Multiplexer using Transmission gates [1]

The 2-to-1 multiplexer with its truth table is shown in Fig.3. The multiplexer is designed by using transmission gates which is used to prefer the desired channel. Here transmission gates are preferred because CMOS gates should be biased to work properly which increases power consumption.

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II. EXISTING TESTER CIRCUITS

To test the functionality of functional unit the tester unit is used i.e. 2-to-1 multiplexer. In this the tester unit consists of a logic unit to get the desired value and a comparator to compare actual output values with the desired values. Here four different tester architectures with their truth tables are given in Fig.4. The tester units consist of the multiplexer designed using transmission gates and pass transistors. In the tester circuits, "in1," "in2," "in3"are the inputs to logic unit and "out1" is the input of the comparator. Here the output of the logic unit and the input of the comparator are compared to get the output. The desired values are compared with actual values to get "output" which is output of tester unit. In this tester circuit the logic unit operation is carried out like the basic 2-to-1 multiplexer which is shown in Fig.3.

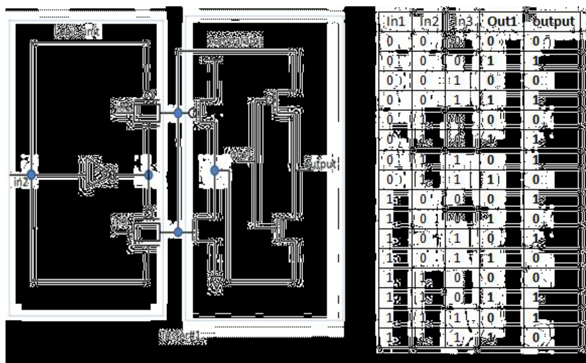
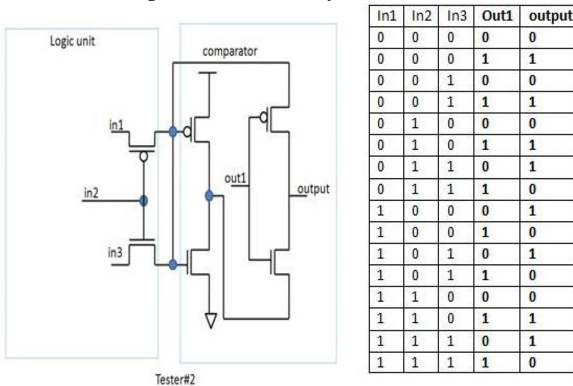


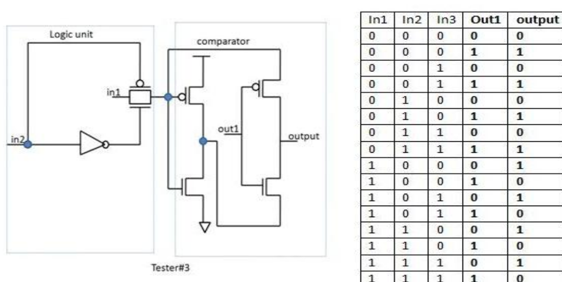
Fig. 4 (a) Tester #1

In Tester#1 the logic unit is designed by using transmission gates which provides 100% accuracy in functional unit testing. In Tester#2, the logic unit is designed using pass transistors which provides accuracy as similar to the Tester#1.



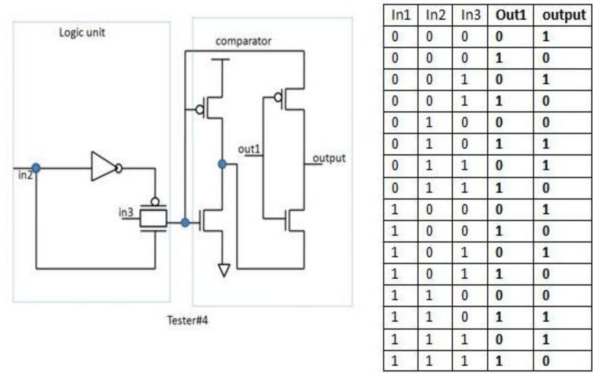
In1	In2	In3	Out1	output
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Fig. 4 (b) Tester #2



In1	In2	In3	Out1	output
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

Fig. 4 (c) Tester #3



In1	In2	In3	Out1	output
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

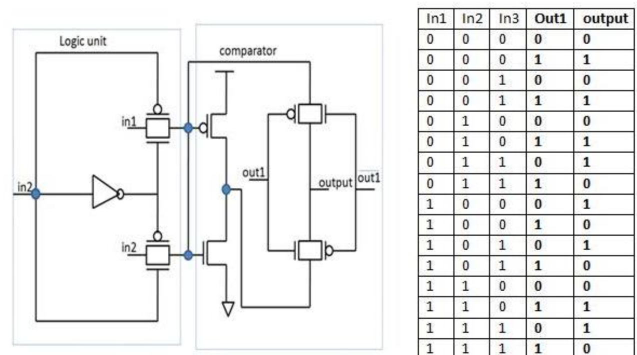
Fig. 4 (d) Tester #4

Fig. 4 Different tester architectures with truth tables [1]

The Tester#3 and Tester#4 are appropriate multiplexers which consists of two inputs instead of three by providing 75% accuracy.

III. MODIFIED TESTER CIRCUIT

The Modified tester circuit with its truth table is shown in Fig.5. In this "in1", "in2", "in3"are the inputs of the logic unit. "out1"is the input of the comparator and "output" is the output of the tester unit. Due to the worst output voltage swing shown in Fig.6, the existing tester circuit (Tester#1) shown in Fig.4 is modified by replacing the two transistors at the comparator with transmission gates which is shown in Fig.5.



In1	In2	In3	Out1	output
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Fig. 5 Modified Tester circuit with truth table

In existing tester circuit i.e. Tester#1 the full output voltage swing occurs only at 0111,1000,1001,1011and in Tester#2 the full output voltage swing occurs at 1001,1010,1011 .In the Tester#3 the full output voltage swing occurs at 101,100 and in Tester#4 the full output voltage swing occurs at 111. The advantage of the modified design gets the full output voltage swing at all the values shown in Fig.10.

IV. SIMULATION RESULTS

The results of the modified tester circuit are simulated in 180 nm, 65nm CMOS technology using cadence virtuoso tool.

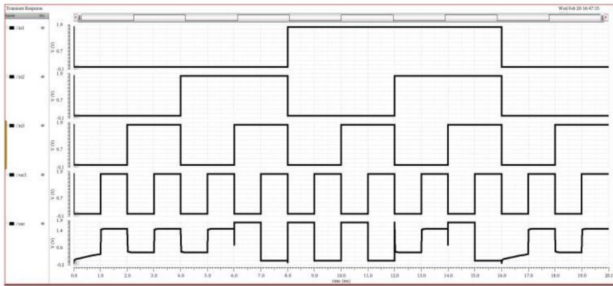


Fig. 6 Transient response of Tester#1

Fig.6 shows the transient response of existing Tester#1simulated in 180nm, 65nm CMOS technology with1.8 V,0.65V power supply and 20 mV input voltage and have100% accuracy in fault detection.

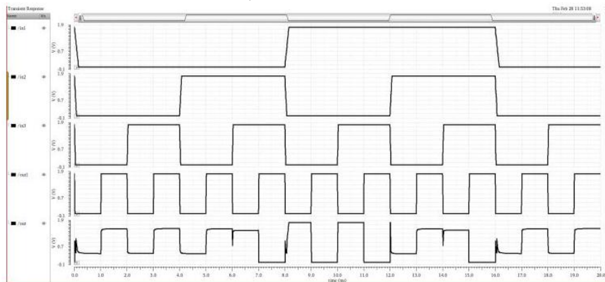


Fig. 7 Transient response of Tester#2

Fig.7 shows the transient response of the existing Tester#2 circuit simulated in 180nm, 65nm CMOS technology by applying 1.8 V,0.65V power supply and 20 mV input voltage and 100%acuracy in fault detection.

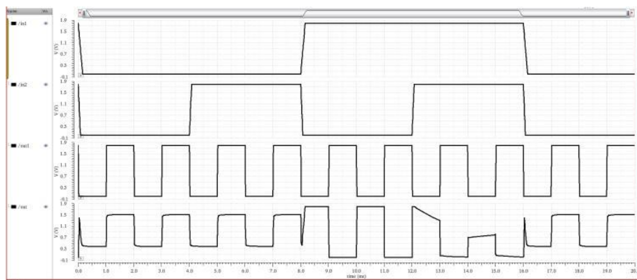


Fig.8 Transient response of Tester#3

Fig.8 shows the transient response of existing Tester#3 circuit simulated in 180nm, 65nm CMOS technology by applying 1.8 V,0.65V power supply and 20 mV input voltage and 75%acuracy in fault detection.

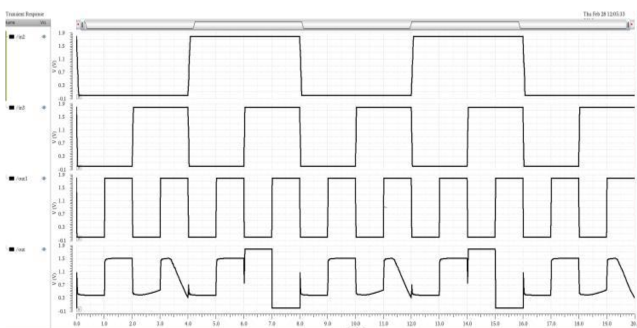


Fig. 9 Transient response of Tester#4

Fig.9 shows the transient response of existing Tester#4 simulated in 180nm, 65nm CMOS technology by applying 1.8 V ,0.65Vpower supply and 20 mV input voltage and 75%acuracy in fault detection.

Fig.10 shows the transient response of modified tester circuit simulated in 180nm, 65nm technology with 1.8 V,0.65V power supply and 20 mV input voltage and 100% accuracy in fault detection.

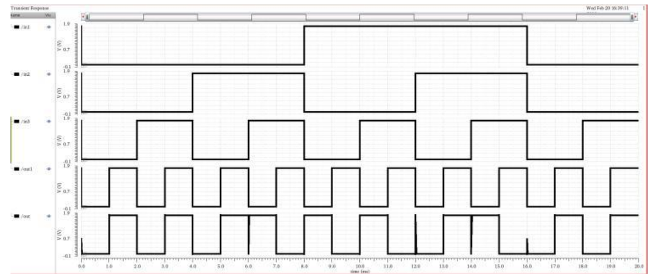


Fig. 10 Transient response of modified tester circuit

TABLE I

TESTERS	1.8V	1.6V	1.4V	1.2V	1V
Tester# 1 [1]	5.29E-04	5.29E-04	5.29E-04	9.17E-06	9.17E-06
Tester# 2 [1]	5.06E-01	5.07E-01	5.16E-01	5.17E-01	5.15E-01
Tester# 3 [1]	9.35E-04	9.45E-04	9.63E-04	9.62E-04	9.65E-04
Tester# 4 [1]	9.95E-04	9.96E-04	9.97E-04	9.98E-04	9.98E-04
Modified Tester	5.30E-04	5.30E-04	4.90E-04	5.30 E-04	5.30E-04

Numerical results of Delay(ms) in 180nm technology

TABLE II

Numerical results of Power in 180nm technology

TESTERS	1.8V	1.6V	1.4V	1.2V	1V
Tester# 1 [1]	418.04 uw	409.35 uw	400.09 uw	406.37 uw	417.30 uw
Tester# 2 [1]	362.61 uw	271.71 uw	214.56 uw	214.67 uw	214.67 uw
Tester# 3 [1]	232.51 uw	406.35 nw	417.32 uw	417.40 uw	417.38 nw
Tester# 4 [1]	315.23 uw	235.11 uw	266.98 uw	312.16 uw	367.28 uw
Modified Tester	364.69 uw	363.82 uw	392.09 uw	364.44 uw	34.464 uw

TABLE III

TESTERS	DELAY (ms)	POWER (W)
Tester#1 [1]	0.01	7.70E-07
Tester#2 [1]	0.01	3.88E-07
Tester#3 [1]	0.05	7.73E-07
Tester#4 [1]	0.07	5.23E-07
Modified tester	0.015	7.69E-07

Numerical results of Delay and Power in 65nm technology

The simulation results of modified tester architecture are 530.0e-6 delay and 364.693uw power shown in Table 1. Fig.12, Fig.13 shown graphical representation of the existing and modified tester circuits.

V. CONCLUSION

In this paper, the design of new tester architecture for fault detection has been proposed. For different tester circuits the output voltage swing is poor so, the modified structure provides full output voltage swing compared to existing circuits. The power and delay values are calculated in 180nm, 65nm technology shown in table I, table II.

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