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DWT Chip Design and FPGA Synthesis for Image Processing

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Abstract: ***The wavelet transforms are used for the detection, extraction, de-noising, compression and analysis of signals and images. A Discrete Wavelet Transform (DWT) is the wavelet transform in which the wavelets are discretely sampled. HAAR DWT is one the popular method of image compression as its coefficients are either 1 or -1. In the DWT, the filters are half band about the quadrature frequency of $\pi/2$radians per sample. The image is decomposed in LL, LH, HL and HH subbands in HAAR DWT method. The research paper focuses on the design and chip implementation of 2D-DWT using VHDL programming in Vivado Design Suite 17.4 and its synthesis on Virtex 5 FPGA. The 2D original image (64 x 64) is processed in (32 x 32) size LL, LH, HL and HH subbands in level 1 decomposing and further 16 x 16 subbands decomposition in level-2 processing. The FPGA hardware utilization and Timing parameters are analyzed for the design.***

Index Terms: VHDL Programming, Discrete Wavelet Transform (DWT), FPGA Synthesis

I. INTRODUCTION

In the real world, data or signals consists of frequent sharp transients. These abrupt transients are important in terms of carrying important information. The Fourier transform is one of the powerful tools for data analysis. Fourier transform does not represent abrupt transients efficiently as it describes data as a sum of sinusoids, which are not localized in space or time. The waveforms have infinite range and oscillate forever. Therefore, it is needed to use the concept of wavelets to analyze signals or images with abrupt transients accurately. Wavelet is simply a short waveform having finite duration with zero average value. It has a time duration from minus infinity to plus infinity in comparison to the sine function. The sinusoidal signals are regular and predictable whereas wavelets are irregular. In the point of view of analysis, the Fourier analysis deals with frequency representation of a sinusoidal signal and wavelet analysis is related to splitting a signal into its scaled and shifted form. The analysis of an irregular wavelet is much easier than a regular sine signal. The ability of frequency and time localization is a very important property of wavelet transform and localization is relating to total time range and frequency.

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The process of compression and expansion of the original or mother wavelet is known as scaling. The wavelet will be more compressed if the value of scaling factor is smaller.

Fig1 and Fig.2 represents the scaling and shifting nature of wavelets respectively.

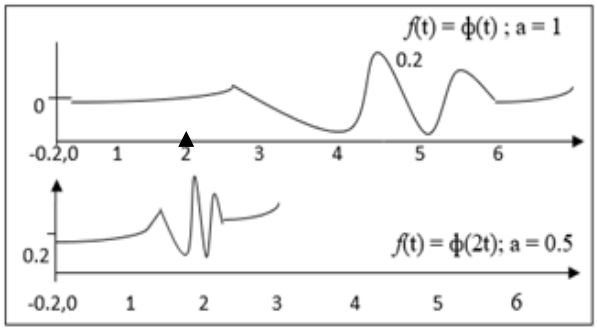

Fig.1 Scaling in wavelets

The shifting in a wavelet is the delay or advancement in the original wavelet.

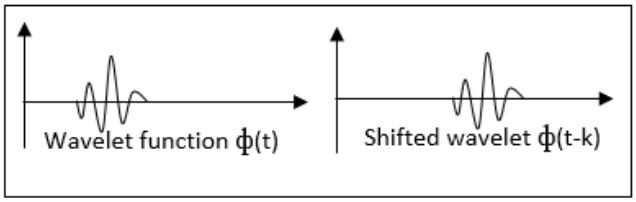

Fig.2 Shifting in wavelets

Discrete Wavelet transform (DWT) is the wavelet transform in which the wavelets arediscretely sampled. In Fourier Transform of a signal, we simply multiply that signal by an analyzing function, which is sum of sinusoidal signal. Similarly, in wavelet transform we multiply the signal by a wavelet analyzing function as shown in the mathematical definition of the two transforms. Both transform the given signal, which is a function of time. However, the difference is that the output coefficients of Fourier transform corresponds to frequency whereas for wavelet transform the output is a two-dimensional matrix of coefficients which are identified by scale and translation.

Fourier Transform: $X(F) = \int x(t)e^{-j2\Pi ft}dt$ from -∞ to +∞

Wavelet Transform: $X(a,b) = \int x(t)\phi^{*}_{a,b}(t)dt$ from -∞ to +∞, a corresponds to scale and b corresponds to translation.

The DWT is used in many applications of image processing such as cryptographic security, watermarking, ultra-wideband (UWB) wireless communications, authentication and biomedical signal processing applications such as design of low-power pacemakers and many more.

DWT is preferred in many applications of image processing because DWT provides multi-resolution and image compression can be carried out for different stages of resolution as per required and high robustness to signal processing. The Wavelet coefficients distribution remains centered around zero, it means that the major part of the image information is concentrated within a small fraction of coefficients as a result it is easy to compress the image efficiently and computations takes less time. The VLSI based architecture and FPGA implementation of DWT algorithm and applying for specific application provides more programmable environment in hardware-based applications. The current research is going on in the field and applying for low power chip design and integration in real time image and signal processing applications.

II. RELATED WORK

watermarking application. The HAAR DWT is followed by four frequency subbands (LL, LH, HL and HH) working independently. The functionaliy of the design is simulated with the help of hardware cosimulation approach followed by MATLAB-Xilinx system generator (XSG), on Virtex 5 FPGA. Halder, A et al (2019) suggested the large level memory block reduction methods by the incorporation of DWT and byte compression method. The DWT has been proved the fast technique for image compression in comparison to other existing method such as JPEG and JPEG 2000 in terms and provides good compression ratio. Hussain, M. S et al (2018) suggested 2D DWT for non-causal Deslauriers-Dubuc applied for real-time video processing is proposed. The method was decomposed based on horizontal and vertical details with approximation and Simulink HDL coder platform is used to analyze the system performance on Intel/Altera DE2i-150 board. The technique with FIFO logic and counter provides serial data processing based on wavelet transform that decreases the overall delay and system becomes faster. Arrabal-campos et al (2018) presented a new application, which has been developed power quality disturbances, white noise. The MATLAB system integration provides the monitoring of Fourier transform (FT), short time FT, DWT and de-noised signals constantly. Lopez-Ramirez, M **et al (2018) Suggested the method of** Power quality disturbances (PQD) for the classification and recognition with the integration of FPGA, mathematical morphology and DWT for different real time current and voltage signals. The system provides the online PQD detection and classification, which are generated by nonlinear loads and environmental conditions.Nazir Atif et al (2018) worked on Content Based Image Retrieval System (CBIR) used for the retrieval of the images from the original database with the help of DWT. They used DWT for the extraction of texture features. The system was evaluated on Corel 1-k dataset followed by precision and recall approaches to provide efficient and competitive results. Choi, M. R (2018) presented a new technique of interpolation, which is based on the combination of adaptive DWT and DCT. The ADWT is used to decompose the low-resolution image in four sub bands and DCT is used to decompose high frequency bands simultaneously. The same image is reconstructed by the interpolation of subband image using inverse DWT and combining the actual low-resolution images. The proposed work results in much improved visual quality of high-resolution display system. Witwit, W et al (2017) make use of DWT and new edge directed interpolation to make enhancement in resolution of satellite of image. They applied a threshold to preserve the edges and avoid noise. They used DWT to decompose the low input signal in four sub bands and interpolation technique for interpolating high frequency. The system performance is analyzed for the reconstruction of three videos.Lama R. K et al (2016) suggested the new hybrid technique by combining DWT and DCT methods. The DCT is used for interpolating high frequency components on zero padding technique. The upscaled image is obtained using inverse DWT on original image and of interpolated coefficients. Deepa M. et al (2016) proposed automatic image registration based on DWT. The input image is subdivided in four subbands as Less-Less (LL), Less-High (LH), High-Less(HL)and High-High (HH). They used the DWT to extract the LL bands components on reference and sensed images to extract the features using MATLAB image processing tool. Kumar, A. et al (2015) proposed the hardware chip implementation of HAAR DWT applicable for colour image processing, detects three types of edges, and eliminates non-texted portions. The design was based on VHDL code and verified on Virtex -5 FPGA with image decomposition in LL, LH, HL and HH bands. Agoyi, M. et al (2015) introduced an innovative watermarking technique based on DWT combining with chirp z-transform that supports singular level decomposition. The experiments were performed on two 128 × 128 watermark images that support symmetric and non-symmetric image. The performance of the images is verified under different attacks such as histogram equalization, blurring, scaling, and contrast enhancement, AWGN and gamma correction.Shahadi, H. I. et al (2014) proposed proficient and high-performance architecture for HAAR DWT working in forward and inverse mode. They implemented the chip for the algorithm using HDL and synthesized on Xilinx Spartan6-SP601 FPGA Evaluation Board. It is the integer HAAR DWT core and optimized as multipliers free design. Nagabushanam, M wt al (2013) implemented the DWT on Virtex-5 FPGA that operated on 180 MHz and uses less than 1W of power. The chip design occupied less than 1% of the LUT as hardware resources on FPGA applicable for real-time image processing on FPGA hardware.Ja'afar, N. H. prosed the design and hardware chip implantation of 3D DWT architecture on Spartan-3 (XC3S2000) FPGA used for image compression. The design was based on cascaded design of 1-D HAAR DWT following N×N×N configuration. The FPGA synthesis and experimental results analyzed the chip performance in terms of power consumption, area, latency, maximum frequency, and throughput. Bahoura, M et al (2012) presented the FPGA implementation of DWT and Inverse DWT for signal denoising application with the help of Xilinx System Generator for DSP. The algorithm was verified on Virtex-II Pro development board. The architecture evaluation is done with respect to hardware resource utilization, reconstruction error and denoising performance. Huang, Q et al (2011) implemented the DWT and IDWT in Altera Cyclone II platform - DE II FPGA development board. The design was supported the 100 MHz frequency.

The optimization was carried based on look-up table, distributed arithmetic, and pipeline architecture. Çavuşlu, M. A et al (2010) proposed the DWT and IDWT implementation using Altera Cyclone-II FPGA. The Filtering [process is done row wise and column wise.

The design has proved good results in terms of cost and device hardware utilization as 2% approximation of available resources for same FPGA. Jayaraman, S (2009) presented the DWT in detail for image compression, segmentation and watermarking applications. They have tested on 'cameraman image in MATLAb tool for watermarking and cryptographic applications Chilo, J. (2008) et al purposed the FPGA implementation of DWT consisting of two FIR filters, a high-pass and a low-pass filter, applied for real-time infrasound data processing. The chip design was done in QUARTUS II platform using FPGA implementation using VHDL programming.

DWT has been proved the best method for image processing. The ASIC and FPGA realization will solve the different problems in real time processing of images in hardware-based system in comparison of traditional Fourier Transform based system analysis in terms of higher processing speed, optimized hardware utilization and throughput.

III. HAAR DWT

As far as the application of DWT on images is concerned we apply one-dimensional filters first along the rows of image and the along the column vice versa, because images are two-dimensional. In the figure below j refers to scale, r refers to row and c refers to column.

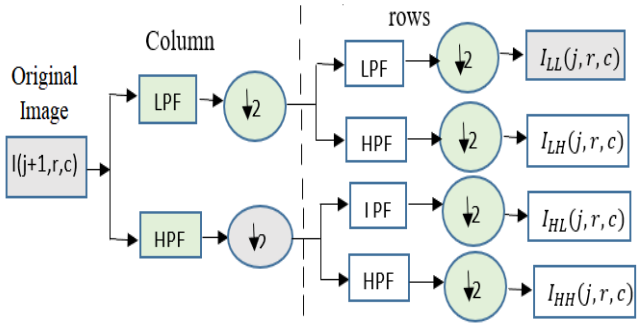

Fig.3 DWT Filtering

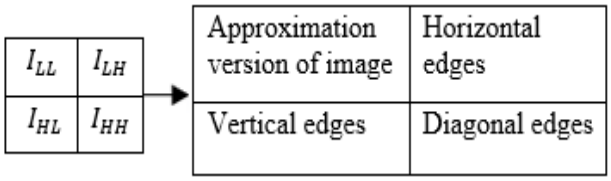

Fig.4 Image decomposition bands

As we know that a low pass filter does the approximation and a high pass filter extract the features of the original image. So, if we examine the output side, the approximation of the input image is given by the output I_{LL}. The output I_{LH} has passed through a high pass filter which has operated on the rows of the image, so it will give the horizontal properties or features of input image. Similarily vertical features of the input image is given by the output I_{HL} and the output I_{HH} gives the diagonal edges. This was first level decomposition of the input image. If we make the approximation output of the image as input and do the same operation to this input image, then we will get the second level decomposition of the original image. The fig. 3 shows the DWT filtering with low and high pass filtering. The fig. 4 presents the image ecomposition bands. The fig.5 and fig.6 presents the HAAR DWT processing and HAAR DWT decomposition of an image respectively. The image of size (64 x 64) is processed as the original image. In level -1 decomposition, the image is divided into 4 subbands LL(32 x 32), LH(32 x 32), HL(32 x 32) and HH(32 x 32) and further processed in LLLL(16 x 16), LLLH(16 x 16), LLHL(16 x 16) and LLHH(16 x 16) subband in level-2 processing.

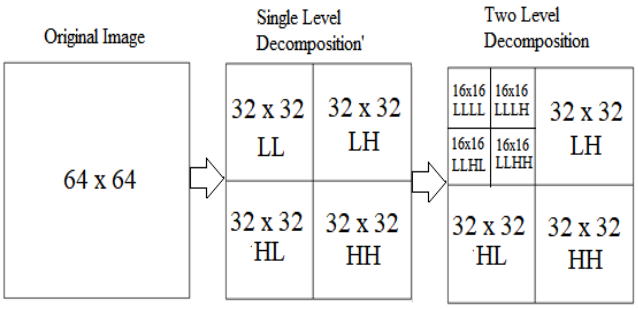

Fig. 5 HAAR DWT Processing

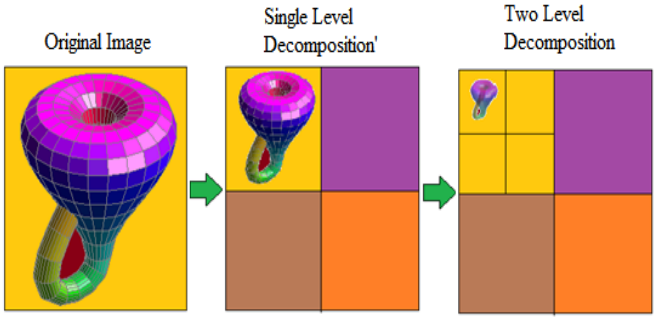

Fig. 6 HAAR DWT decomposition of an image

IV. RESULTS & DISCUSSIONS

The results of DWT chip design are carried out in Xilinx Vivado Design Suite 17.4. The RTL chip view is shown in fig.7 and the detail of pins functionality is listed in table 1. The internal schematic of the chip is shown in fig.8 (a) and (b).

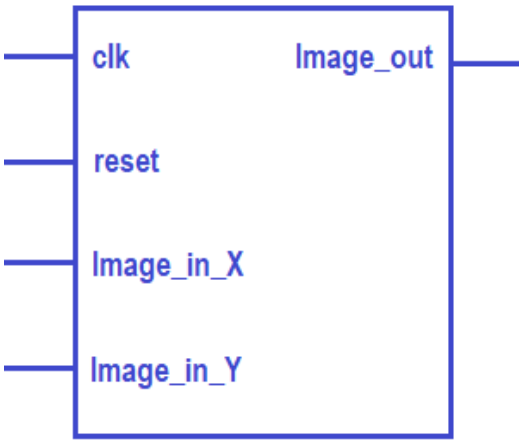

Fig. 7 RTL view of chip

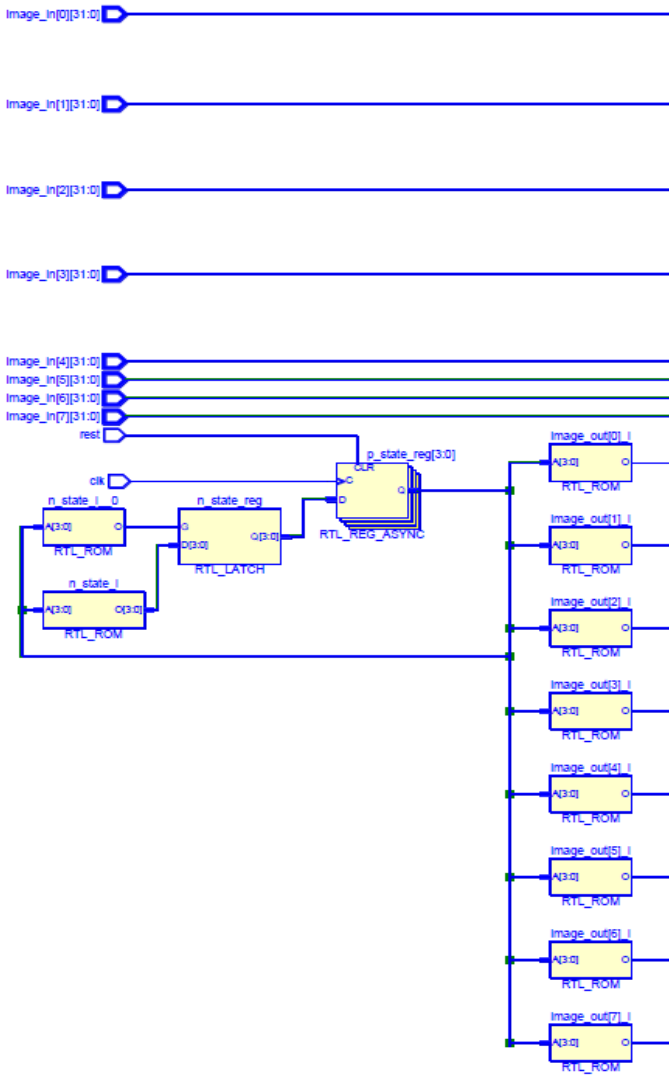

Fig. 8 (a) Internal schematic view-1

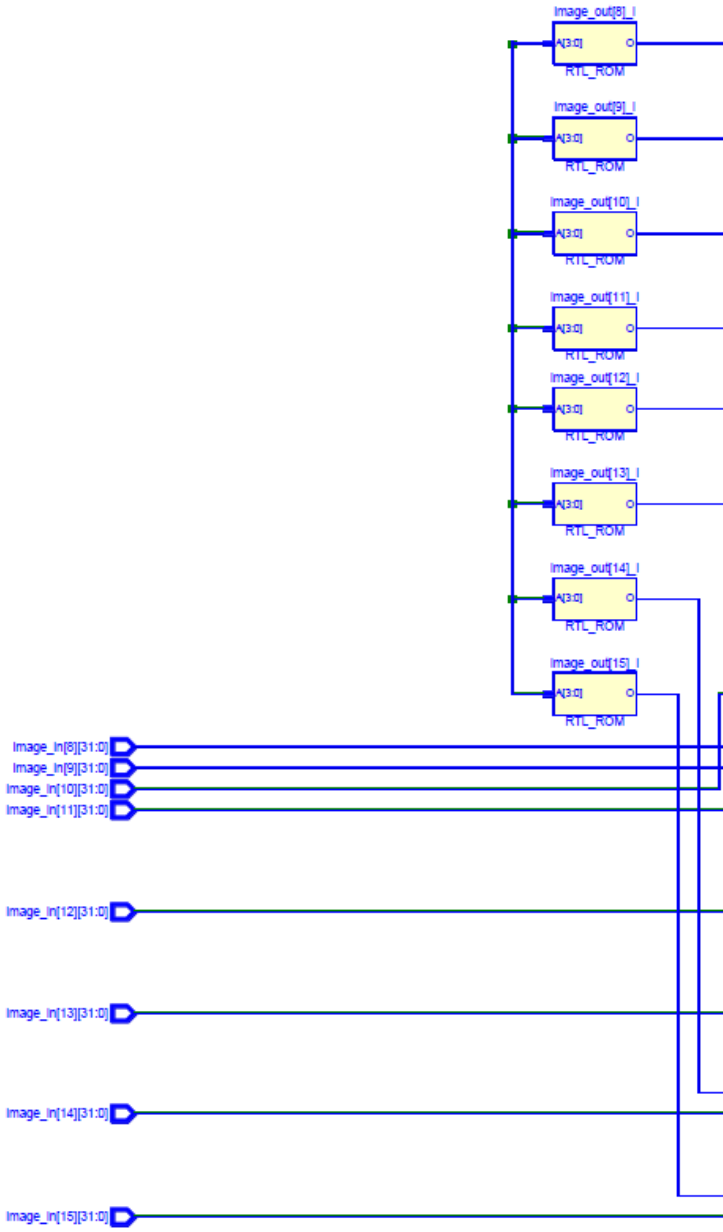

Fig. 8 (b) Internal schematic view-2

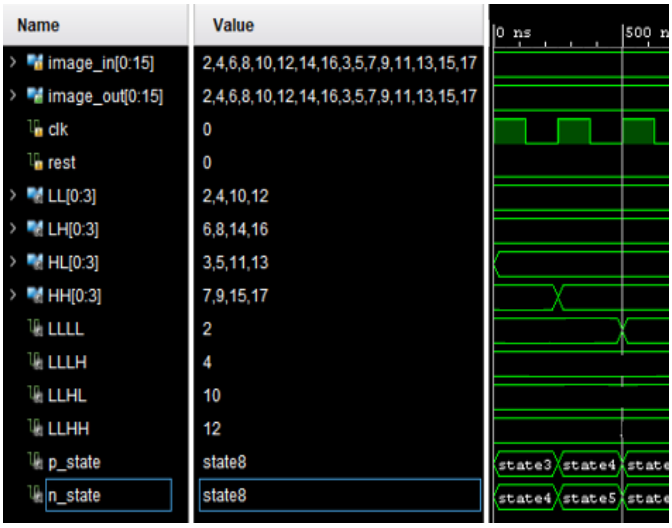

Fig. 9(a) Xilinx Simulation for 2D DWT- Test1

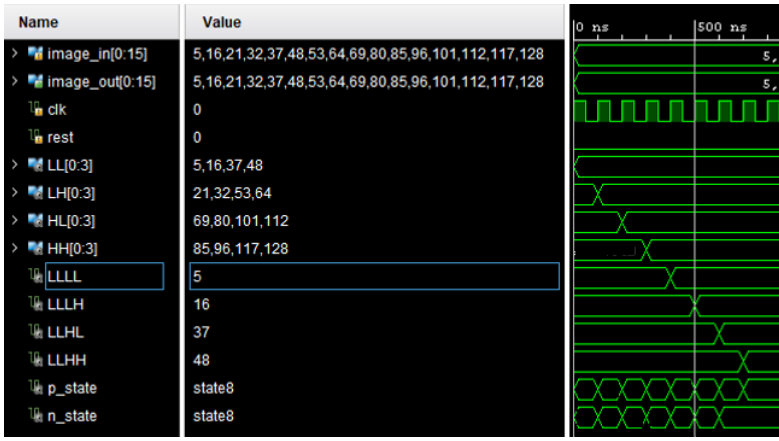

Fig. 9(b) Xilinx Simulation for 2D DWT- Test2

Table 1 Pin Functions

Pins	Functional Description
reset	It is input logic, used to reset the hardware chip with zero contents in memory
clk	It is input to provide the default clock signal input with rising edge pulse
Image_in_x	Array input of the image pixels intensity matric in X directions
Image_in_y	Array input of the image pixels intensity matric in Y directions
Image_out	Output array to the image pixels after DWT decomposition in LL, LH, HH and HL subbands

The Xilinx ISIM simulation for test case 1 and test case 2 is shown in Fig 9(a) and (b). The inputs for test -1 and test -2 for image (16 x 16) is {2, 4, 6, 8, 10, 12, 14, 16, 3, 5, 7, 9, 11, 13, 15} and {5, 16, 21, 32, 37, 48, 53, 64, 69, 80, 85, 96, 101, 112, 117, 128).

Table 2 Device utilization for 2D DWT (64 x 64)

Device Part	Utilization	
Number of Slices	242 out of 12480,	2%
Number of Slice Flip Flops	560 out of 12480,	5%
Number of 4 input LUTs	180 out of 493,	37%
Number of bonded IOBs	130 out of 172,	76%
Number of GCLKs	1 out of 32,	3%

Table 3 Timing parameters for 2D-DWT

Timing Parameter	Utilization
Minimum Period	1.1017 ns
Maximum Frequency	345.00 MHz
Minimum input arrival time before clock	2.216 ns
Maximum output required time after clock	4.230ns
Total Memory usage	1254839 kB

The chip synthesis is carried on Virtex -5 FPGA on xc5vlx20t-2-ff323 target device. The hardware parameters are shown in table 2 with the information of no. of slices, flip-flops, IOBs, LUTs and GCLKs utilization. In the same way, the timing parameters with minimum maximum period is listed in table 3 that provides the information of chip timing such as minimum **p**eriod (ns), minimum time before clk (ns), maximum time after clk (ns), and combinational path delay. The frequency of the design is 435.00 MHz and CPU memory usage is 1254839 kB.

V.CONCLUSIONS

The 2D -DWT is a significant wavelet function in numerous multimedia applications, such as JPEG2000 and MPEG-4 standards, filtering, digital watermarking, and several related operations of image compression and segmentation. The 2D image (64 x 64) decomposed in (32 x 32) first level and further (16 x 16) in second level. The VHDL code support the designed chip on FPGA hardware. The simulation results show the successful decomposition of the 2D image. The chip is tested on Virtex -5 FPGA on xc5vlx20t-2-ff323 against the sampled values of (64 x 64) and (16 x 16) image. The hardware and timing results are optimal, and design supports 345.00 MHz frequency. In future, we are planning to integrate the higher end FPGA hardware with watermarking and cryptographic applications with more compression ratio.

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