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SEPIC Topology Based High Voltage gain DC-DC Converter

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Abstract: ***DC Voltage boosting is essential for many applications. Several techniques and topologies have been developed to produce high DC voltages. The Transformerless technique of producing high voltage DC is also been developed however there are certain inherent drawbacks in the developed techniques .This paper introduces the analysis and design of SEPIC (Single Ended Primary Inductance converter) topology based high voltage DC-DC Boost converter with single and two stage added boost converter, to achieve high boost ratio in the range 10 to 50 with low input voltage ranging from 12V-15V. The paper describes the operation of SEPIC topology converter and compares with other boost topologies .The converter is operated in open loop for high step up without the use of transformer thus reducing the magnetic leakage and associated losses. The designed SEPIC converter is simulated in PLEC's software with ideal operating conditions and desired output of 200V with low inductor current ripple is obtained.***

Keywords: Current Ripple, SEPIC-Single-ended-primary-Inductance converter, Transformerless.

I. INTRODUCTION

In today's scenario the trend is to optimize the components and cost with improved efficiency and one such development in power electronics is to produce high voltage from low voltage source with optimal components by choosing or designing the suitable converter topology. There are vast applications of high voltage DC-DC boost converter in medical equipment, Aviations, industrial drives, LED drivers, renewable energy system, wireless charging system and in experimental physics (HV pulse power, plasma science and scanning microscope).Based on the application where high input to output boost ratio with better dynamics, stability ,high power density and high efficiency is required there are different voltage boost topology like SC-switched capacitor (charge pump),VM-Voltage Multipliers-Switched Inductor, Luo converters, Magnetic Coupling and Multistage/level topologies. Further conventional method to achieve high voltage gain is by means of step up transformer but the use of transformer is limited while using in circuit with high switching frequency device due to leakage reactance and losses, this has resulted in transformer less[1] converter topologies for high voltage gain.

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There are many options to derive high voltage boost circuit from basic single-stage boost converter. A typical conservative recommendation for boost converter is not to boost by more than factor of six in single stage, this is because to achieve voltage gain exceeding 6, the converter has to operate at higher duty ratio which can saturate the PWM and hence degrade the efficiency of converter [2].
Over past decades many topologies have been discussed to achieve transformer less high voltage gain in the ratio 1:100 [3],[4] with improvement in PWM techniques for high duty ratios, reduced component stress and increase in Efficiency [5].Many topology has been discussed and compared by the author cited in [6].

In this paper the attempt is made to design and simulate SEPIC topology based high voltage gain DC-DC Boost converter as SEPIC based topology has inherent Merits compared to basic boost converter and charge pump converter for same output boost voltage and power level.

The Basic boost converter [7] though is simple with lesser number of components but suitable for low boost ratios, for high voltage boosting they have to be operated in high duty cycle close to unity which leads to high voltage and current stress and increase in conduction loss. Whereas the Charge pump circuit /Voltage multiplier [8],[9] though a choice for high voltage low current applications has its own limitation, each voltage multiplier stage need two series diode leads to forward conduction losses and large value of capacitor in VM stage increases RMS switch current. These drawbacks are overcome in the SEPIC based topology. In this paper the design and analyses of single stage SEPIC is carried out further extending design for SEPIC with added boosts stage [10], [11] for high voltage gain applications.

II. METHODOLOGY

The SEPIC produces an output voltage that is either greater or less than the input but with no polarity reversal. It uses two inductor either coupled or discrete, equal voltages are applied across the inductor through switching cycle. Fig 1(a) shows the basic SEPIC circuit. Fig 1 (b) shows SEPIC in switch closed condition, here the diode is blocked and voltage across L1 for interval DT (duty ratio and total time of switch on and off) is equal to the source voltage V_{in} while in open condition as shown in Fig 1(c) the diode is in conduction state for interval of 1-DT output voltage given as Vo=Vs (D/1-D).

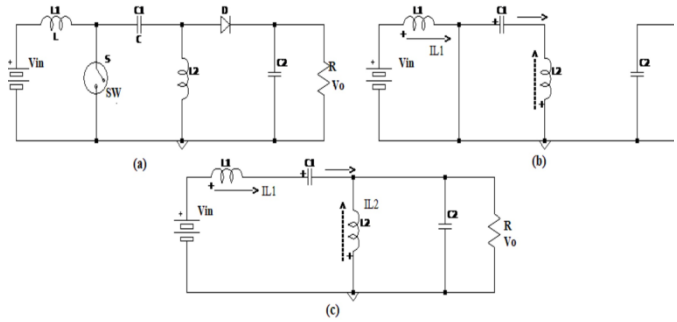


Fig.1. (a) SEPIC Circuit (b) SEPIC with Switch closed (c) SEPIC with Switch open

Circuit Parameters for Sepic Single stage

Input output voltage relation for SEPIC single stage is given by (1) from Kirchhoff's voltage law.

$$G = \frac{Vo}{Vin} = \left(\frac{D}{1-D}\right) \quad (1)$$

Where,

G = Gain

Vo = output Voltage

Vin = input voltage

D = duty ratio

(A) Inductance calculation

Power supplied from DC source is equal to the average inductor current and source voltage, average inductor current is same as the source current.

The minimum inductance L1 value is determined by

$$L1 = \left(\frac{Vs\ DT}{\Delta Il1}\right) \quad (2)$$

Inductor average Current

$$IL1 = \left(\frac{Vo^2}{Vin\ R}\right) \quad (3)$$

R = Load resistance

Is = Source current

Is = IL1

ΔIl1 = Inductor ripple current

Ripple current=40% of Inductor average current

The minimum inductance L2 value is determined by

$$L2 = \left(\frac{Vs\ DT}{\Delta Il2}\right) \quad (4)$$

The output current is same as average inductor current at L2, hence I_0 = IL2

(B) Capacitance calculation

Capacitance C_1 is calculated at switched closed and magnitude of charge stored in capacitor current IC_1 is same as IL_2 where IL_2 is equal to the output current.

$$\Delta Vo = Vc_1 = \frac{VoD}{RC_1 f} \quad (5)$$

ΔVo = output ripple voltage

Capacitor C2 is determined considering output ripple voltage

$$\Delta Vo = Vc_2 = \frac{VoD}{RC_2 f} \quad (6)$$

III. SEPIC CONVERTER WITH 2 STAGE ADDITIONAL BOOST

To increase the output boost voltage the diode is added at the first stage and filter capacitor at the output, Fig 2 shows the modified sepic converter. To design the sepic boost converter the below mentioned operating conditions are followed.

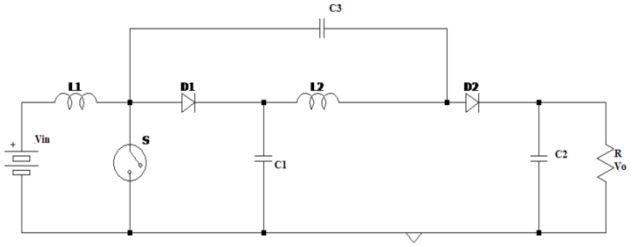


Fig. 2. SEPIC With added boost

All components are ideal .The MOSFET and diodes have low forward voltage drop and less off state leakage current.

The inductor ripple current is negligible. The circuit operates in CCM-Continuous current mode operation. There are no losses.

Parameter derivation for 2 stage SEPIC added Boost

By adding diode and capacitor C_3 to the sepic, the 2 stage boost output can be obtained, inductor L_2 is now connected to diode D1 and capacitor C1, the sepic stages are connected in DC series with boost output at C2[12],[13]. Both the ends of L_2 have an average DC voltage equal to single stage boost voltage on C1 and 2nd stage Boost output at C3 from 1 the two stages SEPIC duty ratio is derived as

$$D = \frac{VC_1 Vin}{VC_1} = \left(\frac{D}{1-D}\right) \quad (7)$$

$$VC_1 = Vin + \left(\frac{Vo-Vin}{N}\right) \quad (8)$$

N=2, 3... For Number of boost stage

IV. SIMULATION RESULTS

This section discusses the simulation results of topology mentioned in Fig 1 and 2. A simulation model of the proposed converter has been built in PLECS sim software.

A. Simulation of Single stage SEPIC

Single Stage SEPIC is designed and analyzed, the designed parameter is listed in Table 1 the calculation is made considering ideal operating condition and converter operates in CCM-continuous conduction mode.

TABLE I
SIMULATION PARAMETERS

SL No.	*Parameter*	*Value*
1	Input voltage *Vin*	12V
2	Output voltage *Vo*	100V
3	Power rating	30W
4	Duty Ratio	0.88
5	Switching Frequency *fsw*	500kHz
6	Inductor L_1 and L_2	39µH
7	Capacitor C_1 & C_2	32nF,80µF

a. Inductance design

The inductor current in both phase during switch ON and OFF is taken as average inductor current, the average inductor current is also equal to the average source current $Is = IL_1$,the minimum inductor size is obtain from (4) and next higher value of inductor is selected for simulation .

The duty ratio is calculated using (1).

$$\frac{100}{12} = \left(\frac{D}{1-D}\right)$$

$$D = 0.88$$

The inductance value is calculated using equation 4 considering peak to peak ripple current occurs at 40% of duty cycle with input voltage of 12V the inductor value obtained is $L_1 = 39\mu H$..

b. Capacitance design

The voltage variation in C_1 is determined in switch closed condition capacitor current I_{C1} is opposite to inductor current, the capacitance value is calculated using(5) considering 10% of average ripple voltage across capacitor. The output stage consist of the diode D_2, C_2 and the load resistor is same as in the SEPIC boost converter so output voltage ripple is taken as 10% of ripple voltage and capacitor C_3 is calculated. Fig 3 shows the simulation model of SEPIC single stage converter using MOSFET switch, operated at 500 kHz at 88% duty ratio. The fig 4(a) represents output current waveform. The desired output of 100V is obtained from low input voltage of 12V as shown in fig 4(b).The simulated wave form of output current and voltage is represented along Y-axis and time 0.2/div X-axis respectively.

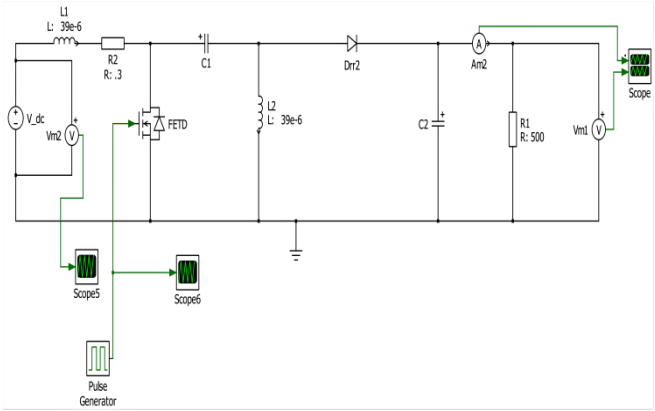
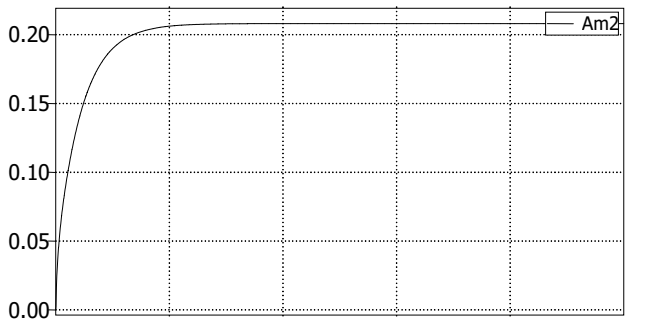
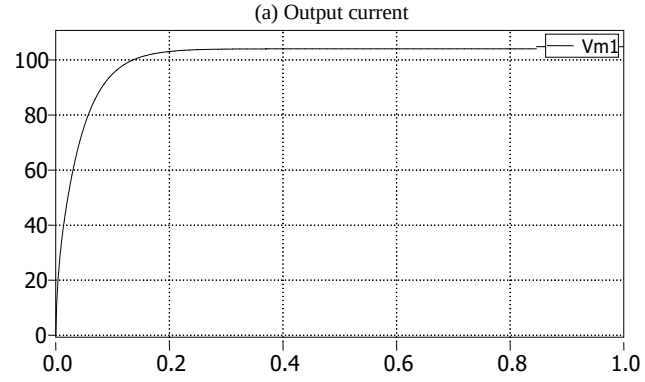


Fig.3. Simulation model of single stage SEPIC



(a) Output current



(b)Output voltage

Fig.4. Simulation waveforms with simulation time 1.0s
(a) output Current (b) output Voltage

B. Simulation of 2 stage SEPIC

The simulation parameter of 2 stage SEPIC is as shown in table II and is designed with slight modification in SEPIC circuit such that the voltage level is twice as SEPIC converter. Adding additional series diode at end of first output stage and filter capacitor at output without change in operating duty cycle.fig 5 shows the Simulation model of 2 stage SEPIC.

The duty ratio is calculated using (7) and is same as single stage converter.

$$VC_1 = 12 + \left(\frac{200 - 12}{2}\right)$$

$$VC_1 = 106V$$

$$D = 0.88$$

TABLE II
SIMULATION PARAMETERS

SL No.	*Parameter*	*Value*
1	Input voltage *Vin*	12V
2	Output voltage *Vo*	200V
3	Power rating	30W
4	Duty Ratio	0.88
5	Switching Frequency *fsw*	500kHz
6	Inductor L_1 and L_2	39µH
7	Capacitor C_1 ,C_2 &C_3	32nF,80µF 35 µF

a. Inductance design

The inductance value L_1 and L_2 remains same with slight change in Peak to peak handling capability. The inductance value is calculated using 4 considering peak to peak ripple current occurs 40% of duty cycle with input voltage of 12V.

b. Capacitance design

The voltage variation in C_2 is determined in switch closed condition capacitor current I_{C1} is opposite to inductor current, the capacitance value is calculated using 5 considering 10% average ripple voltage across capacitor.

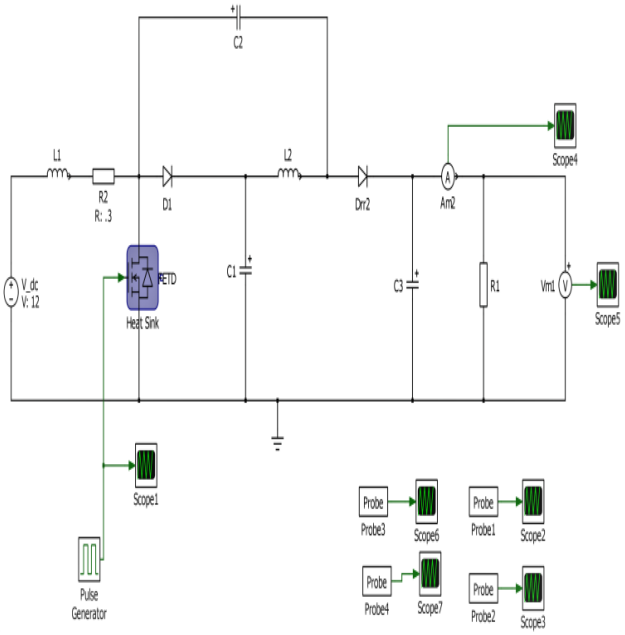


Fig. 5. Simulation model of 2 stage SEPIC

The voltage and current waveforms are shown in Figure 6 for 2 stage SEPIC based boost converter, it can be seen that for an input voltage at 12V output voltage accomplished is around 190V when compare to theoretical calculation of 200V.

This verifies operation analyses of the converter where output voltage is around V_o=200V under open loop condition with very small switching loss and voltage stress across the switch. Fig 6(a) and 6(b) shows the load current and voltage waveform respectively. Simulated wave form of output current and voltage is represented along Y-axis and time 0.02/div along x-axis respectively.

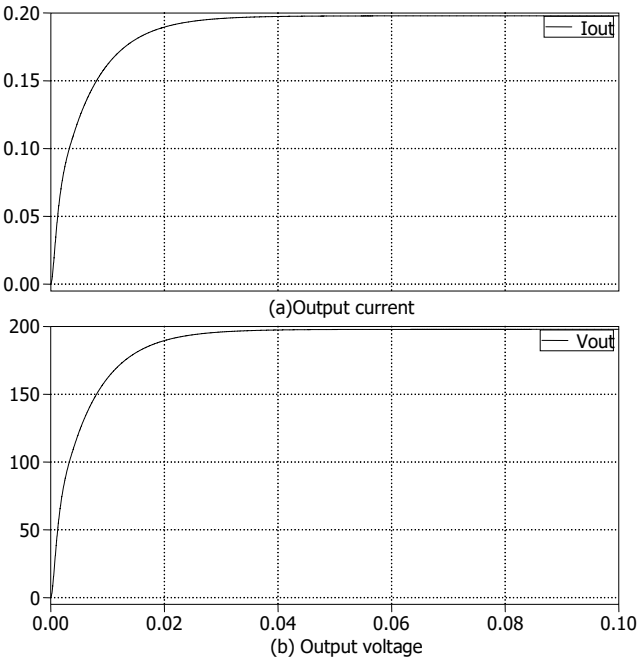


Fig.6. Simulation waveforms with simulation time 0.1s
(a) output current (b) output voltage

Fig 7(a) and 7(b) corresponds to inductor voltage and current across inductor L1 respectively. The inductor current ripple $\Delta Il1$ is 0.14 which quiet less for SEPIC two stage converter.

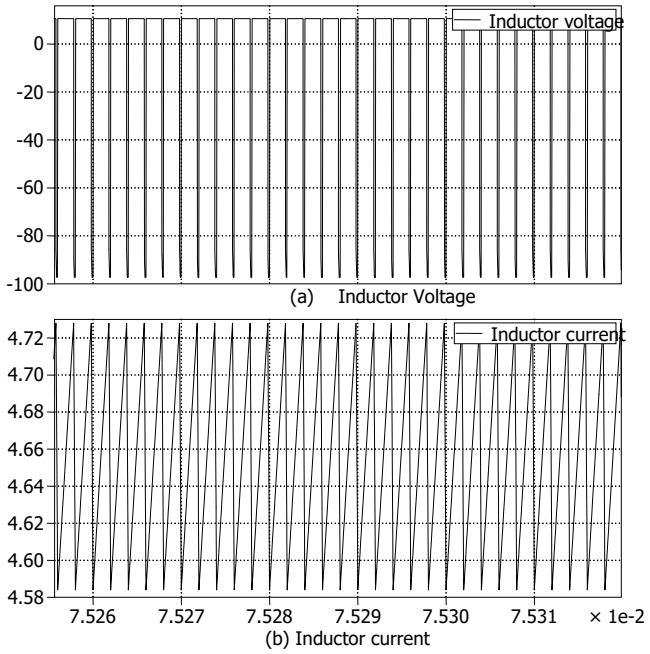


Fig.7. Simulation waveforms with simulation time 0.1s
(a) Inductor voltage (b) Inductor Current

V. CONCLUSION

The SEPIC converter with added boost stage is designed, simulated and analyzed, the following conclusion are drawn from present simulation work.

- Proposed converter supports the high step up voltage gain operating under open loop condition with duty cycle up to 88%.
- The Duty cycle is quiet less compared to simple boost circuit to achieve the same voltage level and hence losses are reduced.
- Converter has lower inductor current ripple which is of practical importance in certain applications.
- The voltage can be boosted further to higher values without change in voltage stress across semiconductor switches with increased number of stages.

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