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Verification of Accessibility and Connectivity of Multi-Die Module Through TAP Interface

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Abstract: ***In the recent years, there is advancement in the SoC (System on Chip) designs along with the rapid evolution in the technology scaling. SoC Package may include multiple chips, semiconductor dies, core components with many system management blocks and multiple IP (Intellectual Property) cores with identical or different functionality integrated onto the single integrated chip (IC). In present days, when compared to the MCM (Multi-chip Module) multiple dies are fabricated onto the single package which collectively account for achieving several goals accounting for less manufacturing cost. The complex design requires structured and novel way of testing the structural interconnects. Therefore, TAP (Test Access Port) interface proves to be simpler and efficient. This is carried out by employing the three standards, IEEE 1149.1, IEEE 1687, IEEE 1500 at different levels of SoC which modularize the testing mechanism in an efficient way. Thus, the structural testing must be performed at chip level as well as SoC level to ensure proper interconnection between the IPs and the multiple dies respectively. This paper presents the test access configuration for accessibility verification from Package level to down the hierarchy to IP cores through MTAP (Master-TAP) controller and structural interconnects among dies. The intention is to ensure internal registers through several modes of connections. Among the modes discussed, we can observe that the number of clock cycles required for bypass mode and broadcast mode is 24% and 26% reduced respectively. Also, prior detection of number of dies present in the SoC adds the advantage at platform-based testing reducing the testing time to the greater extent.***

Index Terms: ***Design for Testability, IEEE 1149.1, IEEE 1500, IEEE P1687, Multi-Die Module***

I. INTRODUCTION

In modern VLSI, the SoC (system-on-chip) design proves to be complex and area efficient where SoC package contains several cores inside, along with multiple IPs, blocks/modules where each of them contains individual design components. Area, speed and the power are of major concern in the current VLSI design. [5] discuses about the challenges and trends in the modern SoC design verification. With the trend of SoC technology, high density and high capacity embedded memories are required for successful implementation of the system. Instead of integrating all or most of the system needs on large and complex single chips, smaller and high yielding chips were fabricated and reconstituted them to behave like large chips as multi-chip modules (MCMs) [7]. To make the design as cost effective and to obtain the good yield, instead of multiple chips on a single substrate, multiple dies are being fabricated onto the single package along with the multiple IP cores and other design blocks which employ lot of functionalities and together add up to achieve many system goals. This SoC package refers to the Multi-Die Module.

The high density SoC package must consume low power with minimum delay. To meet these requirements, a design must operate typically in different clock frequencies and use a set of sophisticated power management and clock distribution strategies. Therefore, testing of such complex SoCs becomes crucial and requires an adequate testing approach. Structured and area efficient DFT (Design for Testability) [8] methodology in the SoC verification helps to achieve more yield and meet the product requirements. DFT provides the increased testability (controllability and observability) features which makes the testing of complex microprocessor based SoC and other multi-die modules of the modern VLSI circuits easier regarding access time. As the number of cores increases the testing methodology should be improved which provides cost benefits over the debugging. Hence, we use TAP interface for the verification of accessibility and connectivity of the cores. DFT includes many methods [10] such as Boundary scan standard technique for testing the interconnections among the ICs and internal logic of the IP cores sometimes, MBIST (Memory Built in Self-Test) for testing the memories etc. The structural testing is also as important as functional testing. The one way of structured methodology for testing the SoC is the modular testing of the embedded cores by isolating the groups of core blocks in order to gain test access to each of the partitions in the SoC for the delivery of test data. This paper [6] presents the novel method which helps in reducing the test data cost and increase the production capacities. This method can be used for embedded chips containing multiple cores that are identical and isolated. All the core blocks can be tested at the same time in parallel along with the achievement of accurate diagnosis of failure with limited test resources. The structural testing can be carried out by employing the well-defined test access mechanism (TAM), through which one should reach out to the test data registers (TDRs) in the RTL to give the test data as an input and to check the response of the RTL or design under test (DUT) for the given test data input. Test data registers should be reached out at each level of the design hierarchy from IP or complex level down to the leaf level module.

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IEEE 1149.1 [1] can be used at the board level as well as chip level, IEEE 1687 [2] gives the test access standards at the chip level and IEEE 1500 [3] gives the structural testing standard at the chip/core level. The IEEE 1500 standard gives the controllable test architecture for IP cores using the configured wrapper of IP cores referred to as test control switch [4]. The TAP interface helps to access the test data registers through the IEEE 1687 protocol employing test access mechanism at different levels for the actual RTL which helps to increase the core accessibility and testability of the design after manufacturing of the chip. The connectivity verification can be done through various modes of operation performed to ensure the proper connection among the multiple dies in the chip.

This chapter included an introduction to the Multi-Die Module package, DFT and the test access mechanism. The section II briefs about the TAM in the SoC, section III about the Multi-Die Module and its various modes of operations. Results are discussed in section IV.

II. TEST ACCESS MECHANISM-SoC NETWORK HIERARCHY

The first challenge that the DFT engineers would face is the way of exercising all internal stages of design and reaching the full coverage goal. One should employ simpler and efficient method to access all the internal stages. The SoC network contains various blocks of different functionalities. Some of these blocks include the cores, power management block, system management block, clock controllers, BIST circuitry etc. These blocks are designed in a hierarchical manner so the functionality verification and interconnect testing can be done in a systematic manner.

The SoC test access mechanism is shown in the block diagram of Fig.1. The SoC test network hierarchy is divided in conjunction with the three IEEE protocols which are defined with the standards IEEE 1149.1, IEEE 1687and IEEE 1500. Every block or core logic in the SoC is controlled and accessed by the Master-TAP controller which works based on the 1149.1 protocol. The specific operation is performed based on the instruction provided at the instruction register through test data input pin.

At higher level of the design to the core/leaf level module of the design the interface happens through the wrapper logic. The Master-TAP allows the core level access through P1687 interface which employs the test wrappers at IP controller level and the 1500 logic level. The test wrappers include the instruments or the IP blocks and ease for establishing the link between various controllers, child controllers and many core logic blocks controlled by them. The block diagram shows mainly the three levels of hierarchy in the design.

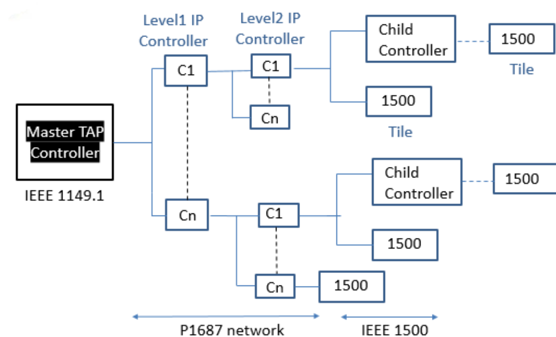

Fig.1 Test access mechanism of the SoC Network

The first level is the Master Test Access Port (MTAP) level which allows us to give test data input from external sources through test data input pin and get the responses from test data output pin. It comprises of the IEEE 1149.1 standard along with the boundary scan architecture which facilitates interconnect testing and internal logic verification through assembled PCBs (printed circuit boards) and several other products which contain complex integrated circuitry and high-density surface mounted techniques of assembly. The standard also provides ways to access and control the DFT features which are built into the digital ICs itself.

For the next level of hierarchy, it begins with IEEE 1687 [2] controllers of many embedded cores or logic design blocks. These target for the embedded instrument access through on-chip network configuration from the device interface. The test access network configuration is used as transport method of test data input and get the test responses and the patterns between the Inputs/Outputs and the SoC.

The leaf level of SoC network hierarchy contains IEEE Std 1500 embedded core blocks and the system management blocks. It defines a scalable standard architecture in order to enable test reuse as well as embedded cores integration and its associated circuitry [3]. This standard includes parallel and serial test access mechanisms with several instructions suitable for testing cores, SoC interconnects, and circuitry. It also promotes good techniques of DFT (design-for-test) and will enhance the quality of test through improved access.

III. MULTI-DIE MODULE

The complex multi-die package with high performance designs involve expensive technology, hence it certainly requires efficient DFT methodology for verification and fault diagnosis of structural interconnects between the multiple chips in MCM [9]. This paper presents the key feature of boundary scan test strategy for interconnect debug and fault diagnosis in the multi-chip modules [10].

In the present work, SoC package includes multiple core dies along with the one Master-Die to control the other dies certainly through package TAP controller. Fig.2 shows the conceptual diagram of the multi-die module and the connectivity among the dies through the master-die.

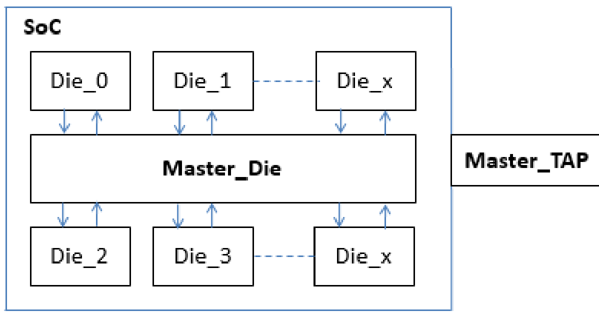

Figure 2 Conceptual block diagram of the Multi-Die Module

The order of connectivity among the several dies is based on the requirement. The next section includes the various modes of connectivity the dies can be accessed in an assembled package. In the multi-die module, the dies can be connected in various fashion which would benefit the accessing of the core dies through the master-die and these are called as slaves of the master-die. The accessing of each die depends on the requirement and is possible through TAP interface at the SoC package level. The mode of accessibility eases the verification process; hence the multi-die module should be connected in such a way that it can be accessed in various modes. Below are the various modes of connectivity among dies in the MDM.

A. *Standard Mode:*

The Standard mode is the default mode in effect on power up or after reset where all the states and registers found with default values. In this mode none of the core dies are selected or functional whereas the master-die should be accessible.

B. *Selected Mode:*

In the selected mode only one die will be accessible at a time through the master-die. The Fig.3 shows the die accessibility through master-die in selected mode.

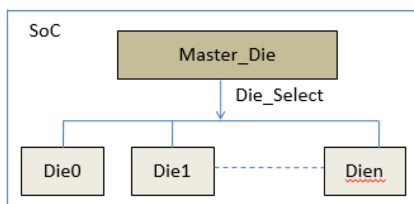

Fig.3 Selected Mode connection

The flow chart of the selected mode verification of the MDM is shown in the Fig.3.1 The master-die contains the Die_SELECT test data register when programmed to the value of '1' selected mode will be enabled. When Die_SELECT TDR of all the dies is set to the value '1', then all the core dies will be snooping for the instruction. With the specific value programmed to the Die_SELECT TDR of master-die, specific die will be selected and available for accessing through the package MTAP.

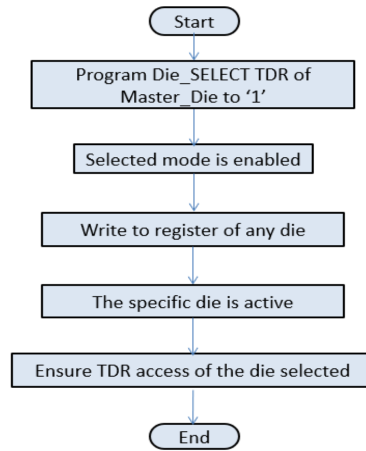

Fig.3.1 Flow chart of the Selected mode operation

C. *Serial Mode:*

The serial mode of operation can be utilized when user wants to access all the dies. All the dies are connected in single chain fashion serially from master-die through serial test data input pins. The output value is obtained from the master-die TDO to the chip TDO. The Fig.4 shows the serial mode connectivity from master-die to the other slave dies.

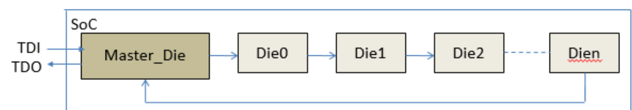

Fig.4 Serial Mode Connection

Fig.4.1 shows the flow chart of the serial mode operation for verification of accessibility among the dies. The serial mode is selected when all the bits of Die_SELECT TDR is programmed to value '1'.

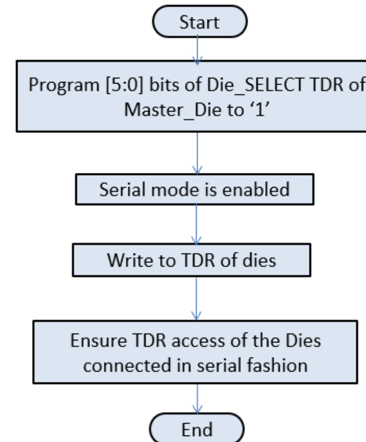

Fig.4.1 Flow chart of the Serial mode operation

D. *Bypass Mode:*

When the dies are connected in serial mode and the particular die is not functional or need not to be accessed, it can be bypassed by programming the Die_BYPASS test data register of the master-die. With the bypass mode test access time can be reduced. The flow chart of the bypass mode is shown in the Figure 5.

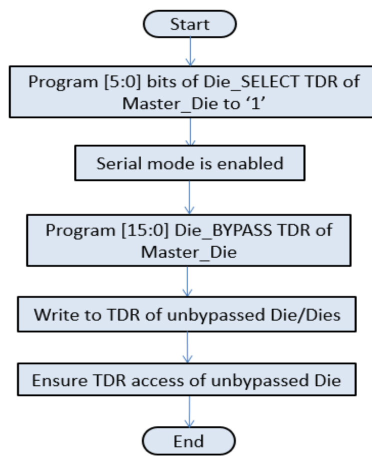

Figure 5. Flow chart of the Bypass mode operation

E. Broadcast Mode

MDM module also has the provision of enabling broadcast among all the dies which allows to program the test data register of all the broadcast enabled dies at the same clock pulse. Hence it accounts for the easy and efficient accessing of all the TDRs provided the TDR of all the dies present at the same level in the design hierarchy. When the unique value needs to be programmed to the identical TDRs of the dies, Die_BROADCAST TDR of the core dies needs to be enabled through which the broadcast mode of connectivity can be utilized which reduces the access time of test data register to the greater extent. Fig.6 shows the flow chart for the broadcast mode of operation.

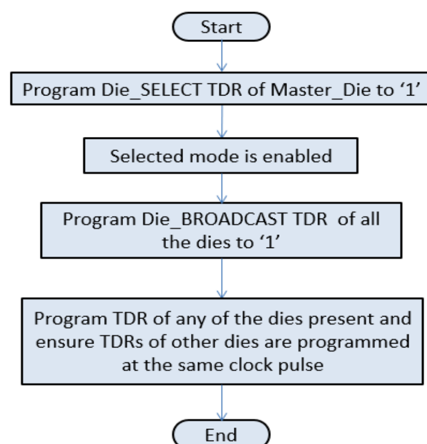

Fig.6 Flow chart of the Broadcast mode operation

This section included the discussions of the various modes of operation for verifying the connectivity among the multiple dies of the SoC.

IV. RESULTS & DISCUSSIONS

The verification of accessibility of internal registers at each level of the hierarchy is performed through the test access mechanism shown in the Fig.1. This section discusses about the waveforms corresponding to the test data register access at each level from package level to core level and multi-die connectivity verification in various modes.

The TDR access at the master TAP controller level is shown in the waveform of Fig.7 Package level TDRs can be accessed and here mainly the IDCODE (Device Identification code) and Manufacturing Identification code of the device is being read.

Fig.7 Read access of IDCODE and MAN_ID registers at MTAP level

The test data register access at the complex or higher level of the network hierarchy which is possible through IP controllers which are IEEE P1687 based controllers. Fig.8 shows the TDR access at the IP controller level which includes many core logics.

The waveform in the Fig.9 shows the core block register access at the leaf level of the hierarchy which is based on IEEE 1500 protocol. The core block is accessed through the IP controllers via master-TAP controller at the package level.

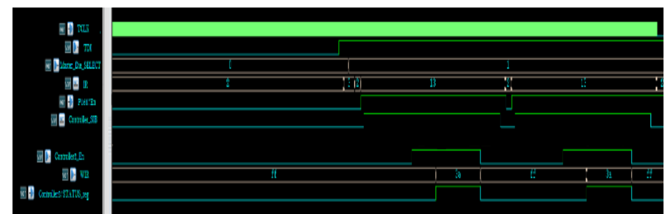

Fig.8 Test data register access at IP controller level through MTAP

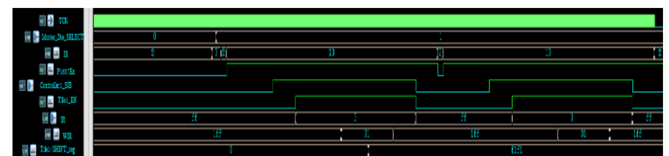

Fig.9 Test data register access at leaf level through TAM via MTAP

The waveforms below describe the verification of various modes of connectivity for the multi-die module SoC package. The Fig.10 shows the register accessibility of the die when selected mode is enabled. Waveform shows test data register access of Die0. Any die can be accessed irrespective of the order of connectivity by programming required bits of Die_SELECT TDR to the specific value of die.

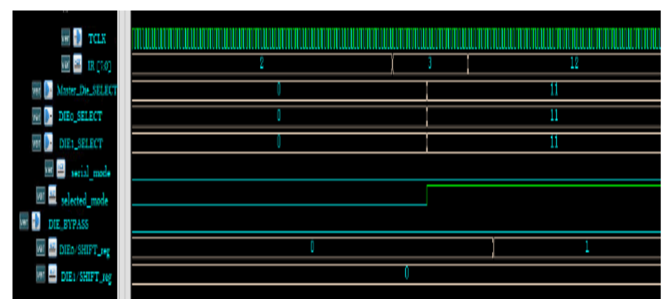

Fig.10 Test data register access of Die0 in selected mode

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The Fig.11 shows the die accessibility when serial mode of operation is enabled, where dies are connected in single chain through serial data input pins as shown in Figure 4. This also gives information on the order the die connectivity in the package. All the dies will be selected through Die_SELECT register where all bits of TDR are programmed to the value '1' and the waveform below shows register access of 2 dies connected in serial mode.

The waveform in the Fig.12 shows the bypass mode of connectivity where specific number of dies can be bypassed by programming the Die_BYPASS register of the master-die. Here the waveform shows that 2 dies are not bypassed to verify TDR write operation where other dies are bypassed in the serial path and not accessed.

The identical registers of various dies are programmed by enabling the Die_BROADCAST register of the specific core dies. Fig.13 shows the register write operation at the same clock pulse with the broadcast mode enabled.

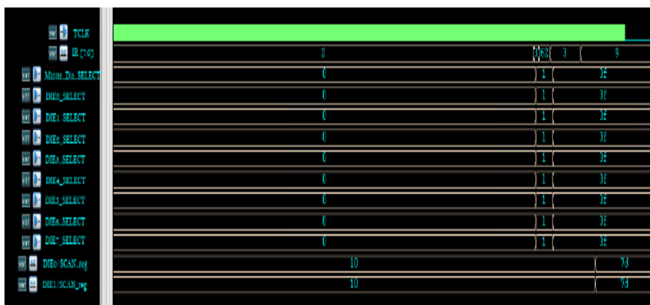

Fig.11 Test data register access of Die0 andDie1 in serial mode

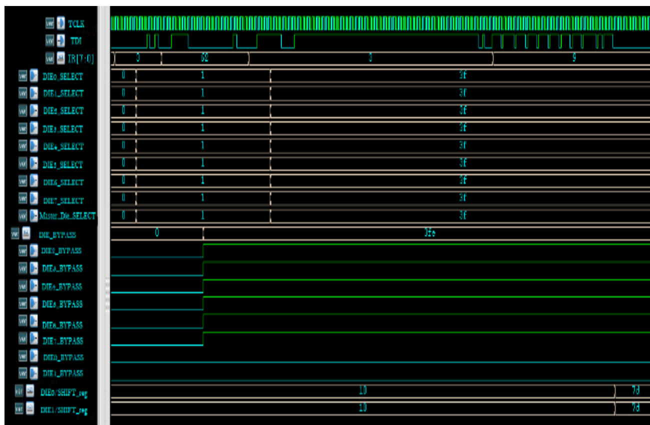

Fig.12 Test data register access of Die0 and Die1 in Bypass mode

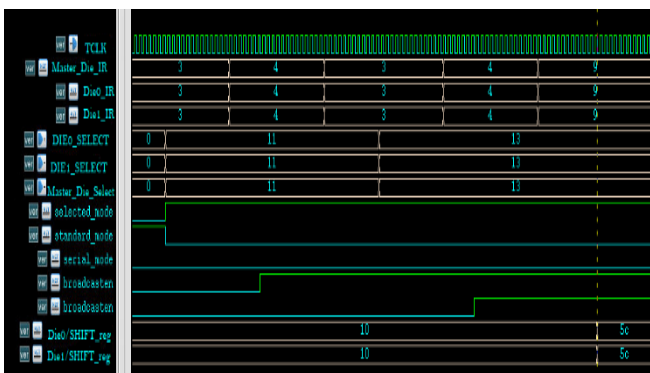

Fig.13 Test data register access of Die0 and Die1 in Broadcast mode

The multi-die module package can contain 'n' number dies assembled onto a chip. Therefore, it is necessary to know the die count in the package pre-verification as it would result in some of the test failure as well as consume unnecessary longer test time. The waveform in the Fig.14 shows the test results for detecting the die count present in the fully assembled SoC package for which Die_DETECT test data register of master-die is programmed.

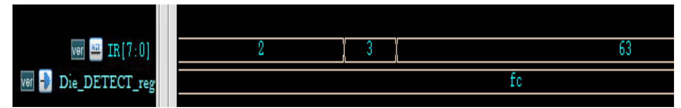

Fig.14 Test data register access to detect number of dies present in SoC

The number of clock cycles to access the test data register of die0 through various modes of connectivity is accounted in the Table I.

TABLE I. No. of clock cycles in register access of Die0 at various modes of connections

Mode of Operation	Selected Mode	Serial Mode	Bypass Mode	Broadcast Mode
#Clock Cycles	128050010	103550001	102550001	101370010

Abbreviations and Acronyms

DFT (Design for Testability), DUT (Design Under Test), MBIST (Memory Built in Self-Test), MCM (Multi-Chip Module), MDM (Multi-Die Module), MTAP (Master-TAP), SoC (System on Chip), TAP (Test Access Port), TAM (Test Access Mechanism), TDR (Test Data Register), TDO (Test Data Output).

V. CONCLUSION

The complex design of SoC accessibility of the internal registers at each level from package level to leaf level is performed through the structured way of test configuration network via IEEE 1149.1 protocol-based test access port. The advancement of the multi-chip module to the multi-die module results in the reduction of manufacturing cost of each chip with better yield. The interconnect verification among the dies proves to be crucial in structural testing for ensuring the proper inter-die communication. Therefore, the register accessibility in various modes of operation facilitates the connectivity verification among the dies through master-die. Each mode has its advantage for specific requirement. Bypass mode connection results in 24% and broadcast mode results in 26% more efficiency in terms of clock cycle consumption than the selected mode of connectivity. The new enhancement in the SoC verification is prior identification of the number of core dies present in fully assembled SoC package. This helps the tester to know the die count and fire the test accordingly which benefits the verification of SoC at platform-based testing.

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