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FPGA Implementation of Contention Free Turbo Decoder for Wireless Communications

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Abstract: ***higher data rates were supported by long term evolution (LTE). When there is higher data rates, error detection and correction of the data goes complex. To solve that problem turbo codes are much efficient. By parallelizing the required procession in turbo decoders, effective high rates are achieved and it reaches the channel capacity much better than other codes. In turbo decoder an interleaver plays a crucial role. An interleaver is much preferable for LTE is Quadratic Permutation Polynomial (QPP). It makes the interleaver which is appropriate in parallel decoding. In this paper, a simple Add-compare-select (ACS) network is proposed instead of QPP interleaver which is efficient. The proposed architecture can be used as both interleaver and deinterleaver. The hardware interleaver is used for high speed low complexity. In turbo coding deinterleaver is used. For the proposed interleaver/deinterleaver doesn't require any memory. The implementation of turbo encoder and turbo decoder is done by a Virtex-6 FPGA and compared the result with QPP interleaver.***

Index Terms:add-compare-select network, FPGA, interleaver, LTE, parallel decoding, QPP, turbo decoder.

I. INTRODUCTION

In 1993 error correction of results will attain to Shannon-limit by the turbo codes were introduced [1].In parallel two recursive convolutional of turbo decoder codes. Iterative algorithm [2] is based on the turbo decoder which is having the maximum a posteriori and interleaver. In MAP decoder and Channel was transmitted by the parity bits and systematic bits. Soft values were captured in MAP decoder and receiver that compute reliability of log-likelihood ratios. A careful design is required for high speed decoding in the process of decoding, which is a vital role of inter leaver.

In wireless communication high rate is the one important requirement. In high throughput sliding method were used for parallel decoders it results in a loss of throughput and silicon area is also increased.For utilizing contention free and QPP interleaver is resolved which were suitable for turbo decoder of parallelization. The problem existing interleaver by the memory which leads to architecture in efficient. Many Architectures were introduced as master slave batcher network[6]. Deinterleaver is another block in the turbo decoding that has inverse operation in its original order.

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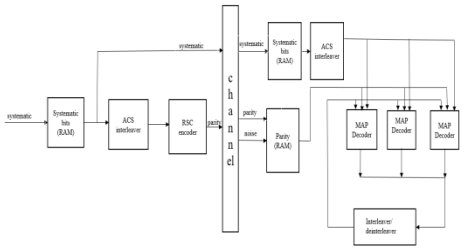

Figure 1: Architecture of turbo decoder and encoder

Although some works are introduced to find the QPP interleaving in quadratic inverse [4] which makes more complex hardware as well as more area will be consumed by the use of deinterleaver-free architecture [8], for deinterleaving architecture is still missing efficient of deinterleaver is still missing in efficient VLSI architecture. In this paper, turbo decoder is proposed which uses an add-compare-select (ACS) network. Fig.1 shows the proposed turbo communication system architecture that reduce the complexity and increases the latency.

II. ACS INTERLEAVER

A parallel turbo decoder of key design parameter which is working in a parallel is MAP decoders. All blocks were multiplied by eight and the designed is N=8 which is achieve by maximum by proposed architecture .In LTE all blocks were decoded in parallelism. For specific size it can be order by parallelism which can easily adopted.

A. Network for Add-Compare-Select(ACS) Permutation

An interleaver involves of permutation and address generator block (Fig.2), the values of *K* LLR were stored in the column wise in a folded memory. I *S* rows were defined so trellis segment is for Sand $N \times S = K$ and number of parallelization units are defined by N. each addresses in folded memory were started from 0 to descending order which can denote the small interleaved rows which were associated. In LLR values every row was denoted non interleaved and folded memory. The values of S in consecutive addresses were difference between them.

The interleaved addresses were address generator computed which were taken by permutation order. The networks for ACS permuting were proposed one which is seen in Fig.3 & Fig.4, involves in selection units, adder and comparison. With address generated by the small address comparison .The creation permutation is unit. From the trellis segment the address by folded memory were sorted in ascending order. The adder of output is sent till the permutation signal was obtained. For scrambling inputs, in which the selection unit having N multipliers for N inputs in the permutation signals. The network is proposed in VLSI architecture to enhance the results of implementation. So 37.8% energy consumption was found which is compared with the existed art of state.

B. *Generator for Address*

Inputs were generate by the addresses based on [3] is proposed as ACS permuting network in a way of recursive, were seen in the equations below.

$$\pi(i) = f1.i + f2.i2 \ (mod\ K), \qquad (1)$$

$$\pi(i+\tau) = f1.i + f2.i2 + f1.\tau + 2.\tau.f2.i + \tau 2.f2 \ (mod\ K),$$

$$= \pi(i) + \gamma(i) \ \ (mod\ K), \qquad (2)$$

$$\gamma(i) = f_1 + 2.\tau f_2.i + \tau^2 f_2 \qquad (mod\ K), \quad (3)$$

$$\gamma(i+\eta) = \gamma(i) + 2.\tau^2 f_2 \qquad (mod\ K). \quad (4)$$

interleaver with an adder blocks is used for generating the input bits from the address is named as address generator by using a permutation circuit as shown in Fig.2 In memory M LLR values are stored where M is given as M= K*T is for number of parallelization K units and T trellis segment. The smallest address is denoted by the folded address in ascending order from row 0 address. Adding to folded memory address of value T and the result in address is computed by comparing the address generator. In comparison block as shown in Fig.4

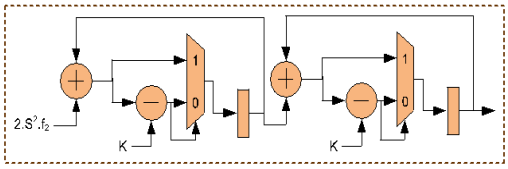

Figure 2: The Serial Address Generator Block.

C. *Interelaver/Deinterleaver Block*

Deinterleaver is the most demanding block in turbo decoder. To execute generator block create address of generator block in QPP inverse. The cubic inverse of sizes of block, large in more complexity in hardware in addresses block. All block sizes for better solution in simple architecture were needed. By replacing interleaved addresses a small addresses is achieved by adding in the generator by adding MUXs of two inputs were seen in Fig.3.

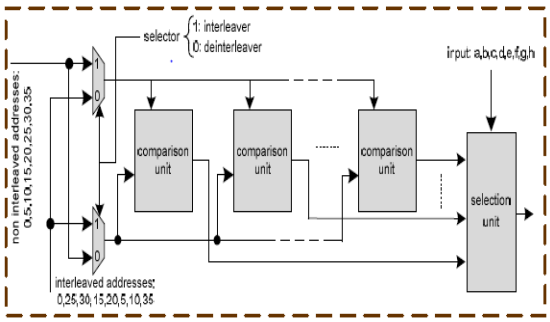

Figure3: Block Diagram for Selecting Interleaver/Deinterleaver.

The address generator of this method by using addresses was to compute an adder by simple implmentation. Extra hardware is required for the proposed deinterleaving.

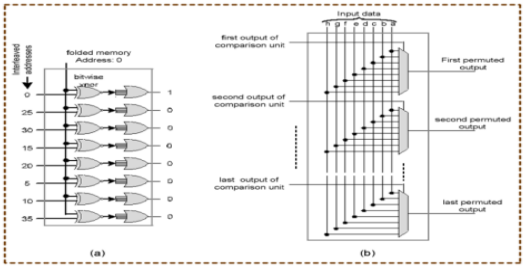

Figure 4: a) Compare unit b) Selection unit.

III. TURBO ENCODER

In a turbo encoder a code can be formed from the concatenation of two codes separated by an interleaver. The two RSC encoders used are identical to each other as shown in Fig.5. The data is in a form of systematic i.e. the input bits are also available at the output. General architecture for systematic recursive codes of convolutional were seen in Fig.6 the interleaver scrambles the bits in a pseudo-random order. The turbo encoder is built using two systematic recursive encoders of convolutional those have parallel concatenation, an RSC encoder of RSC is typically ½=r and is also called as component encoder.

The main purpose of interleaver is to randomize burst error patterns so that it can be correctly decoded. This increases the distance of the turbo code. In this only one of the systematic outputs from the two encoders is used for the transmission, because the systematic output from the other component encoder it only has ashuffled systematic output. Turbo encoder with an add-compare-select network as interleaver is proposed needs only one recursive systematic convolutional encoder but the operation is same as generic turbo encoder i.e. using of two identical RSC encoders. For one of the RSC encoder data is non interleaved i.e. systematic data is given as input to it and for the second RSC encoder interleaved data is used as input.

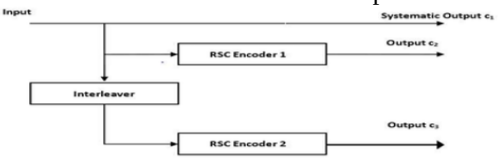

Figure 5: General Turbo Encoder Block Diagram.

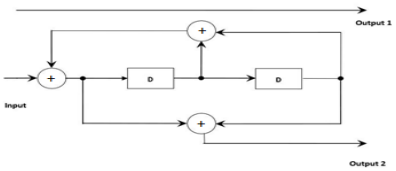

Figure 6:RSC Encoder obtained from the Conventional Convolution Encoder with r = 1/2 and K = 3.

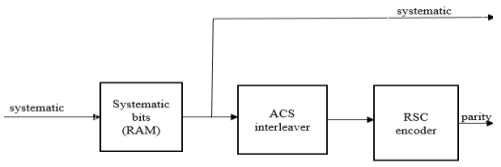

Figure 7: Proposed Turbo Encoder with ACS Interleaver.

Turbo encoder with an add-compare-select network as interleaver is proposed are shown in Fig.7 needs only one recursive system For one of the RSC encoder data is non interleaved i.e. systematic data is given as input to it and for the second RSC encoder interleaved data is used as input. Among this two outputs only one is taken as parity by using this method we can decrease the hardware requirement.
In the interleaver we are adding two Multiplexer with the help of that we can form any one RSC encoder .from this we can get the desired output and it is stored in a memory at turbo decoder side.

IV. TURBO DECODER

The iterative decoding technique is used for the turbo decoder and it is parallel in nature to get high throughput rates. It achieves by dividing block into sub blacks of N with S length in the N MAP processor. Which means more silicon area is required and difficult to implement. By using ACS as the interleaver it will solves all the disadvantages arrived by using QPP interleaver like large power consumption.QPPinterleaver is used by the LTE whose input and outputs are followed by:

$x'_i = x_{\pi(i)}$, $i = 0, 1, 2, \ldots, K-1$, (5)

where K is the code block size and $\pi(i)$ is:

$\pi(i) = f_1.i + f_2.i^2 \pmod K$ (6)

Where the parameters $f1$ and $f2$ depend on the block size K. This property of the QPP interleaver, makes it contention-free if for all $t1 \neq t2$ the following expression is satisfied:

$$\lfloor \pi (j + t1S) / S \rfloor \neq \lfloor \pi (j + t2S) / S \rfloor, \quad (7)$$

Where $0 \leq j < S$, $0 \leq t1, t2 < N$.

Vectorizable is in interleaver of QPP [7]. In [5] it is proposed the interleaver bottleneck [7]. Block sizes of *K in LTE in* the range of 40 to 6144. In [8] it is showed that the inverse of QPP is also made from QPP interleavers. Therefore, the algorithm for interleaving can also be applicable for the deinterleaving process. Although QPP inverse exists for most of the block size but for some blocks it is very difficult to apply the same algorithm whose hardware implementations incur a very high computational complexity [8].

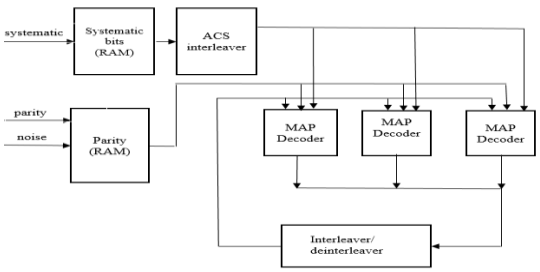

Figure 8: Parallel Turbo Decoder Architecture.

The proposed turbo decoder consists of two Maximum-a-posteri(MAP) decoders [4], interleaver and interleaver/deinterleaver blocks. The data stored in RAM of systematic bits those are scrambled and given as one of the input for MAP decoder. Noise added through channel and parity are given as second input to the MAP decoder and the third input is generated from the interleaver/deinterleaver. It is an iterative process when the input of the encoder and decoder output is same then it comes out of the loop.

V. SIMULATION RESULTS & COMPARISON

The proposed architecture is designed using Xilinx ISE design suite 14.7 and it is implemented on vertex 6 FPGA.\

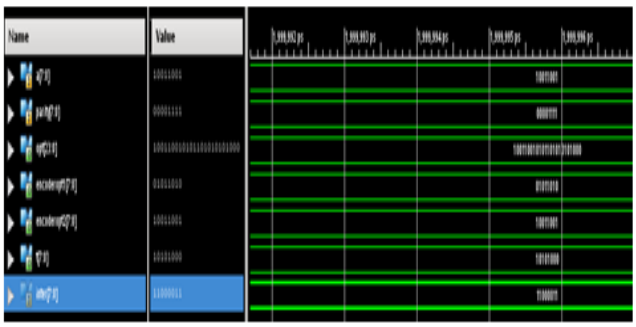

Figure 9: Simulation Results for Turbo Encoder.

Fig.9 shows the simulation results of turbo encoder block,a[7:0] is the systematic data generated from the address generator, inter[7:0] is the ACS interleaved data of a[7:0], t[7:0] is the noise generated from channel, parity[7:0] is the parity bit for the encoder block and the output opt[23:0] of encoder block is 24 bit data which is given as input to decoder block.

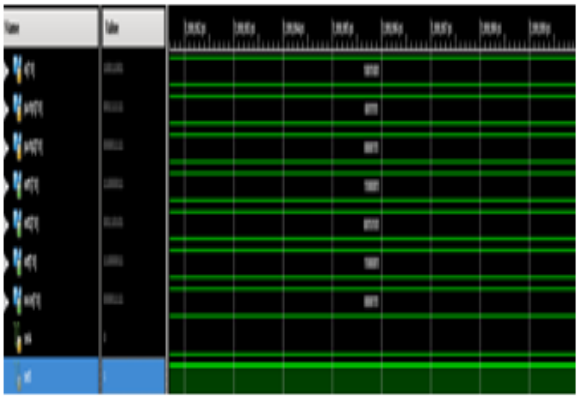

Fig.10 shows the simulation results in ACS

interleaver/deinterleaver. Input of the interleaver block is systematic bitsa[7:0] given as in[7:0], sel4 and sel5 are given to choose interleaver or deinterleaver operation, out1[7:0] is the interleaved data at turbo encoder block and out2 is the deinterleaved data at turbo decoder block. These data is used inside the turbo encoder and decoder blocks.
Fig.11 shows the simulation results of turbo decoder block a[23:0] is the input for the turbo decoder block, inter[7:0] is the ACS interleaved data from systematic bits, decoder2[7:0] is the first iteration decoder output, which given to deinter[7:0] and it is given to the second iteration decoder decoder1[7:0], from the decision box results are comparedand found that a[7:0] and decoder1[7:0] are same then the iteration stops and gives the result which are turbo encoder input and turbo decoder output respectively.

Hence it is proved that the input to the encoder and the output to the decoder is same. Which makes this work to use higher rates also this proposed work has a block size of k =6144 and the width is 8bits. As we applied a pipeline technique a higher date is obtained. It is known that the basic interleavers like row-column, pseudo random, etc., are effective but for higher rates those are not usable the computation increase gradually when the data rate increases so QPP interleavers are proposed in [4].

It consumes lot of area and delay so we are going to use

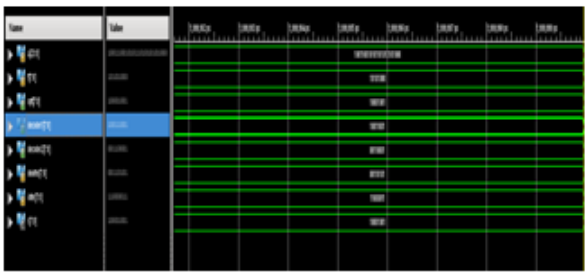

Figure 11: Simulation Results for Turbo Decoder.

ACS network as to replace QPP interleaver.

The full FPGA implementation of turbo decoder using QPP interleaveris given in [4]. From that the area and timing analysis are compared with ACS interleaver.

Table1:Comparison between QPP Interleaver and ACS network Interleaver.

Type	Area analysis(LUT)	Timing analysis (ns)
QPP interleaver [4]	859 LUTS	24.509ns
ACS network Interleaver	296 LUTS	19.962ns

Table.1 shows the comparison between QPP interleaver and ACS interleaver from the table it is clear that ACS network interleaver hardware efficient than QPP interleaver because by using ACS interleaver technique some components are not needed so that it reduces the time taken for simulation and area.

VI. CONCLUSION

In this paper it is proved that ACS interleaver is much preferable than QPP interleaver in a communication system using turbo codes. Due to less computational complexity and hardware efficient the proposed technique can be utilized for satellite communication with simple changes like adding decoders in turbo decoder block in future. It also achieves channel capacity, high throughput and low latency with higher data rates.

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