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Analysis of Various Master-Slave Configuration based D Flip-Flops

Shivali, Shobha Sharma, Amita Dev

Abstract: ***The needs of fast devices are growing day-by-day and so flip flops are coming into picture. For many digital devices flip flops are the elementary unit for construction. They are termed as one bit memory element. This paper enumerates review on various earlier proposed master slave configuration based D flip flop models including respective circuits and their description. It includes NAND logic gate based D flip flop, NOR logic gate based D flip flop, 2x1 mux based D flip flop including MTCMOS technique and transmission gate based D flip flop .All these topologies are used to develop D latch which are then converted into D flip flop by the cascading of two D latches in master-slave configuration***.

Index Terms**: D flipflop, Gates, Master-slave configuration, Multiplexer**

I. INTRODUCTION

Flip-flops are the basic unit for creation for the digital models. Each flip flop performs the storage of one bit. Flip flop is always clocked. Flip flop is either positive edge triggered or negative edge triggered which implies that the input affects the output when the clock is going low-to-high or high-to-low, respectively. Flip flops are called single edge triggered flip-flop when the data storage is done either on rising or on falling edge of the clock. Also, they are known as dual edge triggered when the data storage is done on both falling as well as rising edge of the clock.

During past years, the designers were more tilted towards the silicon area consumption and its performance. The power dissipation was also one of the parameters. Moreover, cost and reliability also gained dominance. Power consumption is being provided significant note as compared to the speed of operation and Silicon area consumption, as the trend at rapid pace has been inverted in recent past years. Power dissipation and propagation delay are the main issues for device performance. One basic ingredient in any integrated circuit is power consumption.

In this paper, review of number of various master-slave configuration based D flip flops like NAND logic gate based D flip flop, D flip flop based on NOR logic gate, 2x1 multiplexer based D flip flop including MTCMOS technique and D flip flop based on transmission gate are presented.

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***** Correspondence Author

Shivali*, Department of Electronics & Communication Engineering, Indira Gandhi Delhi Technical University for Women, Delhi, India.

Shobha Sharma, (Corresponding Author) Assistant Professor, Department of Electronics & Communication Engineering, Indira Gandhi Delhi Technical University for Women, Delhi, India.

Amita Dev, Pro Vice Chancellor, Indira Gandhi Delhi Technical University for Women, Delhi, India.

II. DIFFERENT IMPLEMENTATIONS OF MASTER-SLAVE CONFIGURATION BASED D FLIP-FLOP

A. D flip flop using NAND gate

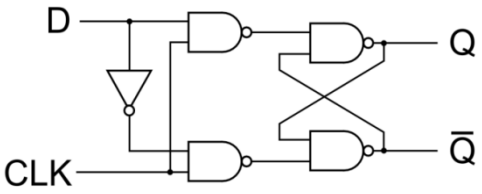

Figure 1: NAND based D Latch

As Figure 1 shows the D latch which is made by logic gates namely NAND gate and one NOT gate. It consists of four NAND gate. Each NAND gate is made by CMOS logic having four transistors out of which two are NMOS and two are PMOS connected in push-pull configuration. D-latch can be made by SR latch by giving complimentary inputs to S and R inputs of SR latch. The D flip flop can be constructed by cascading two D latches back-to-back in master slave configuration as shown in figure 2 below.

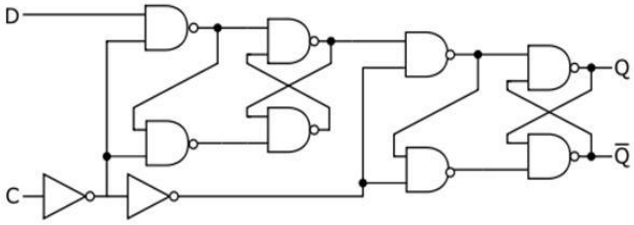

Figure 2: NAND based D flip flop based on master slave configuration

B. D flip flop using NOR gate

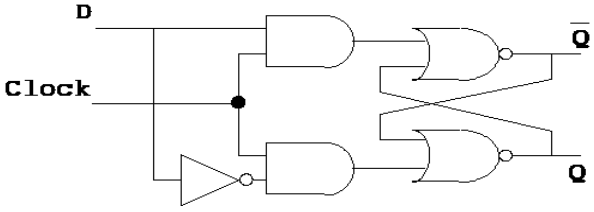

Figure 3: NOR based D Latch

Figure 3 shows the D latch which is made by logic gates namely NOR gate, AND gate and one NOT gate. It consists of two NOR gates.

Each NOR gate is made by CMOS logic having four transistors out of which two are NMOS and two are PMOS connected in push-pull configuration. D-latch can be made by SR latch by giving complimentary inputs to S and R inputs of SR latch. As shown in figure 4, by back-to-back connection of two D latches in cascade fashion D flip flop can be build.

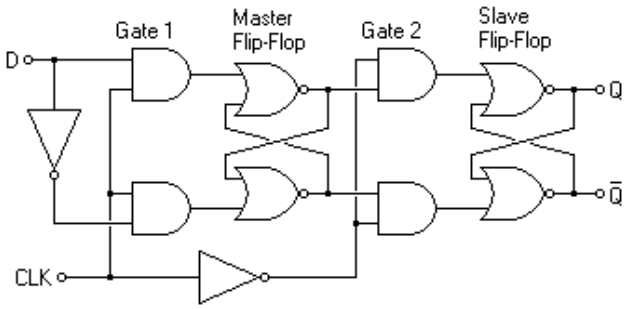

Figure 4: NOR based D flip flop based on master slave configuration

C. D flip flop using Multiplexer

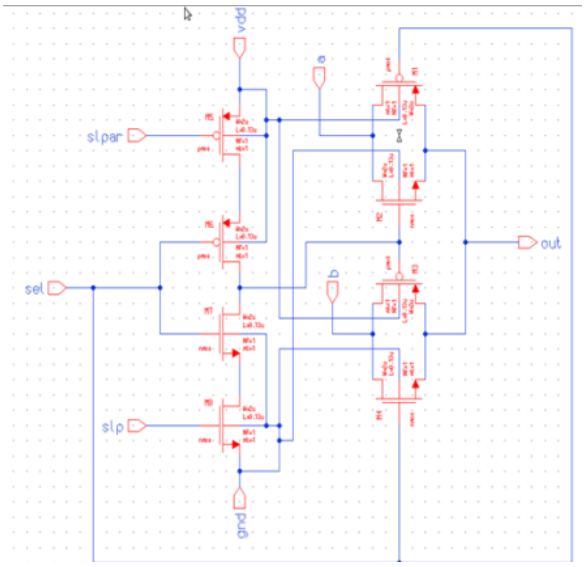

Figure 5: Schematic of 2:1 mux D latch using MTCMOS technique

A D latch can be made using a 2x1 multiplexer. Then this D latch can be further used in master-slave configuration to make a D flip flop. The multiplexer can be made using transmission gate. Further the performance of the conventional CMOS multiplexer can be enhanced by using MTCMOS technique and transmission gates.

For obtaining, low power consumption and high performance circuit design, MTCMOS (Multi-Threshold CMOS) technique is use. MTCMOS technique uses low, moderate and high threshold voltage transistors. The sleep transistor which is connected between the PMOS circuitry and the power supply (i.e., Vdd) enhances the performance of the device when it is ON, whereas the sleep transistor connected between the NMOS circuitry and the ground terminal is used to dissipate less power when it is in OFF mode.

The figure 5 shows the schematic of 2:1 multiplexer by using MTCMOS Technique.D latch using 2x1 multiplexer is shown in figure 6 which is further used to make D flip flop in master slave configuration as shown in figure 7.

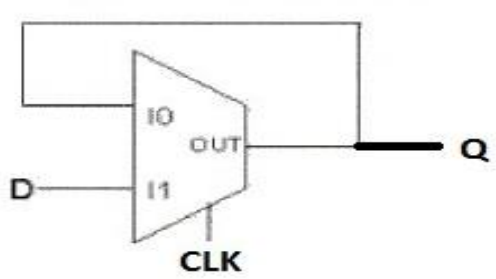

Figure 6: Symbol of D Latch using mux

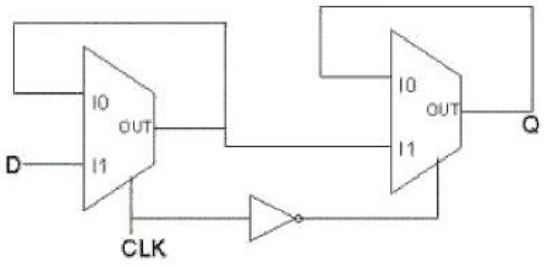

Figure 7: 2:1 MUX based D flip-flop using MTCMOS technique

D. D flip flop using Transmission gate

The circuit shown in figure below depicts two CMOS transmission gate (TG) switches and a basic two-inverter loop.

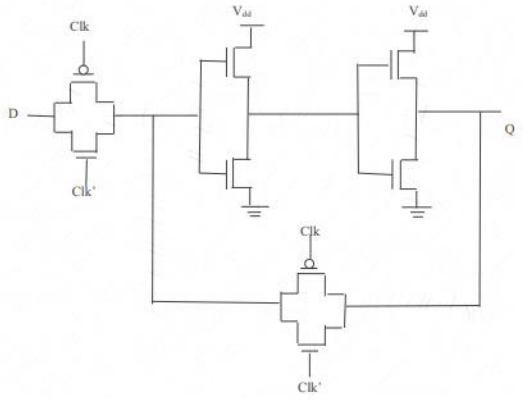

Figure 8: Transmission Gate based D-Latch

By theory, two field effect transistors are used to make a transmission gate. In this, the substrate terminal and source terminal are not internally connected in contrast to the former discrete field effect transistor. Due to the parallel fashion connection between the NMOS and PMOS transistors, the connection only between the drain and source terminals is present. For the formation of control terminal, the transistor's gate terminals are connected to each other by inverter. In opposite with discrete FETs in which there is no connection between the substrate terminal and source terminal, for ensuring parasitic substrate diode to be reverse biased always for not affecting the signal flow, the substrate terminals are linked to their respective supply voltages.

The positive supply potential is thus supplied to the substrate terminal of the PMOS whereas the negative supply potential is supplied to the substrate terminal of the NMOS.
When the clock is high, the input terminal TG gets activated whereas when the clock is low, the inverter loop TG is activated. When the clock is high, the input signal is accepted and it is retained when the clock is low as the state of the inverter.

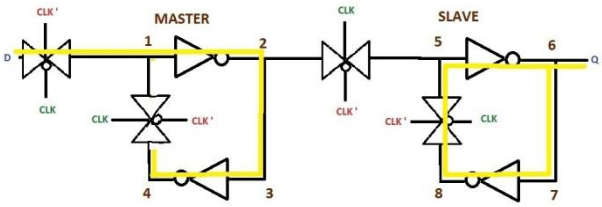

Figure 9: D flip flop by Transmission Gate based on master slave configuration

III. CONCLUSION

On the basis of above stated reviews of different Master-Slave configuration based D Flip Flop models, it can be concluded that they require significant amount of area, i.e., more number of transistors are utilized in this type of topology. Also more delays are produced due to which more number of elements in the circuits. Moreover, the use of clock signal and inverted clock signal arises the clock skew issue.
So, there arises a need of concept which requires fewer numbers of transistors and also reduces the propagation delay of circuit along with maintenance of low power dissipation in the circuit too.

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AUTHORS PROFILE

Shivali is persuading her B.Tech in the discipline of Electronics & Communication Engineering for Indira Gandhi Delhi Technical University for women (IGDTUW). Her area of interest includes Digital Circuits & Systems and VLSI design.

Shobha Sharma is Faculy in Department of Electronics and Communication Engineering in Indira Gandhi Delhi Technical University for Women (IGDTUW)Delhi . Her area of interest includes Nanocmos issues and challenges at the frontend and backend of Chip designing. She has many research papers in international Journals including Scopus indexed journals.

Amita Dev is the First Pro-Vice Chancellor of Indira Gandhi Delhi Technical University for Women. She has excellent track record of Administration quality Teaching, Innovation and Research. She has passion for Teaching and Research. She has published 63 + research papers in International and National Journals and Conference Proceedings. She has more than 33 years of experience in Industry, Teaching, Research and Administration. Her teaching and research areas include Artificial Neural Networks, Speech Processing, Opportunistic Networks, Speech Recognition Systems, MANETS, Advanced Computer Networks, Data Mining etc.