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High Speed ALU Design using Vedic Neurons for Energy Efficient Sensor Nodes

Saji. M. Antony, S. Indu, Rajeshwari Pandey

Abstract: ***Achieving low power consumption is a major challenge in designing any wireless sensor node. In a sensor node, major domains of power consumption are during Sensing, Communicating and information processing. Sensor nodes consume maximum power during data communication. Energy consumption for processing data is very less compared to energy consumption for communication of data. So processing data locally at each node in a sensor network, is important for minimizing power consumption. High processing speed and low area designs are in ever growing demand. In order to predict outcomes, based on previous inputs, ALU can be designed with neurons. Processing speed of ALU can be improved by replacing conventional multipliers with Vedic multipliers. This paper suggests implementation of high speed ALU using Vedic Neurons. Proposed design has been simulated using Active HDL and Xilinx ISE in order to compare with existing conventional ALU. The analysis of the results shows that the proposed design leads to reduction in the delay and reduction in LUT count (an indicator of area) of the ALU.***

Index Terms: ***Artificial Neural Networks, Vedic Algorithm, Urdhava Triyakbhyam, Vedic Neuron, ALU Design.***

I. INTRODUCTION

Current advances in silicon technology, micro-electro-mechanical systems, embedded systems, wireless communications and computer technology, have enabled the design of small, low cost, multifunctional sensor nodes. A wireless sensor network (WSN) consists a collection of such sensor nodes used for various applications including precision agriculture, transportation, habitat monitoring, structural health monitoring, medical monitoring, military surveillance and many more [1]. Fig.1 shows block diagram of a sensor node.

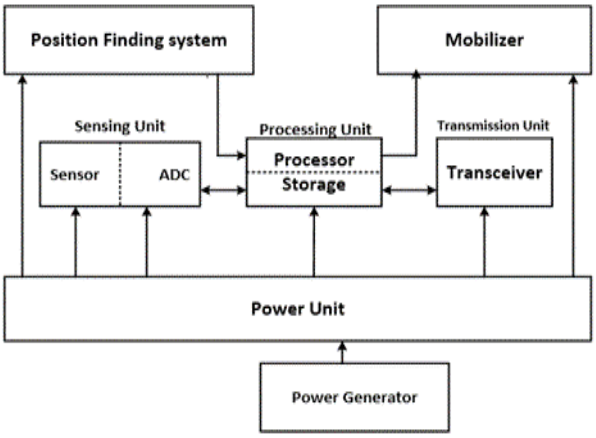

Fig. 1. Block diagram of a Sensor Node [1]

Sensor nodes are battery powered devices, with limited, irreplaceable power. Hence, low energy consumption requirement is the most crucial constraint of sensor nodes, as life of a sensor network mainly depends on its energy consumption. So, energy utilized by each and every part of individual nodes precisely affects the life of the complete network. This leads energy optimization more complicated, as it involves increasing life of sensor network by reducing energy consumption. This can be achieved with energy awareness in every step of design and operation [2]-[3].

In WSN, primary functions of sensor nodes are to detect events, process and transmit data. Therefore, major domains of power consumption are during Sensing, Communicating and data processing. Among these three domains, maximum energy consumption is during data communication. Energy consumption for processing data is very little compared to communicating data. So instead of transmitting raw data, sensor nodes carry out simple computations locally, then transmit partially processed required data. Hence, local data processing is very important for low power consumption in a WSN [4]. For many real time applications like monitoring battle field, controlling of environmental conditions, sensor nodes require fast processors for processing the detected signals. High speed processing and low area design are essential requirements for sensor nodes in an efficient WSN. This paper addresses on the implementation of high speed ALU using Vedic Neurons realizing faster computational speed and lower area than that achieved with current standards.

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***** Correspondence Author
Saji. M. Antony*, Research Scholar, ECE Dept, Delhi Technological University, New Delhi.
Assistant Professor, ECE Dept, Bharati Vidyapeeth's College of Engineering, New Delhi. India
Dr. S. Indu, Professor, ECE Department, Delhi Technological University, New Delhi. India
Dr. Rajeshwari Pandey, Professor, ECE Department, Delhi Technological University, New Delhi. India

II. RELATED WORK

Recent advances in technology have enabled dense deployment of small, inexpensive sensor nodes. These sensor nodes are capable of data processing and communicating. But they have constraints on energy and computation. Due to the wide range of applications, a lot of research has been focused on power dissipation, physical size and processor design of sensor nodes. M Hempstead *et al.* focuses on architectural design with application driven approach in [5]. Platform independent, content aware data management architecture of power aware processors for WSN are recommended in [6]. To overcome crucial constraints like power utilization, volume speed, and to achieve greater performance for real time applications of sensor nodes, several architectures have been discussed and reviewed in references [7-10]. As most of the power is consumed in data transmission, the importance of low power transceiver design is explained in [11]. In reference [4], authors emphasized the necessity of local data processing at each sensor node. Data processing consumes much less energy compared to communication. So sensor nodes carry out data computation and transmit partially processed required data in place of entire raw data. A Munir *et al.* explain compromise between communication and data processing for many applications and permits transmission of event driven data to conserve energy [12]. So design of high speed low area processors, are important for many applications in wireless sensor networks. J A bailey *et al.* investigate structure of neuron and explains basic behaviour of biological neuron in [13], and this behaviour is emulated in an artificial neuron. Implementation of network model for neurons and synapses are demonstrated in the paper. In reference [14], complicated models of biological systems are accurately simulated. Neuron model VHDL library has been established which empowers a wide variety of complex neuron systems. Availability of standard library allows to implement complex neuron system on field programmable gate array (FPGA). Using artificial neural network (ANN), as basic building block, digital logic circuits are realized, and verified in [15]. Using ANN, 5-bit ALU is designed in the paper. By using Vedic algorithm, computation speed of single neuron is increased in [16]. Using Vedic Mathematics, Anshika et.al implemented high performance neuronal logic gates in [17]. High speed neural network has wide range of applications like medical applications, image compression and many more.

III. PROBLEM FORMULATION

This paper focuses on designing a high speed ALU using Vedic Neurons. A conventional ALU is less capable of intelligently predicting outcomes based on previous inputs. Its neural counterpart, on the other hand, aims at improving its prediction capabilities by employing an activation function and making it an intelligent ALU. But ALU designed with neurons suffers from bulky and slow architecture. This can be solved by implementing the Vedic logic in all arithmetic and logical operations performed. The Vedic logic helps in performing faster calculations by utilizing simple techniques to solve complex problems. This provides a faster and a smarter ALU design. This work is intended for laying a foundation for the intelligent sensor nodes by implementing Vedic logic on neural platforms.

IV. ARTIFICIAL NEURAL NETWORKS (ANN)

Research on ANN has been inspired from the complex structure of human brain. Using neurons, human brain can compute much faster than equivalent digital hardware circuit. The computation can be viewed as a system in which, external stimulus sends input to receptors. The function of receptors is to transform the received stimulus from outside into electrical impulses. These electrical impulses carry information to the neural net. According to received electrical impulses, the neural net sends information to effectors. These effectors issue an excellent response to stimulus as shown in fig. 2. The brain is composed of an integral constituent known as neuron. By training these neurons, brain is skilled to differentiate contrasting patterns and gives appropriate output. Behavior of a brain can be emulated with the concept of ANN. ANN is a parallel distributed unit, consisting of many highly inter linked processing elements, known as artificial neurons. These processing elements store experiential knowledge and make it available for further use. Analogous to human brain, ANN also acquires knowledge through learning process from environment. The learned knowledge is stored in interneuron connection strengths as synaptic weights. An ANN is a collection of interconnected nodes known as artificial neurons. Artificial neuron is a simplified model of biological neuron in a human brain. The connections between artificial neurons transmit signals from one neuron to another inter connected neuron. Received signals are processed by artificial neuron and it, in turn, signals other inter connected neurons. In ANN implementation, the signal at the connection between neurons is always a real number. The output of a neuron is arrived at by a non-linear function of total of its inputs. The artificial neurons and connections have weights that adapt itself with ongoing learning experience. These weights control the signal strength at the connections. Artificial neurons have a threshold value and signal will be transmitted by neurons only when the aggregate signal exceeds the value of threshold

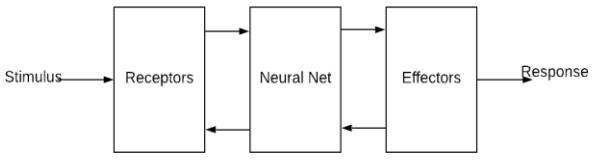

Fig. 2. Block Diagram of Nervous system [16]

Primary objective of ANN is to resolve problems in a similar manner in which a human brain would have solved it. However, with passage of time, focus has been shifted from biology to matching peculiar tasks.

ANNs have wide use in applications like medical diagnosis, computer games, speech recognition, computer vision, social network filtering, machine translation etc.

A. Components of ANN.

The model of basic artificial neuron is shown in Fig. 3. The basic components are weighting factors, summation function, activation function and transfer function.

1) Weighting Factors: Weights are adaptative coefficients which determine strength of input signal. Each input has its own corresponding weight.
2) Summation Function: Considering (x1, x2 . . . xn) as inputs and (w1, w2 . . . wn) as relative weights, Product of these two vectors gives total input. Total of all these products are derived in the summation function
3) Activation Function: Summation functions are passed on to nonlinear filter called activation function. The activation function enables the summation output to change with respect to time. The activation function used in our neuron is the linear function for the bias.
4) Transfer Function: Neural output is calculated by comparing summation with threshold in the transfer function. If summation is greater than threshold, a signal is generated by the processing element. If total sum is less than threshold, no signal will be generated.

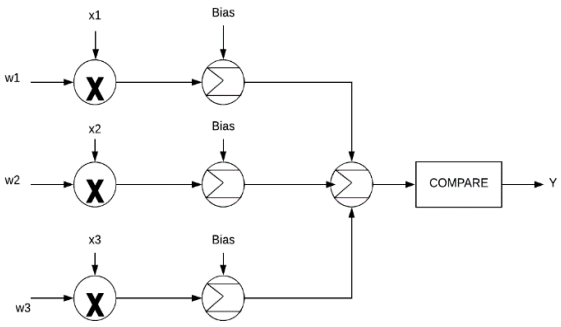

Fig. 3. Basic Artificial Neuron Model [16]

B. Advantages of ANN

Key advantages of ANNs make them capable of solving certain specific problems and situations, as under:

1) ANNs can memorize and represent complex and non-linear relationships. So ANNs have great importance in real life situations due to complex and non-linear nature of relations of inputs and outputs in real life.
2) After analysing inputs and their relationships, ANNs can predict unobserved relationships on undetected data, and can generalize the model.
3) Unlike other prediction methods, ANNs do not impose any constraints on the input parameters. Also research has shown that ANNs have better ability to learn hidden relationships in the data without applying any established relationships in the data [16].

V. VEDIC MATHEMATICS

Vedic mathematics is an ancient renowned mathematical approach that can be applied to resolve many mathematical challenges in the present day situations. It was recreated by famous mathematician, Sri Bharati Krishna Tirthaji. Based on his studies, Vedic approach is derived from 16 Sutras (formulae), which can apply to all branches of mathematics. One of the sutras for multiplication, known as Urdhava Triyakbhyam has been implemented in this work.

Urdhava' literally conveys "vertical and cross-wise". Urdhava Triyakbhyam Sutra proposes vertical and crosswise multiplication for obtaining the partial products and their simultaneous addition. Vedic multiplier is independent of clock frequency due to above parallel processing. A 2x2 Urdhava multiplier implementation is shown in Fig. 4 and Fig. 5. Due to its regular structure, this multiplier can be further extended to higher inputs easily [18].

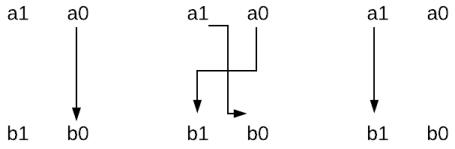

Fig. 4. Urdhava multiplication method for 2 bit binary numbers.

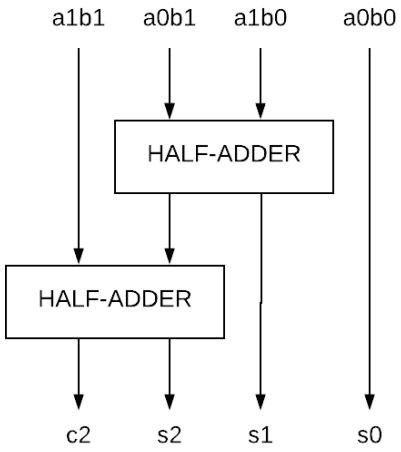

Fig. 5. Block diagram of 2x2 bit Urdhava multiplier

VI. PROPOSED DESIGN

To make ALU suitable for sensor nodes, ALU using Vedic Neurons is proposed in this work. Use of Neurons in the design, gives prediction capability by employing activation function and helps to design an intelligent ALU. To improve the processing speed and efficiency, conventional multipliers in the Neurons are replaced with Vedic Multipliers using Urdhava Triyakbhyam Sutra. Using these Vedic neurons, arithmetic and logical functions have been implemented. The logic gates are designed according to individual truth table conditions.

Threshold values and weights are also selected as per the gates. For modelling the AND gate, threshold values and weights can be set as given below:

$w1\ x1 + w2\ x2 - \Theta < 0$ i.e. $\Theta > 0$ (when $x1 = x2 = 0$)

Similarly, for other cases,

$w1x1 + w2x2 - \Theta < 0$ i.e. $w2 < \Theta$

$wl\ xl + w2x2 - \Theta < 0$ i.e. $w1 < \Theta$

wl xl + w2x2 - Θ ⩾ 0 i.e. w1 + w2 ⩾ Θ

x, w and Θ are the input, weight and threshold respectively. Similarly other gates can be designed.

VII. SIMULATION RESULTS

Our design of ALU has been coded in Active HDL and verified through simulation using Modelsim SE 6.4. The Active HDL codes of the ALU were synthesized using Xilinx ISE 14.7.

Eight-bit Vedic multiplier using Urdhava Triyakbhyam has been implemented and its simulation results are shown in fig. 6. Fig. 7 shows simulation results of designed activation function. Using above Vedic multiplier and activation function, Vedic neuron has been designed. Simulation results of designed Vedic Neuron are given in Fig. 8.

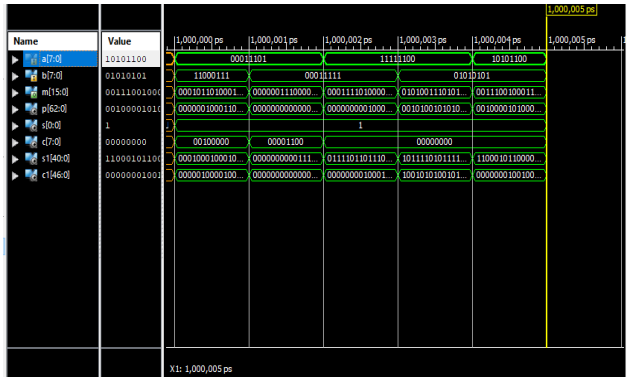

Fig. 6. Simulation results of 8-bit Vedic Multiplier

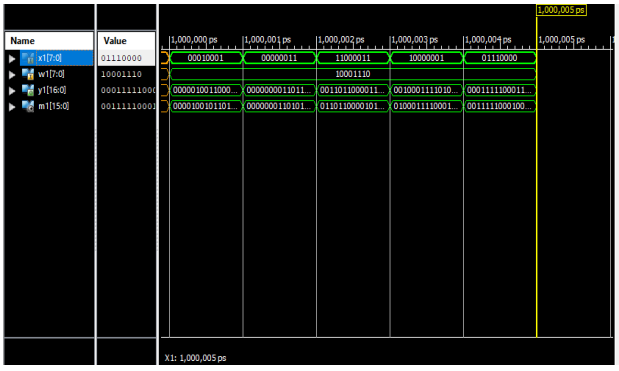

Fig. 7. Simulation result of Activation Function

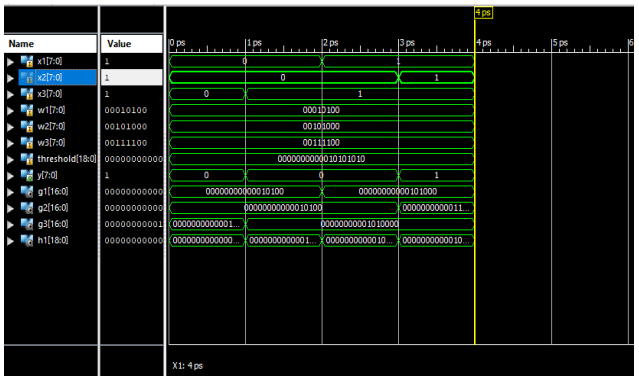

Fig. 8. Simulation result of Vedic Neuron

To design proposed ALU, all arithmetic functions and logical functions given in table 1 have been implemented. Simulation results of eight bit adder and eight bit subtractor are shown in Fig. 9 and Fig. 10 respectively. Eight bit logical gates, AND, OR, NOT and XOR gates are simulated. Simulation results of eight bit AND gate and XOR gate are shown in Fig.11 and Fig. 12 respectively. Using all designed arithmetic and logical functions given in Table1, ALU has been implemented. Fig.13 shows the simulation results of the proposed ALU.

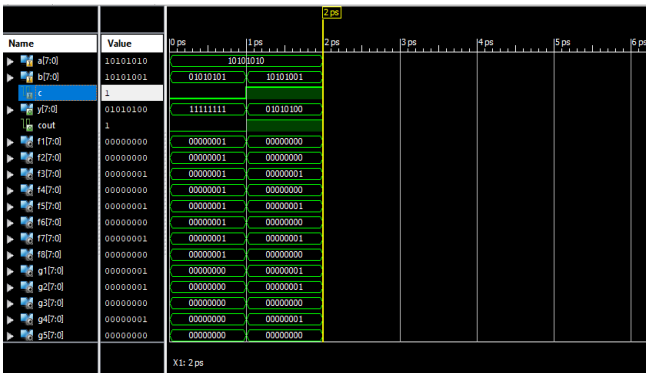

Fig 9. Simulation results of 8-bit Adder

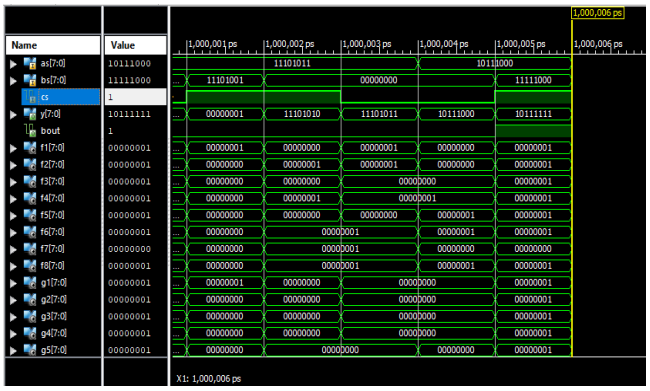

Fig 10. Simulation results of 8-bit Subtractor

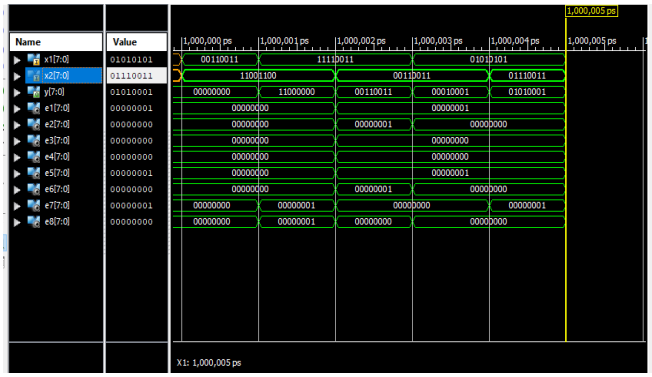

Fig 11. Simulation results of 8-bit AND Gate

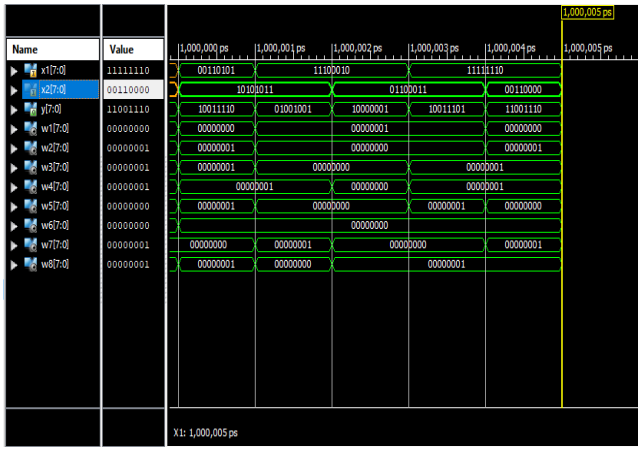

Fig 12.Simulation results of 8-bit XOR Gate

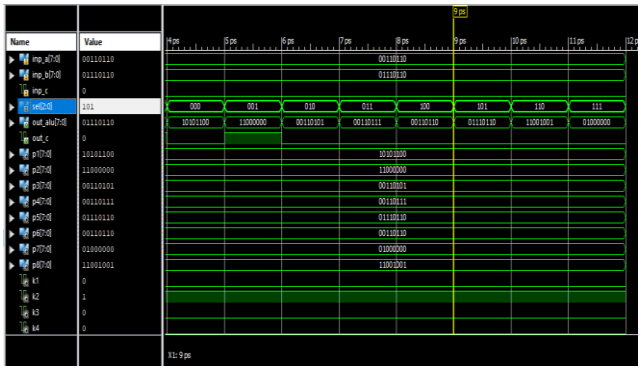

Fig. 13. Simulation results of Vedic ALU

The performance of proposed circuits are compared with existing conventional circuits. New Eight bit ALU using Vedic neuron exhibits 140.29 ns delay, while conventional eight bit ALU gives 170.93 ns delay. It has been observed that proposed designs of all logical and arithmetic circuits exhibit better processing speed. Summarized results are shown in Table I.

Device utilization summary for eight bit ALU using Vedic neurons and conventional ALU are shown in Table II. Compared with conventional ALU, proposed design is more efficient as it is having less area utilisation.

TABLE I. DELAY COMPARISON

S.No	*COMPONENT*	*VEDIC*	*CONVENTIONAL*
1.	ALU (8-BIT)	140.29ns	170.934ns
2.	ADDER (1-BIT)	22.8ns	23.1ns
3.	SUBTRACTOR (1-BIT)	45.3ns	48.5ns
4.	ADDER (8-BIT)	36.720ns	36.8ns
5.	SUBTRACTOR (8-BIT)	81ns	85ns
6.	INCREMENTER (8-BIT)	36.43ns	36.77ns
7.	DECREMENTE R (8-BIT)	80.09ns	84.2ns
8.	AND (1-BIT)	11.909ns	14ns
9.	OR (1-BIT)	12.14ns	14.2ns
10.	NOT (1-BIT)	11.89ns	13.98ns
11.	XOR(1-BIT)	17.67ns	20.5ns
12.	AND (8-BIT)	34.5ns	37.8ns
13.	OR (8-BIT)	34.23ns	35.98ns
14.	NOT (8-BIT)	12.2ns	13.9ns
15.	XOR (8-BIT)	36.8ns	40.01ns

TABLE II DEVICE UTILIZATION SUMMARY FOR VEDIC LOGIC VS. CONVENTIONAL LOGIC OF EIGHT BIT ALU.

Logic Utilization	Vedic Logic Used	Conventional Logic Used
Number of Slice LUTs	10355	11625
Number of fully used LUT-FF pairs	0	0
Number of bonded IOBs	29	29
Number of BUFG/BUFGCTRLs	1	1

TABLE III. PERFORMANCE ANALYSIS

Vedic ALU	Percentage improvement in speed	Percentage improvement in area
8-bit	17.925%	10.92%

VIII. CONCLUSION

Design of ALU using vedic neuron has been implemented successfully. Synthesized results are given in Table I and Table 2. From the results shown in Table I and Table II, it can be seen that compared with conventional ALU, proposed design is more efficient as it is having better processing speed and less area utilization. Overall performance of the designed ALU with Vedic neuron has improved significantly compared with conventional ALU. Processing speed has improved by 17.925% and area utilization has decreased by 10.92% as shown in Table III. Moreover, added advantage of this design is that, artificial neuron can be further trained and used much more efficiently. This breakthrough ALU design with Vedic neurons can be further refined and used in numerous applications where reduction in size and increase in computational speed are of primary concern.

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AUTHORS PROFILE

Ms Saji M Antony is a research scholar pursuing PhD from Delhi Technological University (DTU), New Delhi. Her areas of research interest include Analog Electronics and Wireless Sensor Networks. She received her B Tech and M Tech Degrees in Electronics & Communication Engineering (ECE). She has also acquired an MSc Degree in Computer Science from Bhundelkhand University scuring First Rank. She joined as a lecturer in the Dept of ECE, BVCOE, New Delhi in 2005. She is presently engaged as an Assistant Professor in the same College.

Dr Indu S is a professor and head of the Department of ECE, Delhi Technological University, New Delhi. She has vast experience as a teacher and guide in research projects. She has published a book "Smart Camera Networks" and has authored a chapter of the book "Video Surveillance" published by INTECH, UK. She has published around 70 papers in national and international journals and conferences. She has completed three prestigious projects as Principal Investigator, sponsored by Naval Research Board and Department of Science and Technology, Govt of India.

Dr Rajeshwari Pandey is a professor and research associate at ECE Dept of DTU. She received her Ph.D. from Faculty of Technology, University of Delhi. She has served BITS Pilani, AERF Noida and Priyadarshini College of Computer Science, Noida in various capacities. Her research interests include analog integrated circuits and microelectronics. She is member of IEEE and IEEE WIE for 15 years and is a life member of ISTE and IETE professional societies.