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Energy Efficient D Flip-Flop using MTCMOS Technique with Static Body Biasing

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Abstract: ***The need of fast and energy efficient devices is growing day-by-day and so flip flops are coming into picture. For many digital devices, flip flops are the elementary unit for construction. They are termed as one bit memory element. This paper enumerates, anew circuit design of D flip flop which consists of two techniques, i.e., MTCMOS technique and body biasing technique. The 5 transistor TSPC D flip flop using MTCMOS technique already exists. The body biasing technique is used on the already present circuit with the aim of achieving a new energy efficient design for D flip flop. The simulations are done using the Cadence Virtuoso 180nm technique.***

Index Terms**: Body Biasing, D flip-flop, MTCMOS technique, TSPC logic.**

I. INTRODUCTION

Flip-flops are the basic unit for creation for the digital models. Each flip flop performs the storage of one bit. Flip flop is always clocked. Flip flop is either positive edge triggered or negative edge triggered which implies that the input affects the output when the clock is going low-to-high or high-to-low, respectively. Flip flops are called single edge triggered flip-flop when the data storage is done either on rising or on falling edge of the clock. Also, they are known as dual edge triggered when the data storage is done on both falling as well as rising edge of the clock.

There are different types of flip flop. These are SR flip flop, JK flip flop, D flip flop and T flip flop. D flip flop is used in many applications like processors and as element for storage purposes. D flip flop can be constructed by using universal gates. However, the main use of it is to include proper timing delay. The other names for this are 'Data flip flop' and 'Delay flip flop'. The symbol for this is given below. One data input and one control input is there in this as reflected in figure below.

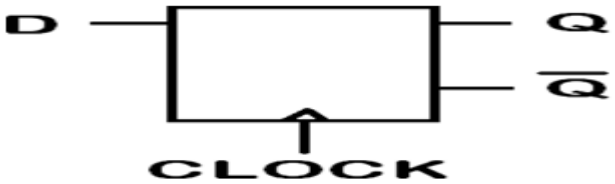

Figure 1: Symbol of D Flip Flop

In this paper, one new circuit of D flip flop is proposed, which is derived from the existing 5 transistor TSPC circuit.

II. LITERATURE REVIEW

Various designs has been suggested or presented for D flip flop. First of all, master slave configuration was implemented which uses the concept of cascading of two D latches in series which are constructed either by NAND gate, NOR gate, MUX, GDI, Transmission gate. In order to reduce the number of transistors, TSPC logic came into existence. D flip flop designs using 11T, 9T, 5T has been proposed. In order to further reduce the energy, some techniques can be applied on these circuits that already exist.

A. Existing Circuit

Multi-Threshold Voltage Complementary Metal Oxide Semiconductor reduce the standby current. This can be done by integrating elements having high threshold voltage with elements which has low threshold voltage. By sleep technique, efficient power management can be attained. The transistors are turned on during the duration when sleep signal is at lower level and inverted sleep signal is at higher level. This makes the circuit ON. On the other hand, sleep transistors are hindered during the duration when sleep signal is at higher level and inverted sleep signal is at lower level. This lands the circuit in idle mode. Hence, there is lowering or reduction in stand by current. In other words, there is cut-off of power rails, so that leakage power reduction can be attained in idle mode by inactivating of sleep transistors.

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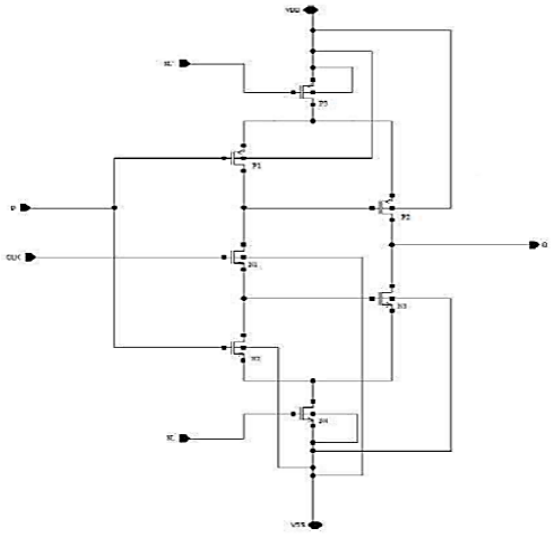

Figure 2: D flip flop based upon TSPC logic of 5 transistors with MTCMOS

The above figure shows the basic circuit of 5 transistor TSPC incorporating MTCMOS technique D flip flop. In this design, one PMOS at source node and one NMOS at ground node are used as sleep transistors. The SL and SL' are two signals provided to sleep transistor NMOS and PMOS respectively. Both have high threshold value. The working of this circuit is like that, the low threshold value main circuit experience null current flow when SL signal is at zero level of logic and SL' signal is at higher level of logic. On the contrary, the main circuit operates in normal mode when SL signal and SL' signal is at high and low level of logic

B. Proposed Circuit

A different technique called static body biasing has been applied on previous stated existing model. In this technique, the basic motto is to change the threshold value of the device. This can be achieved by changing the VSB, i.e., source-to-body voltage. The MOSFET threshold voltage is given by:

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{\left|2\Phi_F - V_{BS}\right|} - \sqrt{\left|2\Phi_F\right|}\right)$$

Where,

γ = body bias coefficient

VTH0 = threshold voltage when VSB is zero

2ΦF = outside potential at inversion

There are two types of body biasing: forward and reverse body biasing. Reverse body biasing occurs when higher value of gate voltage is required for inversion due to the negative potential supply to the body terminal which enhances the width. This increases the threshold voltage. On the other hand, forward body bias occurs when lower gate voltage is required due to supply of positive potential at body terminal which reduces the width. This results in lowering of threshold value

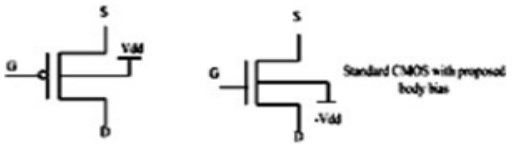

Figure 3: Implementation of Body Biasing Technique

III. SIMULATIONS

A. 5T TSPC MTCMOS D FLIP FLOP

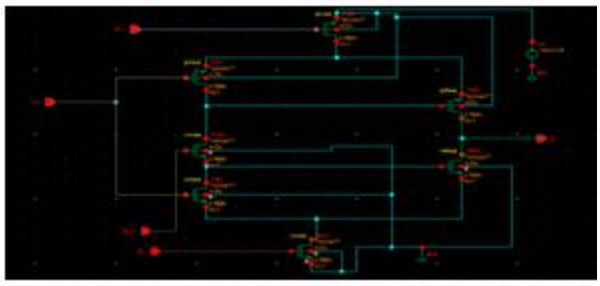

Figure 4: Schematic of 5TTSPC MTCMOS D Flip Flop

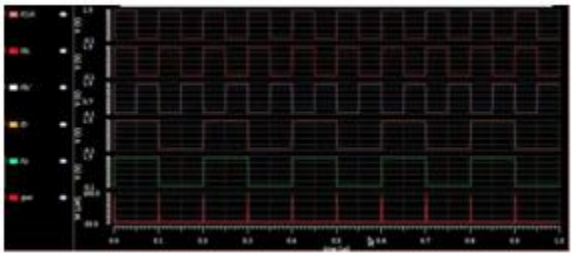

Figure 5: Waveform of 5T TSPC MTCMOS D Flip Flop

B. 5T TSPC MTCMOS STATIC BODY BIASING D FLIP FLOP

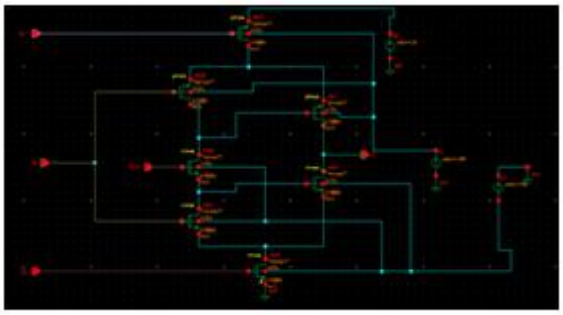

Figure 6: Schematic of 5T TSPC MTCMOS Static Body Biasing D Flip Flop

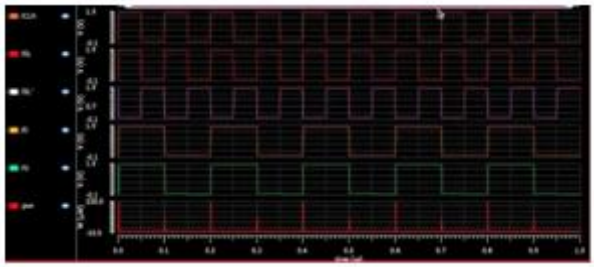

Figure 7: Waveform of 5T TSPC MTCMOS Static Body Biasing D Flip Flop

IV. SIMULATION RESULTS

S. No.	Technique Used in D Flip Flop	Average Power Consumption (Watts)	Delay in Circuits (Sec)	Power Delay Product (PDP)
1.	5T TSPC MTCMOS DFF	0.8127×10^{-6}	0.007383×10^{-9}	0.06×10^{-16}
2.	5T TSPC MTCMOS StaticBody Biasing DFF	0.4733×10^{-6}	0.2952×10^{-9}	1.397×10^{-16}

V. CONCLUSION

The new circuit for designing of D flip flop has been proposed using MTCMOS and body biasing technique on already existing 5 transistor TSPC MTCMOS circuit. The power consumption of new design is lesser than the previous circuit.

The demerit of this circuit is that due to increase in number of transistors, the delay increases. SO, an energy efficient design of D flip flop has been proposed which consumes less energy as compared to already existing ones

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Shivali is persuading her B.Tech in the discipline of Electronics & Communication Engineering for Indira Gandhi Delhi Technical University for women (IGDTUW). Her area of interest includes Digital Circuits & Systems and VLSI design.

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Amita Dev is the First Pro-Vice Chancellor of Indira Gandhi Delhi Technical University for Women. She has excellent track record of Administration quality Teaching, Innovation and Research. She has passion for Teaching and Research. She has published 63 + research papers in International and National Journals and Conference Proceedings. She has more than 33 years of experience in Industry, Teaching, Research and Administration. Her teaching and research areas include Artificial Neural Networks, Speech Processing, Opportunistic Networks, Speech Recognition Systems, MANETS, Advanced Computer Networks, Data Mining etc.