International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-8, Issue-1, May 2019

A 14-bit Dual-Split Capacitor Array DAC Design Based Successive Approximation ADC

Savitha.M R., Venkat Siva Reddy

Abstract: ***For the application of Internet-of-Things (IoTs),a low power, medium resolution ADCs are needed for converting the front end analog signal. In this research work presents, a Successive Approximation Register-Analog-to-Digital (SAR-ADC) design with minimum Capacitive Array Digital-to-Analog converter. Here, a novel Dual-Split-Three-Section (DSTS) capacitor array DAC (DSTS-CDAC) has been proposed to perform 14-bit SAR-ADC function while retaining Signal-to-Noise Destruction Ratio (SNDR) of 69.7dB for the ADC. The use of monotonic switching scheme exhibited reduced capacitive array power consumption for 14-bits CDAC. Furthermore, it requires 185 times unit capacitances on contrary to the conventional SAR-ADC designs, which requires 256 times unit capacitances in a capacitive array. A significant reduction of 28% area too applauds proposed design for low cost CMOS development. Also, in this paper, the linearity performances are theoretically analysed and behavioural simulations are performed. These values are comparable to the conventional method and found to be improved. This design uses 1.5V supply and 100kSps sampling frequency. Moreover, the design is made fully differential, thereby reducing the noise parameter to a considerable extent***

Keywords; Successive Approximation register, Digital to Analog Converter, SAR-ADC, DNL, INL, CDAC.

I. INTRODUCTION

Recently, the Internet-of-Things (IoTs) have grown significantly to meet major up-surging demands of social, scientific, businesses as well as defense purposes. To meet upcoming demands of IoT users, while enabling energy-efficient, sensibly-accurate and swift-processing systems, this research emphasizes on developing a novel Successive Approximation Register-Analog-to-Digital (SAR-ADC) design with minimum Capacitive Array Digital-to-Analog converter. SAR-ADC being an inevitable device for ultra-wideband and Wireless Sensor Networks (WSNs) which has been primarily used in IoT-ecosystem [1] requires optimal SAR-ADCs to assure accurate, fast, energy-efficient, performance. The ultra-low power consumption and fast computation are needed for sensor networks, communication systems, medical equipment's, industrial monitoring and control.

Revised Manuscript Received on 22 May 2019.
***** Correspondence Author
Savitha.M R*, Savitha.M Associate professor EC department KVGCE Sullia Dk
Venkat Siva Reddy, Venkat Siva Reddy M Associate professor School of E and C REVA university Bangalore

The classical SAR-ADC embodies a comparator, a SAR, a capacitive-array DAC (CDAC) and a sample and hold (S/R) circuit designed by the capacitive DAC itself [2]. In the classical ADC architecture, the sampled input voltage is successively approximated which is then followed by the estimation of the output digital bits by means of comparison steps. Undeniably, the sequential functions of the SA algorithm have classically been the limitation for accomplishing high-speed operation,

However, development in technologies lead emergence of the different ADC topologies to enable high-end processing, primarily high-end audio/video requirements [2][3]. Considering SA architectures as low power model identifying optimal design where the maximum power savings could be achieved is vital. Typically, the major power dissipation takes place in capacitive array of DAC structure which is one of component of SAR-ADC architecture. This as a result motivates authors to exploit optimal design of CDAC to achieve optimal function with minimum possible heating problem. Towards this capacitor CDAC design have been found efficient to achieve minimum power dissipation while retaining better linearity characteristics such as Differential Non-linearity (DNL) and Integral Non-linearity (INL) values in comparison to the classical binary-weighted capacitor DAC models... In this research paper, a novel Dual-Split-Three Segment Capacitor Array DAC Design Based Successive approximation ADC for IoT-Ecosystem has been developed. To assess linearity performance of the proposed SAR-ADC design both theoretical as well as simulation methods have been applied. Simulation results exhibited that the proposed DSTS-CDAC model can achieve better linearity with DNL of the range within ±0.5 LSB and standard deviation (capacitor) of merely 0.02%. The14-bit SAR-ADC model designed with DSTS DAC structure employed 1.5V supply and 100kSps sampling frequency, while the ADC retained SNDR of 68.9dB.

II. Dual-Split-Three-Segment CDAC Based SAR-ADC Design

As this research exploits efficacy of split capacitor array for DAC design and hence understating capacitor architecture in CDAC is vital. A snippet of the capacitor structure in DAC design is given as follows:

A. Capacitor Structures of CDAC:

The binary weighted DAC structure with binary weighted capacitive DAC can be used for the design successive approximation ADC. But total number of capacitors required and hence the area needed for capacitor array is used to be large particularly when the resolution of CDAC is high.

In such cases to accomplish relatively lower capacitors, the circuit can be modified from the traditional single split capacitive method to a well-defined and structured three segment capacitive method that eventually can reduce the total capacitance area. Here the capacitor array is split into two components in conjunction with three segments H, M and L that signify the resolution of the DAC. Noticeably, as indicated in Fig. 1, in our proposed model the CDAC comprises two split capacitances Ca_1 and Ca_2.

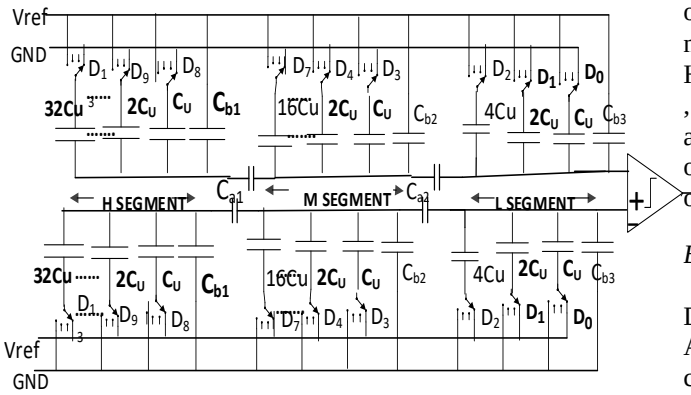


Fig. 1. Three segment CDAC Structure

Q_1 and Q_2 provide information pertaining to the smallest value of capacitors ratio in the adjacent segment. Mathematically,

$$\frac{C_{b3}}{C_u} = \frac{2^l - 1}{Q}\frac{Ca2}{Cu} - 2^l - 1 \quad (1)$$

$$\frac{C_{b2}}{C_u} = \frac{2^m - 1}{Q}\frac{Ca1}{Cu} - 2^l - 1 \quad (2)$$

Noticeably, in equation (1) C_{b3} and C_{b2} presents the extra grounded capacitance to be applied in circuit architecture, the variables l and m are the length of segments and C_u is the unit capacitance. To make clear the following formula, let C_{a1}/C_u=a; C_{d2}/C_u=b; C_{a2}/C_u=c; and C_{d3}/C_u=d,

$$c = 2^l, d = \frac{4^l}{Q_2} - (2^{l+1} + 1,) \; ; \quad x = 2^l - Q_2 \quad (3)$$

$$b = \frac{(2^m - Q_1)a}{Q1} - (2^m - 1)Q_2 \quad (4)$$

And the ratio of the total capacitance to the unit capacitance can be determined based on following factors and referring table I :

Table I: Capacitive distribution method for N-14 bit

H	M	L	a	b-x	c	d	Ct/Cu
7	4	3	2	8	8	49	217
7	5	2	2	18	3	28	205
6	5	3	2	24	8	49	185
There many others not listing							

For the resolution of 14 bit, the capacitors can be split in varied approaches. Some of the significant possible combinations of H, M, and L segments are depicted in Table II. Considering the resolution of 14 bits, let the capacitors in the segment be H=6, M=5 and L=3, the capacitor ratio be the unit value (i.e., Q1=Q2=1), a=2, (b-x) = c = 8 and d =49. Now, assigning these values, the total capacitance needed by our proposed Dual-Split-Three Segment (DSTS) CDAC method as 185 units C_u from capacitor distribution table. Here, it comprises two attenuation capacitances C_{a1} and C_{a2} , where C_{a1} = $2C_{u,}$ andC_{a2} = $8C_{u.}$ According to equation (1) and (2) the value of Cb_3= $49C_u$ and C_{b2}=$31C_u$. To augment our proposed CSDS-CDAC model for noise-resiliency the overall design is crafted as differential [4].

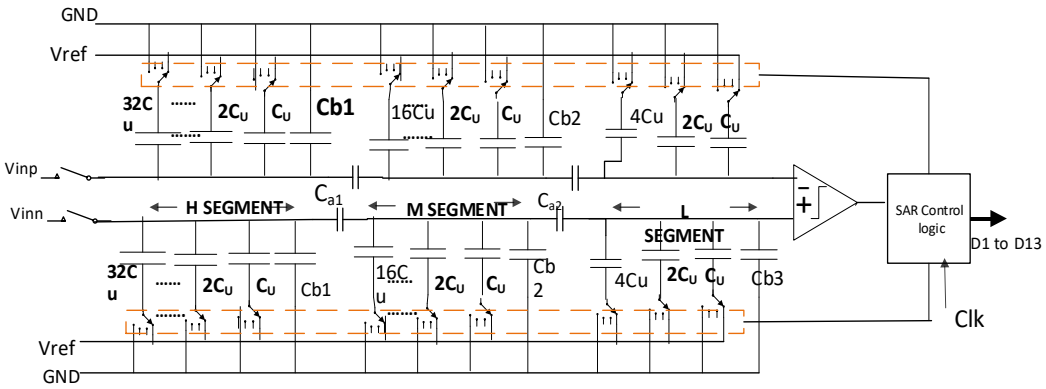
B. Switching Method:

Being a SA assisted ADC design, our proposed DSTS-CDAC structure employs the switching circuit for ADC using Successive Approximation Register (SAR) control logic, as depicted in Fig. 2, which follows the monotonic switching mechanism as discussed in [5-7]

The schematic of the proposed SA-ADC which consists of H- segment, M-segment and L- segment. Here H -segment is considered to be Main -array, M-segment and L- segment are together considered to be Sub- Array. Also, DAC_p (the capacitive array connected to the comparator's positive input) DAC_n (the capacitive array connected to the comparator's negative input) . The switching operation is as follows which is as depicted in Fig 3. In Sampling phase, the input signal is sampled to all top plate of capacitor and whereas the bottom plate of the array is connected to V_{ref}. During 1st cycle of conversion phase, sampling switches are made OFF. The comparator performs the comparison and MSB bit D_1 is determined. This cycle does not consume any switching energy. According to the comparator output, the largest capacitor on the higher voltage potential side is switched to ground and the other one (on the lower side) remains unchanged. The switching repeats the procedure until the LSB is decided.

Fig 3 shows the array energy consumption as function of the ADC output code for the proposed architecture, by following the monotonic switching algorithm. Through periodic sampling and conversion process. this method gives average Energy consumed as $126.03CVef^2$

In addition to the energy-efficiency the proposed DSTS CDAC design has been assessed for linearity analysis to ensure its suitability for IoT ecosystem.



DSTS-CDAC Switching Circuit

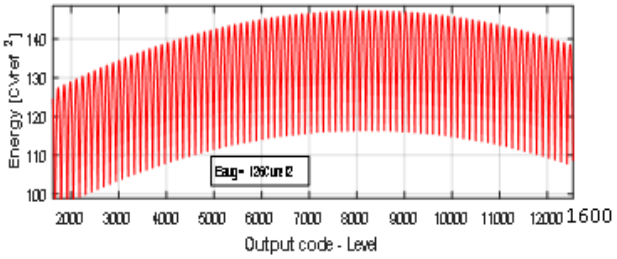


Fig 3. Switching Energy consumption curve

C. *Linearity analysis of capacitive DAC*

The linearity of the capacitive DAC predominantly depends on the matching properties of the capacitors and parasitic capacitances of the unit capacitive elements. Typically, the nonlinearity of CDAC is quantified in term of Integral Nonlinearity (INL) and Differential Nonlinearity (DNL). In this research work, the standard deviation of the DNL and INL has been estimated. Here, to characterize linearity characteristics (i.e., DNL and INL) of the developed DSTS-CDAC, the SAR-ADC was constructed based on capacitive-array DAC structures, where each capacitors in the capacitive array was modeled as the sum of the nominal value of the capacitances and an error term [5],[7][8]. For the binary weighted architecture, each capacitor is obtained as follows:

$$C_i = 2^{N-i}C_u + \delta_i \qquad (5)$$

$$\sigma_i^2 = E[\delta_i^2]$$

In (5), σ_i states the standard deviation of unit capacitance c_u and δ_i signifies the random variable with zero mean and variance of σ_i^2. The power consumption of CDAC structure is directly proportional to the value capacitor intern size of the unit capacitor in the capacitive array. The smallest possible value for is determined either by the kT/C noise requirement [9], the required matching properties of capacitor, parasitic capacitance or design rules of the technology. In general, the matching properties of the capacitors as well as the parasitic capacitances are the dominant factors for medium-resolution ADCs of the converter which affect the linearity characteristics. Therefore, in this paper a comparative assessment of the linearity of a SAR-ADC has been performed using the developed DACs structure due to capacitor mismatch and the standard deviation of the INL and DNL have been estimated. In this research work, the effect of capacitance mismatch has been quantified by its standard deviation for DNL (σ_{DNLMAX}) that actually takes place at the middle of input code. Referring the works in [8][9] for three segment CDAC structures the standard deviation for DNL can be estimated as function of relative standard deviation $\sigma(\frac{\Delta C}{C})$. Mathematically,

$$\sigma_{DNLMAX} = 2^{\frac{N}{3}}\,\sigma\left(\frac{\Delta C}{C}\right) \qquad (6)$$

In above expression (6), the relative value of $\sigma(\frac{\Delta C}{C})$ has been obtained using (7).

$$\sigma\left(\frac{\Delta C}{C}\right) = \sqrt{\frac{k_c^2 c_{spec}}{C_u} + s_c^2 x^2} \qquad (7)$$

In {7), c_{spec} refers the specific capacitance, C_u is the unit capacitance, K_c states pelgrom constant and S_c states the size independent coefficient. The value of capacitor is selected in such manner that there can be minimum value of $k_c^2 Cspec$, and the size of unit capacitance C_u. It is achieved by maintaining $\sigma_{DNLMAX} < 0.5$ by neglecting the size-independent term for medium resolution

D. *Capacitive Parasitic Effect*

In this paper, the parasitic effect of capacitances in CDAC structure has been assessed by considering capacitance effect of the top-plate of the designed array to the substrate, from the top-plate to the bottom-plate of all unit capacitor, and bottom plate to substrate of each capacitive bank of the DAC. Typically, the parasitic capacitances characterize the one connected from the top plate of the capacitor to the substrate (T-S), from the top plate to the bottom plate of the capacitor (T-B) and the bottom plate of the capacitor to the substrate (B-S). However, such type of parasitic capacitance would not affect linearity behavior of capacitive DAC significantly because the bottom-plate of the array capacitances is connected to the ground or supply-voltage. Usually, For the conventional CDAC the output voltage corresponding to a given digital input can be obtained by (8)].

$$Vout = \frac{\sum_{i=1}^{N} D_i . C_i}{C_{Tot} + C_{Par}} \qquad (8)$$

In equation (8), D_i presents the digital input word for $i = 1,2,3 \ldots N$, C_{Par} refers the parasitic capacitance connected at the top plate and $C_{Tot} = 2^N C_u$. For our proposed DSTS CDAC structures with three segments this expression has been obtained for 14 bit with H=6, M=5 and l=3 using (9).

$$Vout = \left[\frac{\sum_{i=1}^{\frac{N}{2}-1} D_i.C_i}{Ctot + C_{Par,H}} + AR.\frac{\sum_{i=\frac{N}{2}-1}^{i} D_i.C_i}{Ctot + C_{ParM} + C_{parL}}\right]V_{DD} \quad (9)$$

In equation (9), C_i states the capacitance associated with i^{th} bit, and AR states the attenuation ratio obtained using (10).

$$AR = \frac{C_u}{C_{H+C_{parH}}} \quad (10)$$

The above expression states that only the parasitic of $C_{ParM}$and C_{parL}influence the linearity which are responsible of a deterministic pattern of the DNL, and hence of the INL. In the proposed research, the transistor level simulation has been exhibited on 14-bit DSTS-CDAC with unit capacitance of $100fF$ and accordingly the linearity variations have been retrieved. This study has revealed that the pattern goes to high at every 128 for 14-bit resolution and the highest value of pattern is obtained at 0.4LSB which is within the range of +0.5LSB/-0.5LSB. Thus, in this study the value of ENOB is obtained as 11bits. In final state of the characterization, the parasitic between top- and bottom plate of the H –array capacitors has been assessed to have its impact on limiting the linearity performance of the proposed DSTS-CDAC structure. It is significant to assess this behavior as due to the routing paths for connecting the capacitor plates there could be certain parasitic capacitance impacting linearity of the proposed DSTS-CDAC structure. Usually, such parasitic capacitors affect the unit capacitance C_u that eventually affects major performance parameters including linearity as well as energy consumption. In the three-segment capacitive array model, the parasitic capacitance affecting C_i may impose an error of ΔC_ion the output voltage given in (11).

$$Vout = \left[\frac{\sum_{i=1}^{\frac{N}{2}-1} D_i.\Delta C_i}{C_{Par,H}} + AR.\frac{\sum_{i=\frac{N}{2}-1}^{i} D_i.\Delta C_i}{C_{ParM} + C_{parL}}\right]V_{DD} \quad (11)$$

In above equation $C_{Par,H}$, C_{ParM} and C_{parL} are the overall capacitances of the DAC structure. Considering this fact, in this research the effect of parasitic capacitances has been assessed, where it exhibits affirmative results ensuring optimal performance with minimum power exhaustion and better stability.

III. RESULTS AND DISCUSSIONS

Considering the significance of a robust DAC design for energy-efficient, SAR-ADC structure in this paper a highly robust Dual-Split-Three Segment Capacitive array DAC model (DSTS-CDAC) has been developed. In this type of capacitive DAC architecture enables two split with three segments that reduces energy exhaustion and overall capacitive area utilization. In the proposed three-segment capacitive DAC multiplexer has been applied as the selecting switch that eventually consumes low power (12µW). And comparator consumes the power of 10.47µW. The overall power consumption of successive approximation ADC was obtained as 90.12µW.. The power consumption of SAR-ADC has been assessed as a function of sampling rate, varying from 100-kSps to 1MSps and for the two different supply voltages (1V and 1.5v). The energy consumption by our proposed DSTS-CDAC model is depicted in Fig. 3. To perform simulation the sampling rate is selected as 1-MSps, the input supply of SAR - ADC was selected at 1.5V.

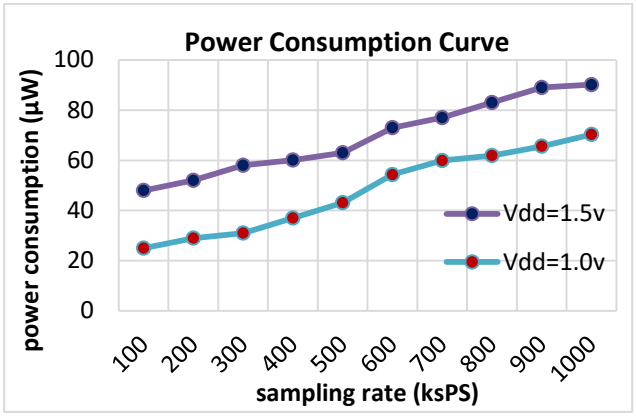


Fig 3. Power consumption curve

The static performance of the proposed SAR-ADC, which reports both DNL and INL in LSB as functions of the output level code of converter. Here the DNL shows periodic peaks at every 128 codes for 14-bit resolution. The measured value of the DNL at 1Msps is +0.4LSB/-0.2LSB and INL of 1LSB /-1LSB.These DNL/INL performance are mainly due to the mismatch value of capacitances present capacitive array. The standard deviation of DNL, INL versus output ode of converter as shown in the results (Fig. 4 and Fig. 5) where

Parameter	[10]	[12]	[13]	[14]	Proposed DSTS-CDAC
Power supply voltage(v)	1.8	1.5	1.2	1.2	1.5
Resolution (bit)	14	14	14	14	14
Sampling rate(MSps)	0.1	40	80	0072	1
Technology	-	65	130	130	180
Power Cons. by SAR_ADC(µw)	4.29	66000	3100	130	90.15
Peak ENOB(bits)	-	13.5	11.6	13.5	11.3
Peak SNDR(dB)	-	83	71.2	83	69.7
FOM (fJ/conversion step					357
Capacitors	-	-	MOM	MiM	PiP

the standard deviation goes to the maximum value of +0.45LSB As for as dynamic performance is concerned, at a sampling rate of 1MSps with power supply voltage of 1.5v the ADC achieves SNDR of 69.7dB and ENOB of 11.3 bits.The performance of the implemented SAR-ADC converter are summarized in Table II and compared with recent state-of-the art SAR -ADCs.

The proposed converter shows that, the parameters derived are in-line with the other medium-resolution converters Fig 6 shows the FFT Spectrum at sampling frequency 200KSps with input sinewave for a frequency of 96KHz.

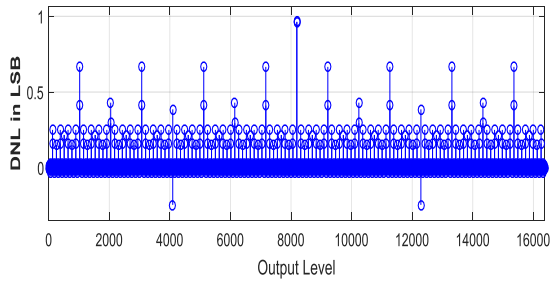


Fig 4. Simulated plot of DNL

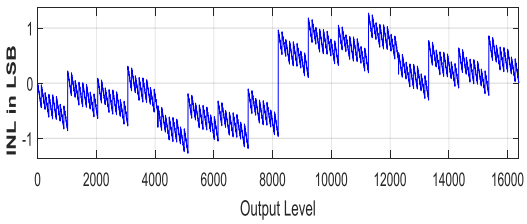


Fig 5. Simulated plot of INL

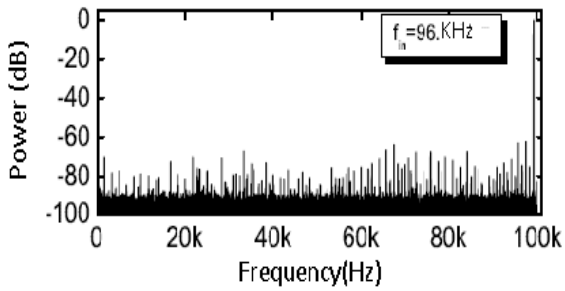


Fig 6: FFT Spectrum at 200Ksps Sampling frequency

Table II: Performance summary of SAR ADC

IV. CONCLUSION

Taking into consideration of the need of a robust data acquisition and communication system for the advanced communication purposes such as IoT ecosystem, in this paper a novel Dual-Split-Three-Section (DSTS) capacitor array DAC (DSTS-CDAC) was proposed to augment classical SAR-ADC design.The proposed DSTS-CDAC model focused on enabling 14-bit SAR-ADC function while retaining optimal Signal-to-Noise Destruction Ratio (SNDR) of the ADC, A graphic user interface MATLAB environment supports the implemented models that allow to simulate both mismatch and parasitic effects on linearity (DNL and INL). The energy consumption performance by the switching capacitors in applied CDAC model with three segment capacitive method revealed that the proposed DSTS-CDAC model exhibits 190 times reduced power consumption than the classical switching schemes. Unlike classical SAR-ADC design, DSTS-CDAC model that employs dual (i.e., two) split capacitor array with multiplex switching conserves more than 28% total capacitance area and hence makes proposed system memory efficient. Since the proposed design was made completely differential and hence reduced the noise parameter SNDR significantly. The proposed CDAC model can be of vital significance for noise-resilient sampling of high frequency differential input signals. However, the simulation results revealed that the proposed DSTS-CDAC model exhibits better stability or linearity under as compared to the classical DAC structures.

Acknowledgments:

The authors are very grateful to Principal and management of KVG college of Engineering Sullia for kindly support and for providing appropriate guidance.

REFERENCES

1. P. Madoglio et al., "13.6 A 2.4GHz WLAN digital polar transmitter with synthesized digital-to-time converter in 14nm trigate/Fin FET technology for IoT and wearable applications," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 226-227.
2. Wen-Cheng Lai, Ho-Chang Lee, Yen-Jung Su and Sheng-Lyang Jang, "SAR ADC with a body effect reduction T/H circuit for wireless power transfer applications," 2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia), Kaohsiung, 2017, pp. 638-642.
3. Y. Tsukamoto, K. Obata, K. Matsukawa and K. Sushihara, "High power efficient and scalable noise-shaping SAR ADC for IoT sensors," 2016 IEEE International Meeting for Future of Electron Devices, Kansai (IMFEDK), Kyoto, 2016, pp. 1-2
4. Inanlou, R., Yavari, M." A simple structure for noise-shaping SAR ADC in 90 nm CMOS technology "AEU - International Journal of Electronics and Communications Vol. 69, issue no.-8, August 2015, Pages 1085-1093
5. Zhangming Zhu, Zheng Qiu, Maliang Liu, and Ruixue Ding A 6-to10Bit 0.5V-to-0.9V Reconfigurable 2MS/s power scalable SAR ADC in 0.18μm CMOS, IEEE Trans. on Circuits and Systems I: Regular Papers, 2015, Vol.62, no.3, pp.689-696.
6. Liu, C., Chang, S., Huang, G., & Lin, Y). "A 10-bit 50-MS / s SAR ADC with a Monotonic, capacitor switching procedure" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 4, 731–740 APRIL 2010
7. Shubin Liu, Yi Shen, and Zhangming Zhu A 12-bit 10MS/s SAR ADC with High Linearity and Energy-Efficient Switching. IEEE Trans. on Circuits and Systems I: Regular Papers, 2016, vol.63, no.10, pp.1616-1627.
8. Saberi, M., Lotfi, R., Mafinezhad, K., Serdijn, W. A. "Analysis of Power Consumption and Linearity in Capacitive Digital-to-AnalogConverters Used in Successive Approximation ADCs, "IEEE Transactions on circuits and systems, vol. 58, no. 8, August 2011, 1736–1748.
9. Bonfanti, A. G., Milano, P., Milano, P., Brenna, S., & Bonfanti, A "A 6-fJ / conversion-step 200-kSps asynchronous SAR ADC with attenuation capacitor in 130-nm CMOS" Article in Analog Integrated Circuits and Signal Processing · August 2014.
10. Milano, P., Bonfanti, A. G., Milano, P., & Lacaita, A. L "A 70 .7-dB SNDR 100-kS / s 14-b SAR ADC with attenuation capacitance calibration in 0. 35-mu m CMOS," Analog Integrated Circuits and Signal Processing August, . 2016. 0–25
11. Zhang, D., Bhide, A., & Alvandpour, A. "A 53-nW 9.12-ENOB 1-kS/s SAR ADC in 0.13-_m CMOS for Medical Implant Devices", Proceedings of the ESSCIRC (ESSCIRC), IEEE 467–470, -2011.
12. R with 73.6dB SNDR in 65nm CMOS, IEEE Journal of Solid-State Cir. Kapusta, J. Shen, S. Decker, H. Li, E. Ibaragi, H. Zhu, A 14 b 80MS/s SAR ADC cuits, vol. 48, no. 2, pp. 3059–3059, Feb. 2013.
13. Fateh, S. S., Schönle, P., S., Bettini, L." A Reconfigurable 5-to-14-bit SAR ADC for Battery-Powered Medical Instrumentation," IEEE Transactions on circuits and systems—, VOL. 62, NO. 11, 2685–2694, NOVEMBER 2015.
14. Pieter Harpe, Eugenio Cantatore, Arthur van Roermund" An Oversampled 12/14b SAR ADC with Noise Reduction and Linearity Enhancements Achieving up to 79.1dB SNDR" IEEE International Solid-State Circuits Conference (ISSCC)-2014.