A Newly Designed Asymmetrical Multi-Cell Cascaded Multilevel Inverter for Distributed Renewable Energy Resources

K. Lakshmi Ganesh, N. Saida Naik, K. Narendra, G. Satya Narayana

Abstract*: *In micro grid system, the distributed renewable energy source (DRES) establishes the continuity of supply by using DC-AC inverter topology. Due to various disadvantages classical DC-AC inverter topology is unsuitable for grid connected DRES, in stage various multilevel inverter designs came into presence. The cascade H-bridge based multilevel inverter plays a significant role in many applications and applicable to medium-voltage by utilizing certain standard limitations. This peculiar design achieves high quality output voltage and current waveform as staircase waveform. The objective of this paper is to obtain higher output voltage level with less number of switches, less cost and lower THD values. It is carried out by asymmetric multi-cell CMLI topology. Hence this paper is introducing a proposed 85 level asymmetric multi-cell cascade multilevel inverter. It improves the fundamental component and also reduces the THD value by using less number of switches while comparing to other topologies of CMLI. In order to verify the proposed topology is integrated to micro-grid by using MATLAB/SIMULINK software and the results are conferred.

Index Terms*: *Cascaded H-Bridge Multi-level Inverter, Micro-Grid, Distributed Renewable Energy Sources, Multi-cell Cascaded H-Bridge Multi-level Inverter, Total Harmonic Distortion (THD).

I. INTRODUCTION

Now-a-days the global warming and climate changes are changed very effectively and focused on growth of eco-friendly power energy as Distributed Renewable Energy (DRES). For delivering standard electric power in terms of reliability, high efficiency and power quality, integrating interface converters plays a key role in DRES. In general, renewable energy sources are as photovoltaic, fuel cells, micro turbines and wind power are integrated into the micro grid system by using power-electronic conditioning systems [1-4]. In such systems, most of Distributed renewable energy sources usually supply a DC voltage that varies in a wide range according to a variety of load conditions. Thus, a DC-AC power processing interface is need and is compliable with commercial shopping malls, residential homes, industries and utility grid standards [5-7].

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Different type of converter topologies have been designed for distributed renewable energy resources [8-16] that exhibit efficient power flow control appearance whether in Stand-alone or grid-connected operation. Among those, various methodologies, the high-range transformers are used to enhance the performance in classical inverters. But, coming to multilevel inverter, it doesn't require any transformers which reduce the size, cost, weight of the over-all inverter module. To maintain international standards allow the use of grid-connected power converters without galvanic isolation, thus allowing called " transformerless" architectures for low rating medium power applications [7], [12].

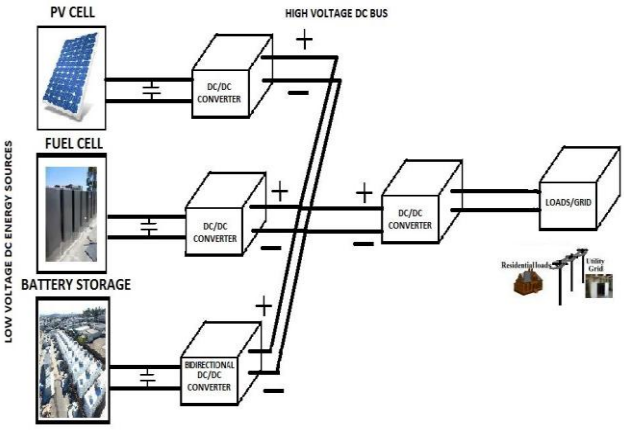


Fig.1 Configuration of Multi cell-CMLI for various DRES

The above Fig.1 shows DRES are connected to loads/grid through DC-DC converter and DC-AC Inverter. Inverter acts as interfacing device to load /grid which conversion energy coming from DRES from constant DC-link voltage into AC voltage. The inverter doesn't create a pure sinusoidal wave as an infinite number of odd harmonics due to square wave shape. The formal square wave inverters require high range filter units for attaining pure sinusoidal quantities. This drawback is resolved by multilevel inverters which produces staircase voltage wave shape which is equivalent to sinusoidal wave form by utilizing low-range filter units [17-18].

Multilevel Inverters (MLI) are very attractive for medium voltage and high power applications by using several low range switching elements.

The most widely recognized semiconductor switching devices are MOSFET, IGBT. These MLI topologies are classified based on structure, namely as Diode clamped MLI, Flying capacitor MLI and Cascaded H-bridge multilevel inverters (CHBMLI). Among these topologies, CHBMLI is the standard topology and best suited for generation of higher number of voltage levels without requirement of clamping diodes and balancing capacitors. The CHBMLI can be classified into two types are Symmetrical and Asymmetrical CHBMLI [19-20].

The symmetrical CHBMLI pre-requisites of equal input DC sources whereas Asymmetric CHBMLI pre-requisites of un-equal input DC sources. Over the symmetrical topology, the asymmetrical topology is highly used for higher number of voltage levels with highly qualified voltage levels. For extended voltage levels the proposed system plays a significant role in grid-connected systems and provides low harmonic distortions, less THD profile, requires low range filter, low common mode voltage, low dv/dt switch stress, high efficiency, etc. The proposed topology is designed as combined operation of Asymmetric Multi-cell modules as Cascaded form (AMC) which is used to generate 25 levels, 65 levels and 85 level output voltage. In this paper, the proposed Asymmetric multi-cell-CMLI topology is powered by co-generation based Solar PV system and Fuel-Cell driving by Fundamental Frequency Pulse-Width Modulation (FF-PWM) technique. The proposed AMC topology is more suitable for grid connected DRES system with enhanced power quality features. The proposed grid-integrated AMC topology is validated by using Matlab/Simulink tool and results are conferred with comparisons.

II. DISTRIBUTED RENEWABLE ENERGY SOURCES

Most of DRES includes solar PV, wind, fuel cell, rectified high frequency alternator outputs on micro turbines or flywheels and ultra-capacitors to bring into being DC Voltage. The above Fig.1 shows different types of DRES are there. In this paper, solar PV and Fuel cell system is designed as co-generation scheme for regulating sudden variations and maintain DC-link voltage as constant.

A. Photo-Voltaic System

A photovoltaic system consists of solar modules or panels achieving the pollution free energy named as clean & neat power producer [21]. The basic unit of a PV array is a PV cell. The modelling of PV system is generally considered as single diode model is depicted in the Fig.2. it consists of active current source, single diode, parallel formation of current source is represented as PV current, shunt and series resistances as Rs and Rsh. The current equation from solar PV cell is illustrated in Eqn. (1) as,

$$I_{pv} = I_{ph}N_p - I_sN_p\left[\exp\left(\frac{q\left(V_{pv} + I_{pv}R_s\frac{N_s}{N_p}\right)}{aV_tN_s}\right) - 1\right] - \left(\frac{q\left(V_{pv} + I_{pv}R_s\frac{N_s}{N_p}\right)}{R_P\frac{N_s}{N_p}}\right) \quad (1)$$

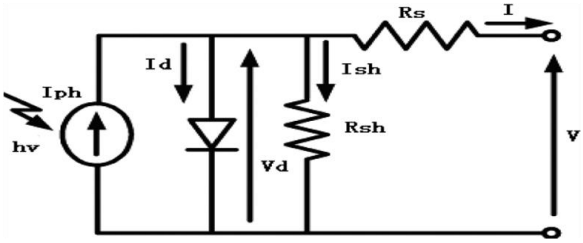


Fig.2 Single diode model of PV cell

Where
I_0 represents the reverse saturation current of diode
V_T represents the thermal voltage of diode
a represents the diode's ideality factor

The solar PV current equation is associated based on environment situations, then the irradiance & temperature is represented as

$$I_{ph} = \left[I_{sc} + K_1\left(T_c - T_{ref}\right)\right]S/1000 \quad (2)$$

Where
I_{PV_STC} represents the PV current at standard test systems
$\Delta T = T - T_{STC}$ (in Kelvin) and T_{STC}=25°C
G represents the irradiation level of surface
G_{STC} represents irradiation levels under standard test systems STS (as 1000W/m²)
K_I represents the coefficient factor of short-circuit current

The equation for the diode saturation current is specified as below,

$$I_s = I_{rs}(T_c/T_{ref})^3\exp\left[qE_g\left(\frac{1}{T_{ref}} - \frac{1}{T_c}\right)/KA\right] \quad (3)$$

Where
E_g represents the semi-conductor energy-gap energy gap
I_{0_STS} represents the current under nominal saturation limits

The reverse saturated current coefficient equation can be improved significantly as a function of temperature as follows,

$$I_0 = \frac{I_{sc} + K_I\Delta T}{\exp\left[(V_{oc} + K_V\Delta T)aV_T\right] - 1} \quad (4)$$

Where
K_V represents the coefficient of open-circuit voltage temperature
I_{SC_STC} represents the rated short-circuited current
V_{OC_STC} I represents the rated open-circuited voltage

The above-specified mathematical formations are used to represent the solar PV cell as single-diode model. These solar PV cells are interconnected as series and /or parallel formation based on PV generated power with respect to load demand. The series formation of PV cells increases the voltage ranges and parallel formation of PV cell maximizes the current ranges of solar PV system.

B. Fuel Cell

Several researchers have tried based on mechanism & experiencing modules of fuel cells. Various modeling schemes has definite complexities with accordance of number of parametric values explored in [22]. The most regular experienced model is,

$$V = E_0 - R * I - mexp(nI) - h[\ln(I) + \ln\left(\frac{P_a}{P_{O_2}}\right) \quad (5)$$

Where E_0 is the thermodynamic potential of the cell, I is the working current, P_a and P_{O_2} are the working pressure of the stack and oxygen partial pressure on the catalyst layer; m, n, R and h are parameters by experience. The terms ln(i) h × and mexp(nI) are due to simulate the polarization voltage drop during a large current density. When we come to the chemical-mechanism model, the output voltage of a single cell can be defined by the following expression

$$V_{FC}=E_{Nernst}-V_{act}-V_{ohmic}-V_{con} \quad (6)$$

Where V_{FC} is the output voltage of a single cell; E_{Nernst} is the electrochemical thermodynamic potential of the cell and it represents its reversible voltage, which is an ideal output voltage; V_{act} is the voltage drop due to the activation of the anode and cathode, or we can call it as activation polarization loss; V_{con} is the voltage drop resulting from the concentration of reactants, which is the gas transportation loss, V_{ohmic} is the ohmic voltage drop, and also call it ohmic polarization loss.

III. TRADITIONAL MULTILEVEL INVERTER TOPOLOGY

Generally, series-connection of several H-bridge inverters are used to develop the cascade H-bridge MLI topology, followed by a DC-link voltage V_{dc}. It consists of 2(n-1) switches named as upper group switches S_{1a}, S_{2a}, S_{3a}, S_{4a}, and lower group switches are S_{5a}, S_{6a}, S_{7a}, S_{8a}, respectively. The CHB-MLI is highly suitable for high-power medium-voltage applications it doesn't require any additional clamping diodes and balancing capacitors, the traditional CHB-MLI topology is shown in Fig.3.

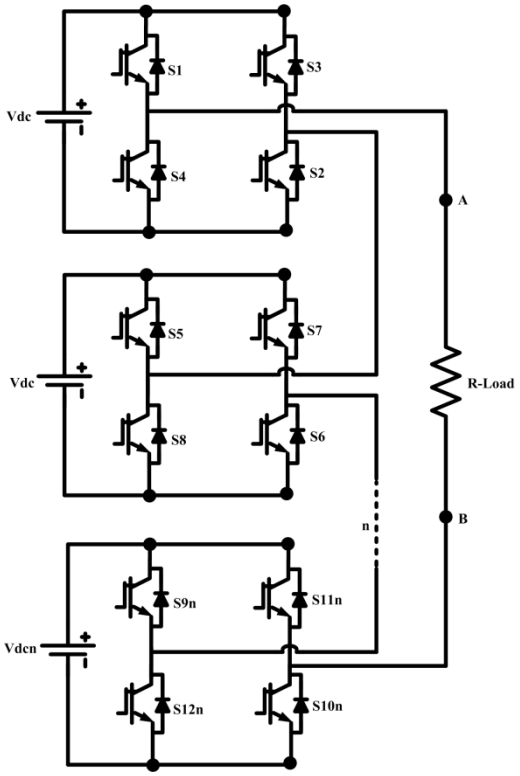


Fig.3 Traditional Cascaded H-Bridge MLI Topology

IV. PROPOSED ASYMMETRICAL MULTI-CELL CASCADED (AMC) TOPOLOGIES

In this proposed system, 25 levels Asymmetrical multi-cell Cascaded (AMC) topology is presented. In this topology, a high quality output voltage and current waveforms are achieved with less number of switches. The proposed AMC topology receives the good THD response, enhanced power quality features, pre-requisite of reduced filter units, etc. For generation of 25 output voltage levels, the AMC topology requires only 12 switches, 4 DC sources and reduced gate-drive circuits. For generation of same 25 output voltage levels, the traditional CHB-MLI topology requires 48 switches, 12 DC sources and more gate-drive circuits; therefore it is un-popular for higher number of voltage levels. In this multi-cell topology, multiple numbers of non-isolated DC voltage sources are given as input. The first terminal engaged with the first extremity of the first bridge and considered as the positive load terminal. The second extremity of first bridge is linked to first extremity of the second bridge circuit. Simply, it is designed as cascaded formation of several multi-cells for getting greater voltage levels with un-equal input DC sources. By utilizing reduced switch count, this topology maximizes the efficiency by decreasing the switching losses, low voltage rated switching devices can be used and leading to reduction in Electro Magnetic Interference and voltage stress (dv/dt) is reduced. Mainly this topology is used for low voltage high power applications. The block diagram representation of proposed 25 levels AMC topology driving the R-load as shown in Fig.4.

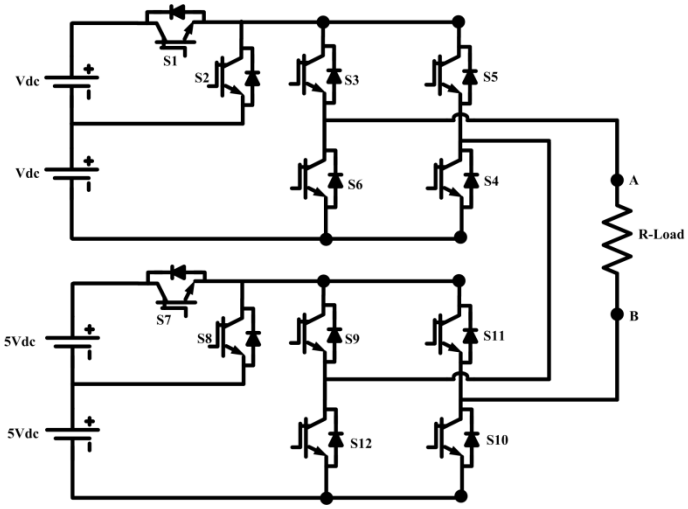


Fig. 4 Proposed 25 level asymmetric multi-cell CMLI

Table.1 Switching Table for Proposed 25-Level AMC Topology

Output Voltage Levels	Switching Sequences (Turn-ON)
0Vdc	S1, S3, S5, S7
Vdc	S1, S2, S5, S7, S10
2Vdc	S1, S2, S5, S7, S9
3Vdc	S3, S4, S5, S6, S9, S12
4Vdc	S3, S4, S5, S6, S10, S12
5Vdc	S1, S3, S5, S6, S12
6Vdc	S1, S2, S5, S6, S10, S12

7Vdc	S1, S2, S5, S6, S9, S12
8Vdc	S3, S4, S5, S6, S9, S11
9Vdc	S3, S4, S5, S6, S10, S11
10Vdc	S1, S3, S5, S6, S11
11Vdc	S1, S2, S5, S6, S10, S11
12Vdc	S1, S2, S5, S6, S9, S11
-Vdc	S3, S4, S5, S7, S10
-2Vdc	S3, S4, S5, S7, S9
-3Vdc	S1, S2, S7, S8, S9, S12
-4Vdc	S1, S2, S7, S8, S10, S12
-5Vdc	S1, S3, S8, S7, S12
-6Vdc	S3, S4, S7, S8, S10, S12
-7Vdc	S3, S4, S7, S8, S9, S12
-8Vdc	S1, S2, S7, S8, S9, S11
-9Vdc	S1, S2, S7, S8, S10, S11
-10Vdc	S1, S3, S7, S8, S11
-11Vdc	S3, S4, S7, S8, S10, S11
-12Vdc	S3, S4, S7, S8, S9, S11

The proposed 25-Level AMC topology consists of two modules and each module consists of two equivalent voltage sources. The upper module of AMC carries Vdc as input DC voltage whereas lower module carries 5Vdc as Input for generating 25 voltage levels in AC formation. The working model of 25 levels AMC topology is designed as, the first arm of the first bridge is considered as the positive load terminal. The second arm from the first bridge is connected to the first arm of the second bridge circuit. The second arm of the second bridge circuit is the negative load terminal shown the two modules as cascaded form for getting more voltage levels. Similarly, by adding several modules acquire more output voltage levels. The proposed 25-level AMC topology is driven by fundamental switching frequency based switching pulse generation by using switching sequences, represented in Table.1.

Generally, the proposed AMC topology is more significant for higher voltage levels with fewer switching devices and gate drive circuitry. By adding additional module to proposed modified AMC topology furnishes the 65-levels and 85-levels with equivalent switching elements. When number of levels are increased to pre-dominant levels which enhances the quality of output voltage and minimizes the harmonic content, improve the fundamental component with low THD profile. The block diagram representation of proposed modified AMC topology driving the R-load as shown in Fig.5.

For generation of 65-levels, the upper module of AMC carries Vdc as input DC voltage whereas middle and lower module carries 5Vdc and 10Vdc as input for generating of 65 voltage levels in AC formation. For generation of 85-levels, the upper module of modified AMC carries Vdc as input DC voltage whereas middle and lower module carries 5Vdc and 15Vdc as input for generating of 85 voltage levels in AC formation. The proposed 85-level modified AMC topology is driven by fundamental switching frequency based switching pulse generation by using switching sequences, represented in Table.2. The traditional CHB-MLI requires 168 switches and 42 DC sources for generation of 85-levels, but the proposed modified AMC 85-level topology requires only 18 switches and 6 DC sources. The harmonic distortions of output voltage are very less and common-mode voltage also very low when compared to traditional MLI topologies, which receives enhanced power quality features with good efficiency. Based on these above-mentioned merits, the proposed 85-level modified AMC topology is highly preferred in grid-integrated DRES systems. The critical evaluation of traditional and proposed AMC topologies are validated by using Matlab/Simulink tool and results are illustrated with several comparisons.

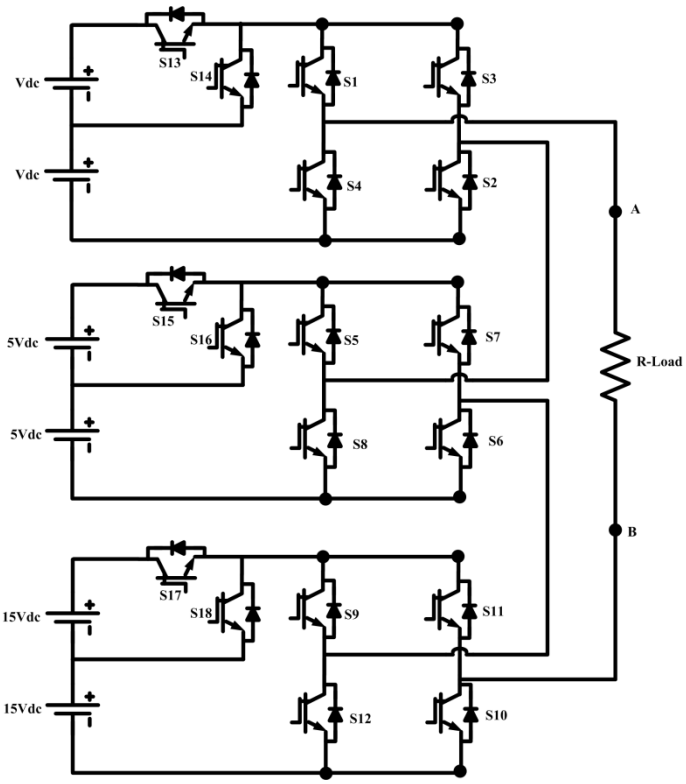


Fig. 5 proposed 85 level Asymmetric multi-cell CMLI

Table.2 Switching Table for Proposed 85-Level Modified AMC Topology

Output Voltage Levels	Switching Sequences (Turn-ON)
0Vdc	S1,S3,S5,S7,S9,S11
Vdc	S1,S2,S5,S7,S9,S11,S14
2Vdc	S1,S2,S5,S7,S9,S11,S13
3Vdc	S3,S4,S5,S6,S9,S10,S13,S16
4Vdc	S3,S4,S5,S6,S9,S11,S14,S16
5Vdc	S1,S3,S5,S6,S9,S11,S16

6Vdc	S1,S2,S5,S6,S9,S11,S14,S16
7Vdc	S1,S2,S4,S6,S9,S11,S13,S16
8Vdc	S3,S4,S5,S6,S9,S11,S13,S15
9Vdc	S3,S4,S5,S6,S9,S11,S14,S15
10Vdc	S1,S3,S5,S6,S9,S11,S15
11Vdc	S1,S2,S5,S6,S9,S11,S14,S15
12Vdc	S1,S2,S5,S6,S9,S11,S13,S15
13Vdc	S3,S4,S5,S7,S9,S10,S13,S18
14Vdc	S3,S4,S5,S7,S9,S10,S14,S18
15Vdc	S1,S3,S5,S7,S9,S10,S12,S18
16Vdc	S1,S2,S5,S7,S9,S10,S15,S18
17Vdc	S1,S2,S5,S7,S9,S10,S13,S18
18Vdc	S3,S4,S5,S6,S9,S10,S13,S16,S18
19Vdc	S3,S4,S5,S6,S9,S10,S14,S16,S18
20Vdc	S1,S3,S5,S6,S9,S10,S16,S18
21Vdc	S1,S2,S5,S6,S9,S10,S14,S16,S18
22Vdc	S1,S2,S5,S6,S9,S10,S13,S16,S18
23Vdc	S3,S4,S5,S6,S9,S10,S13,S15,S18
24Vdc	S3,S4,S5,S6,S9,S10,S14,S15,S18
25Vdc	S1,S3,S5,S6,S9,S10,S15,S18
26Vdc	S1,S2,S5,S6,S9,S10,S14,S15,S18
27Vdc	S1,S2,S5,S6,S9,S10,S12,S14,S18
28Vdc	S3,S4,S5,S7,S9,S10,S13,S17
29Vdc	S3,S4,S5,S7,S9,S10,S14,S17
30Vdc	S1,S3,S5,S7,S9,S10,S17
31Vdc	S1,S2,S5,S7,S9,S10,S14,S17
32Vdc	S1,S2,S5,S7,S9,S10,S13,S17
33Vdc	S3,S4,S5,S6,S9,S10,S13,S16,S17
34Vdc	S3,S4,S5,S6,S9,S10,S14,S16,S17
35Vdc	S1,S3,S5,S6,S9,S10,S16,S17
36Vdc	S1,S2,S5,S6,S9,S10,S14,S16,S17
37Vdc	S1,S2,S5,S6,S9,S10,S13,S15,S17
38Vdc	S3,S4,S5,S6,S9,S10,S13,S15,S17
39Vdc	S3,S4,S5,S6,S9,S10,S14,S15,S17
40Vdc	S1,S3,S5,S6,S9,S10,S15,S17
41Vdc	S1,S2,S5,S6,S9,S10,S14,S15,S17
42Vdc	S1,S2,S5,S6,S9,S10,S13,S15,S17

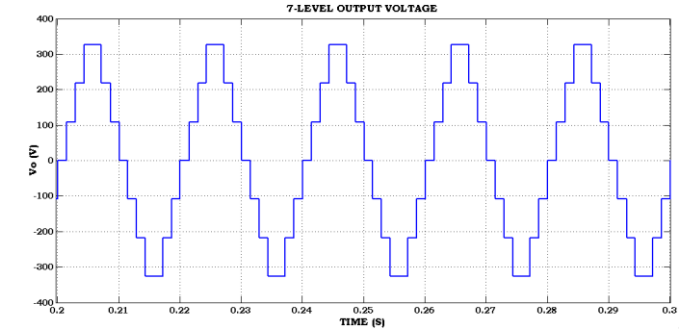
V. MATLAB/SIMULINK RESULTS

The Matlab/Simulink analysis is carried based on designing of various traditional and newly proposed AMC-MLI topologies by using fundamental frequency based modulation technique by using system specifications as shown in Table.3.

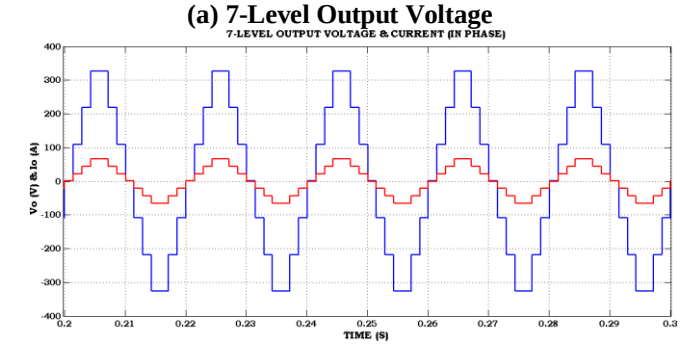
Table.3 Specifications

Parameters	Values
Input DC Voltage	V_{dc1}-7.76V, V_{dc2}-38.8V, V_{dc3}-116.4V
Grid Voltage	Vg-230V, 50 Hz
R-Load	R_L- 70Ω
LC Filtering Units	L-90mH, C-55µF
Fundamental Switching Frequency	Fs-50Hz

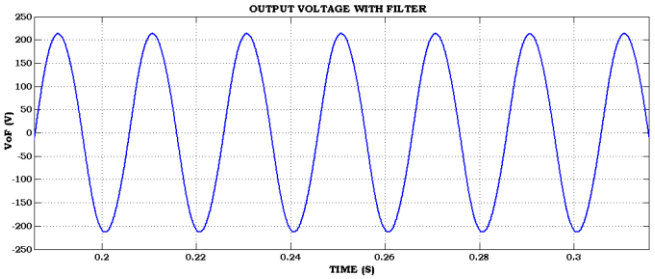
A. TRADITIONAL 7-LEVEL CHB-MLI TOPOLOGY



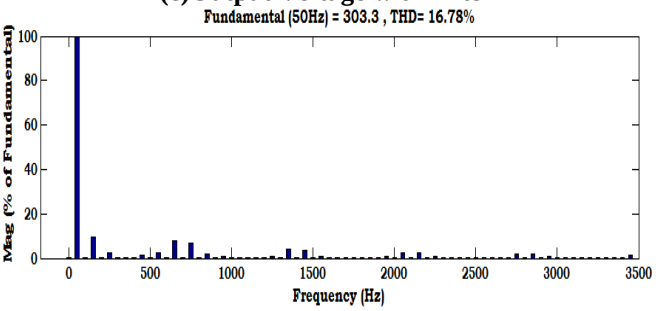
(a) 7-Level Output Voltage



(b)7-Level Output Voltage & Current In-Phase Condition



(c)Output Voltage with Filter

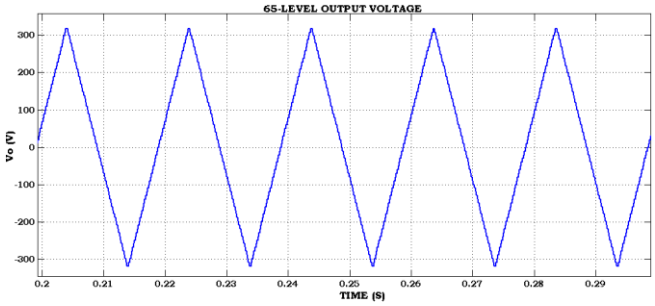


(d)THD Analysis of 7-Level Output Voltage

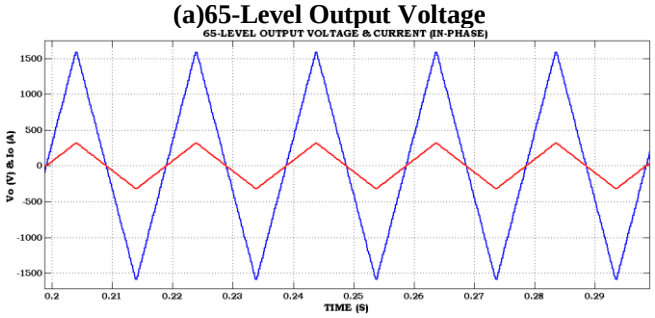
Fig.6 Simulation Results of Traditional 7-Level CHB –MLI Topology

Simulation results of Traditional 7-level CHB-MLI topology are depicted in Fig.6. In that, (a) 7-Level Output Voltage, (b)7-Level Output Voltage & Current In-Phase Condition, (c)Output Voltage with Filter, (d)THD Analysis of 7-Level Output Voltage, respectively. The output voltage has 7-staircase voltage levels which is near to sinusoidal by using low range filter units, the 7-level output voltage & current is in-phase condition which represents the unity power factor. The THD analysis of 7-level output voltage is16.78%, it is moderate than traditional topologies.

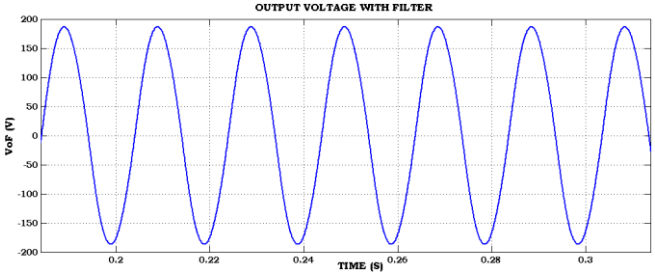
B. PROPOSED 65-LEVEL AMC-MLI TOPOLOGY



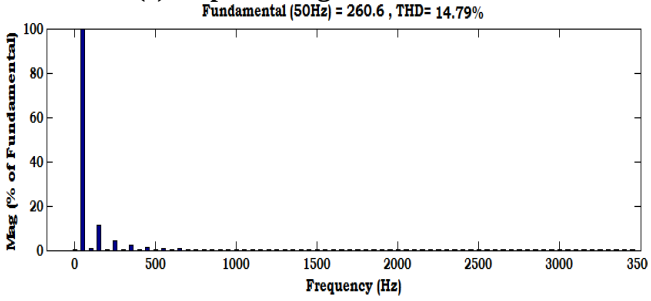
(a)65-Level Output Voltage



(b)65-Level Output Voltage & Current In-Phase Condition



(c)Output Voltage with Filter

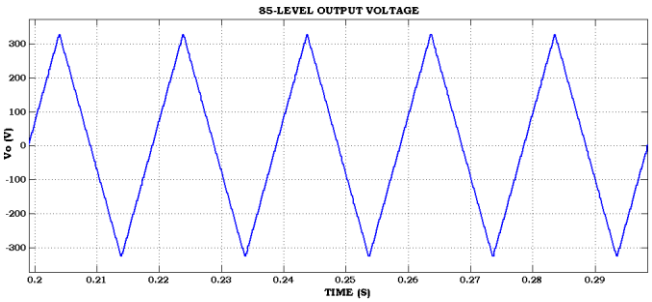


d)THD Analysis of 65-Level Output Voltage

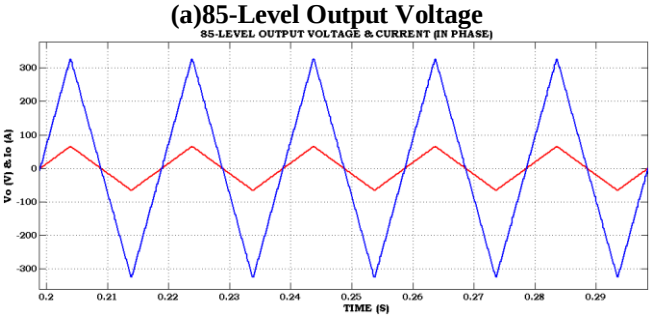
Fig.7 Simulation Results of Proposed 65-Level AMC –MLI Topology

Simulation results of proposed 65-level AMC-MLI topology are depicted in Fig.7. In that, (a) 65-Level Output Voltage, (b)65-Level Output Voltage & Current In-Phase Condition, (c)Output Voltage with Filter, (d)THD Analysis of 65-Level Output Voltage, respectively. The output voltage has 65-staircase voltage levels which is close to pure sinusoidal by using low range filter units, the 65-level output voltage & current is in-phase condition which represents the unity power factor. The THD analysis of 65-level output voltage is14.79%, it is lower than traditional topologies.

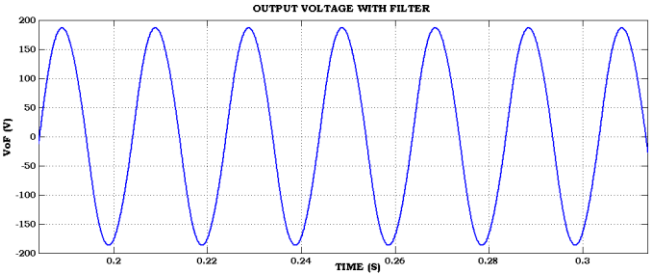
C. PROPOSED 85-LEVEL AMC-MLI TOPOLOGY



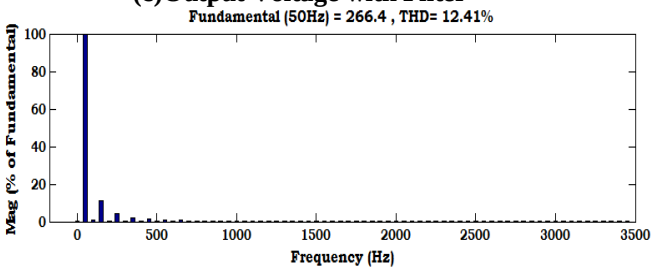
(a)85-Level Output Voltage



(b)85-Level Output Voltage & Current In-Phase Condition



(c)Output Voltage with Filter

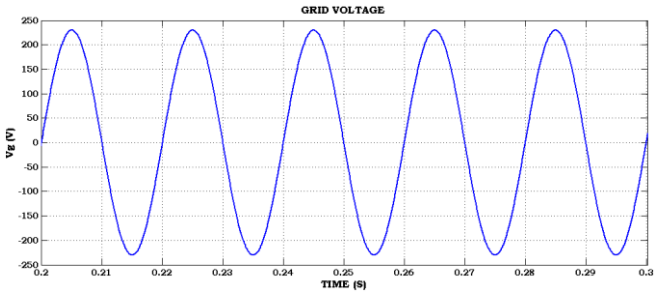


d)THD Analysis of 85-Level Output Voltage

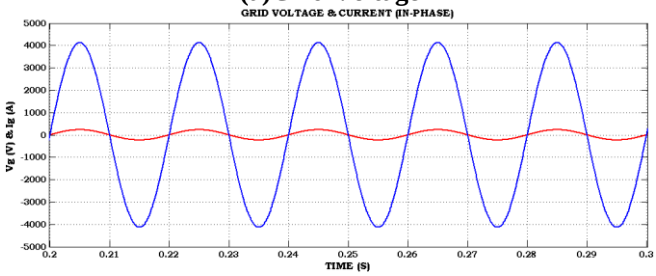
Fig.8 Simulation Results of Proposed 85-Level AMC –MLI Topology

Simulation results of proposed 85-level AMC-MLI topology are depicted in Fig.8. In that, (a) 85-Level Output Voltage, (b)85-Level Output Voltage & Current In-Phase Condition, (c)Output Voltage with Filter, (d)THD Analysis of 85-Level Output Voltage, respectively. The output voltage has 85-staircase voltage levels which is very near to pure sinusoidal by using very low range filter units, the 85-level output voltage & current is in-phase condition which represents the unity power factor. The THD analysis of 85-level output voltage is12.41%, it is very low compare to traditional and proposed 65-level AMC topologies.

D. PROPOSED 85-LEVEL AMC-MLI TOPOLOGY FED GRID CONNECTED SCHEME



(a)Grid Voltage



(b)Grid Voltage & Current-In Phase Condition

Fig.9 Simulation Results of Proposed 85-Level AMC-MLI Topology Fed Grid-Connected Scheme

The Simulation Results of Proposed 85-Level AMC-MLI Topology Fed Grid-Connected Scheme as depicted in Fig.9. In that, (a) Grid Voltage, (b) Grid Voltage & Current-In Phase condition. The grid-voltages and current is maintained as sinusoidal quantities with an fundamental operating frequency and in-phase condition to maintain grid-power factor as unity.

Table.3. Comparison of Switch/DC Source Requirements in Traditional MLI Topologies

Number of Levels	Required Number of Switches	Number of DC Sources
7 Level	12	3
25 Level	48	12
65 Level	128	32
85 Level	168	42

Table.4 Comparison of Switch/DC Source Requirements in Proposed AMC Topology

Number of levels	Required number of switches	Number of DC sources
25 Level	12	4
65 Level	18	6
85 Level	18	6

Table.5. THD Comparison of Conventional And Proposed System

Type of system	Required number of switches	Fundamental voltage In volts	THD (%)
Traditional system	7 LEVEL	240	16.78
Proposed system	65 LEVEL	260.5	14.79
	85 LEVEL	266.4	12.41

In this paper traditional CHB configuration of 7, 25, 65, 85 levels produce by using number of switches and number of DC sources is represented in the table.3. For higher number of voltage levels, the requirement of switches is very high in symmetrical topologies. That's why most researchers are used Asymmetrical topologies, the proposed AMC topologies requires reduced number of switching elements/DC sources over the traditional MLI topologies for same number of voltage levels as represented in Table.4. The acquired fundamental voltage is 266.4Volts and THD is 12.41% by proposed 85level AMC-MLI which is best one compared to other topologies as represented in table.5.

VI. CONCLUSION

Finally, work is conceded out on traditional system of 7 level, proposed system of 65 level and 85 level AMC topologies are driving by fundamental frequency based PWM technique were presented. The THD value attained by traditional system 16.78% and by the proposed system of 65 level obtained THD value is 14.79% and also proposed system of 85 level obtained THD value is 12.41%. The proposed AMC topology requires low switching elements, low cost, low space requirement, low dv/dt stress, high efficiency, etc. The proposed AMC topology is best suited for distributed renewable energy sources such as PV cell and Fuel cell as co-generation scheme for grid-connected system.

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