Experimental Investigation of Dual Terminal Inverter Topology

C. Janani, C. Kalaivani, K. Rajambal

Abstract*: Dual terminal inverters are employed to control two three-phase AC loads. Earlier separate inverters are applied for this operation which increases the size, cost of the overall system. This paper suggests a dual terminal inverter with fewer switches called novel Six-Switch Dual Terminal Inverter (SSDTI) to surmount this impediment. In this investigation, Diode-assisted SSDTI topology is explored. The simulation model of the SSDTI was accomplished using MATLAB/SIMULINK. This study examines the performance for variation in modulation indices. The Experimental verification of the proposed Diode-assisted SSDTI is carried out and behavior of the suggested step-up inverter is tested and validated.

***Index Terms*: CUK Converter, Dual Terminal Inverter, Diode-Assisted Inverter, SEPIC Converter.**

I. INTRODUCTION

The utilization of independently supplying the number of AC loads need separate inverters for each in many applications like induction motor drives and systems. This leads to an inimical rise in system cost, volume and weight. A special inverter with reduced switches helps to surmount these drawbacks. These aspirations are accomplished by lessening the active switches in inverters. The reduced switch count inverter comprises six active switches, divided as three active switches in every leg, the intermediate switches are split for both of them and two separate 3- phase loads are attached to the joints between the switches and the capacitor legs. This inverter is greatly suggested as optimal inverter topology with dual-outputs to deliver and control the dual individual 3- phase loads.

The attractive dual-leg system can be recognized as two individual full bridge inverter topologies. Another technique is develop a six switch inverter is replaced three switches in a leg as cascade combination of capacitors, the conserve cost of the inverter significantly by lessening the significant switches in the scheme. The capacitors are employed to split the voltage between the switches. The single-leg inverter topology, utilizes the three-active switches for driving the two individual single-phase loads, it is analogous to two semi-controlled inverters with a common DC-link capacitor and switch. The articles [1–5] recommend the different reduced switch count topologies. The reported literatures classify the fewer switching elements into two wide modules as multiple and single output inverter topologies. The utilization of this inverter in renewable energy applications requires a buck-boost converter for filtering the un-necessary elements in a AC output voltage for attaining desired values.

The SEPIC and CUK type DC-DC converters are acts as front-end conversion for 3-phase inverter which yields the non-isolated buck-boost bi-directional inverter topology [3]. Renewable energy systems and motor drive application employs the single inverter topology with pre-requisite of six active switches in a power circuit integrated as three-phase manner [4]. The other non-isolated type buck-boost inverter topology plays a significant role which consisted of X-shaped structure design based on impedance for safe-guarding the system from faults, but which predominantly increases the extra passive devices, greater size, high system cost, etc [5]. In [6] proposes the novel X-shaped structured diode-clamped topology which is integrated in between DC source and inverter which boosts the input voltage and attains high voltage gain over the SEPIC & CUK buck-boost converters. This analysis suggests the proposed inverter structure supplying the three-phase AC loads independently with less switches over the classical 9-switch topology [7]. Specific structures of dual integrated inverter structures are SEPIC-SSDTI, CUK-SSDTI and Diode-Assisted SSDTI. The attractive study builds up a unique gate triggering technique utilizing a sinusoidal PWM scheme [8],[9]. The structures of SSDTI demands modifications in a common DC-link capacitors for providing stabilized output. The reduced or fewer switch count type inverter leads to minimizing the components in hardware prototype model such as protection circuitry, gate-pulse generators, cooling scheme, these are highly impact on cost and size of over-all system. In this paper, the simulation model of diode-assisted six switch dual terminal inverter is developed in Matlab/Simulink. Pulses to the inverter are derived by Sinusoidal pulse width modulation technique. The developed simulation model explores the performance of the inverter for varying modulation indices. The experimental model of diode-assisted SSDTI is designed. The pulse to the switches is given using Arduino/UNO. The simulation results are validated using the experimental results.

II. PROPOSED SSDTI

A. SSDTI Structure

This section enumerates the switch arrangement in different configuration and developed carrier-based PWM scheme for the suggested topology. The Fig.1 presents the proposed six switch dual terminal three-phase inverter supplying two 3-phase loads. The inverter comprises two legs each contributing three power switches in each leg. Moreover, at the DC link three sources are placed in series.

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Two phases of 3-phase loads each are connected to two inverter legs and the other phase is connected to one of the joints of the DC link sources.

The middle switches splits between the two AC loads. The number of switches count is reduced by 33% and 40% compared to nine-switch inverter and five-leg inverter. The voltage levels of DC link sources are expressed as a function of three a, b, and c coefficients. These coefficients are to be determined to accomplish stabilized 3-phase outputs voltages without the dc component.

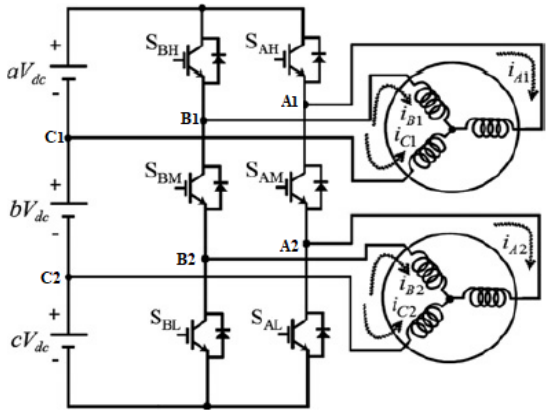

Fig.1 Structure of SSDTI

B. Carrier Based PWM Scheme

Fig.1 shows the system of the six switch dual terminal inverter supplying two AC loads. It comprises six switches, each leg having three switches. To control two AC loads independently, this paper suggests a new PWM switching scheme [10]. This method employs two reference signals for the upper and lower outputs. The lower modulating signal (V_{refL}) is always smaller than the upper modulating signal (V_{refU}) so as to determine the offset values which helps in reducing interference of the signals. The carrier signal is compared with the upper modulating signals to obtain the switching pulse of S_{ah} and S_{bh}. Similarly, the lower modulating signals are compared with carrier to get the switching pulse of S_{al} and S_{bl}. The lower and upper gate signals in each leg are logically XORed to obtain te pulse for the middle switched S_{am} and S_{bm}. This switching pattern allows only two switches ON in each leg. Assuming upper and lower output modulating signals to be sinusoidal waves.

$$V_{refU1} = m_1 \sin \omega_u t + offset_u \quad (1)$$

$$V_{refU2} = m_1 \sin(\omega_u t - \phi_1) + offset_u \quad (2)$$

$$V_{refL1} = m_2 \sin \omega_l t + offset_l \quad (3)$$

$$V_{refL2} = m_2 \sin(\omega_l t - \phi_2) + offset_l \quad (4)$$

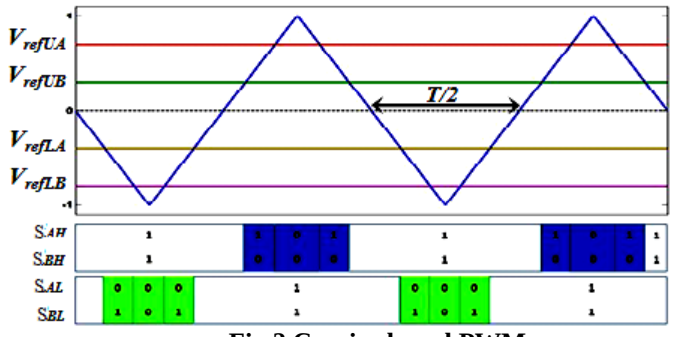

Fig.2 Carrier based PWM

where m_x and φ_x ($x=u,l$) represents the reference and phase difference. ω_x and $offset_x$ denotes the angular frequency and the offset of the modulating signals.

The carrier-based PWM scheme of the inverter and the resultant switching vectors are represented in Fig.2. There are two reference signals in each phase, The offset values are defined as of CUK-SSDTI.is defined as,

$$0 \le offset_u \le 1 \quad (5)$$

$$-1 \le offset_l \le 0 \quad (6)$$

$$offset_u = m_2 \quad (7)$$

$$offset_l = -m_1 \quad (8)$$

There is an added reference signal V_h and V_l besides the reference signals, which controls the duty ratio of the switch. The carrier is compared with V_h and V_l to obtain gate signal to switch SW. the modulation indices satisfying equation (9) is employed to avoid interference of the modulating signals,

$$(mu\_max+ml\_max) \le |V_h| + |V_l| \quad (9)$$

$|V_h| = |V_l| = D$, During switch SW is OFF, the time interval is balanced cutting down the calculation of boost voltage gain and peak AC output voltage. The inductor L charges through SW and the capacitors V_{C1} while SW is ON The capacitor voltages V_{C2}, V_{C3}, V_{C4} create the upper, middle and lower voltage sources respectively.

$$V_L = V_{DC} \quad (10)$$

The lower modulating signal (V_{ref2}) should be less than the upper one (V_{ref1}) at any time. To impede interference between modulating signals the offset value for each reference waveform are determined. The upper modulating signal and the carrier signal are compared to get gate signals of S_{AH} and S_{BH}. Gate signals of SAL and S_{BL} switches are realized by comparing the lower modulating signal with the carrier signal. The logical XOR of the upper and lower gate signals in each leg deduce the gate signals of S_{AM} and S_{BM} . Implementing this method, there are invariably two switches ON in each leg. Accounting the fact that a + b + c = 1, it can be deduced that to obtain balanced output voltages ω_1 should be $\pi/3$ and second that phase voltages of both inverter outputs contain DC component. The values of a, b and c are independently determined in VF and CF modes to eliminate DC component from inverter output voltages which employs two distinct approaches for each operation analysed in the subsequent sections. The equation expressed by (11) to (13) represents the upper output voltage assuming DC component is eliminated

$$v_{A1} = \frac{\sqrt{3}}{6} m_1 V_{dc} \sin\left(\omega_1 t + \frac{\pi}{6}\right) \quad (11)$$

$$v_{B1} = \frac{\sqrt{3}}{6} m_1 V_{dc} \sin\left(\omega_1 t - \frac{\pi}{2}\right) \quad (12)$$

$$v_{C1} = \frac{\sqrt{3}}{6} m_1 V_{dc} \sin\left(\omega_1 t + \frac{5\pi}{6}\right) \quad (13)$$

Similarly, ω_2 is assumed to be equal to $\pi/3$ and DC component being eliminated, the lower output voltage fundamental values of the inverter would be

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$$v_{A2} = \frac{\sqrt{3}}{6} m_2 V_{dc} \sin\left(\omega_2 t + \frac{\pi}{6}\right) \quad (14)$$

$$v_{B2} = \frac{\sqrt{3}}{6} m_2 V_{dc} \left(\sin \omega_2 t - \frac{\pi}{2}\right) \quad (15)$$

$$v_{C2} = \frac{\sqrt{3}}{6} m_2 V_{dc} \sin\left(\omega_2 t + \frac{5\pi}{6}\right) \quad (16)$$

III. BOOST DERIVED INVERTER TOPOLOGIES

A. Cuk derived SSDTI

The Fig.3 represents the CUK derived SSDTI where CUK converter in front stage the inverter using an extra capacitor, inductor and switches compared to SSDTI. The required boost voltage gain is achieved by the proper control of the switches SW, S_{ax}, S_{bx}, (x=h, l, m) [11].

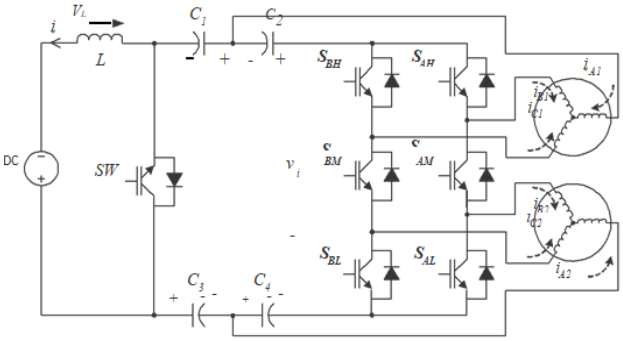


Fig.3 Cuk derived SSDTI

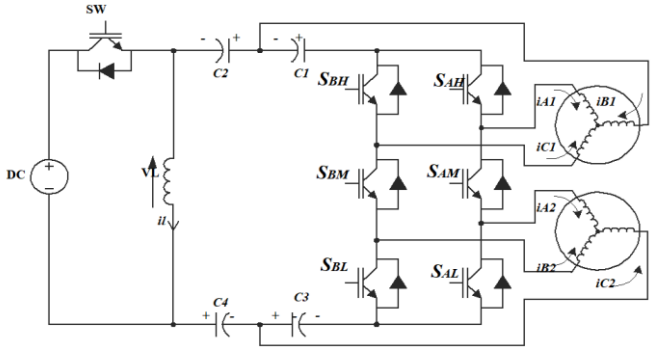


Fig.4 Sepic derived SSDTI

B. Sepic derived SSDTI

The SEPIC and CUK converter are similar in terms of switches and passive elements but with the interchanged inductor and switch SW. this converter has the same output and input polarity. The Fig.4 shows the SEPIC converter circuit with drawback of pulsating input current running from a battery supply. The Table-I is used for determining the peak AC output voltages like CUK-SSDTI. The equation [13] is employed for deducing the value of D.

C. *3.3 Diode- Assisted SSDTI*

The Diode-Assisted SSDTI shown in Fig.5 comprises an X shaped Diode capacitor and an SSDTI. When compared to CUK and SEPIC-SSDTI, the Diode-Assisted SSDTI has additional diodes. The modeling equations used for simulation is referred from [13]

Table 1: Relation of boost derived SSDTI

Parameter	CUK – SSDTI	SEPIC-SSDTI	Diode-Assisted SSDTI
V_{ctotal}	$\frac{V_{DC}}{1-D}$	$\frac{DV_{DC}}{1-D}$	$\frac{2V_{DC}}{1-D}$
$v_{in}\|_{SW\text{-}ON} = V_{in}$	$\frac{V_{DC}}{1-D}$	$\frac{V_{DC}}{1-D}$	$\frac{2V_{DC}}{1-D}$
B	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{2}{1-D}$
$\hat{V}_{AC-x}$	$\frac{\sqrt{3}}{6}\frac{m_x V_{DC}}{1-D}$	$\frac{\sqrt{3}}{6}\frac{m_x V_{DC}}{1-D}$	$\frac{\sqrt{3}}{6}\frac{m_x V_{DC}}{1-D}$

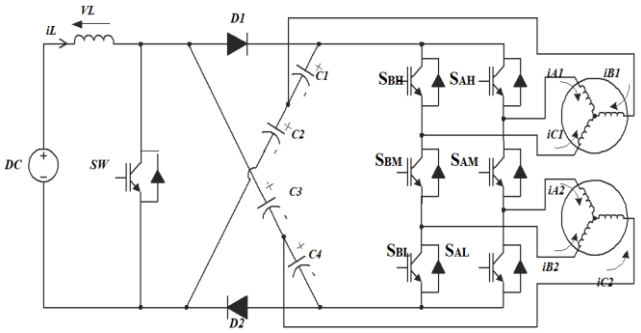


Fig.5 Diode-assisted SSDTI

IV. SIMULATION RESULTS

In this section, the behavior of SSDTI using the simulation results is verified by using simulation parameters presented in Table II. The dual output of the inverter feeds two RL loads. The DC input voltage is chosen so as to maintain same amplitude of output current in the three boost derived inverter topologies. The CUK- SSDTI and SEPIC-SSDTI input voltage is 48V, while the DC input voltage of Diode-Assisted SSDTI is set to 24V

The simulation results of the Diode-Assisted SSDTI are listed with necessary waveforms. From the simulation result, it is identified that the Diode Assisted six switch dual terminal inverter offers better performance when compared to other inverter topologies.

This topology is different from the other two topologies. The diode- capacitor network is used for boosting the voltage gain. It is operated at constant frequency mode of operation. A diode-capacitor structure is included between front-end SSDTI circuits to enhance voltage boost competence. Although Cuk- and SEPIC-derived buck-boost inverters have the same output performance, their results with a diode-capacitor structure exhibit unique factors which can be interpreted by carefully investigating the working principles of diode-assisted SSDTI.

The simulation values of the capacitor voltages of Diode-Assisted SSDTI gets settled at the assumed levels of 20V, 16V, 18V and 19 V

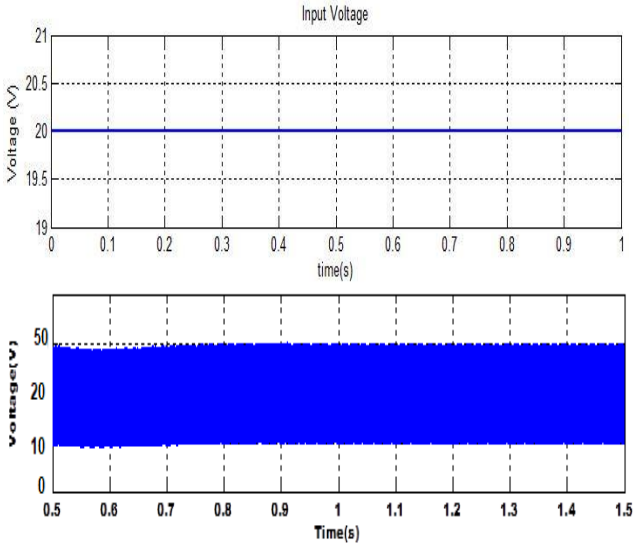


Fig.6 DC Input Voltage and DC bus Voltage

The input of 24V is applied to Diode-Assisted SSDTI. Fig.6 shows the DC input voltage and DC bus voltage which shifts through 10V and 50V for Diode-Assisted SSDTI. Though the input voltage is lesser when compared to other inverter topologies like CUK derived SSDTI and SEPIC derived SSDTI, the boost voltage is 200V.

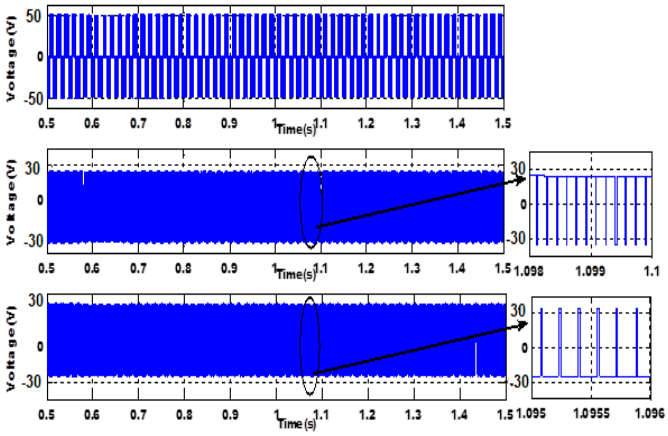


Fig.7 Diode-Assisted –SSDTI LOAD I waveform

The voltage Vab is bipolar ($+V_{DC}$, 0 $-V_{DC}$) in nature whereas the phase voltage Vbc and Vca are unipolar ($\pm V_{DC}/2$) because of the DC link capacitors. As clear from Fig.7, the expected values of frequency and amplitude are attained.

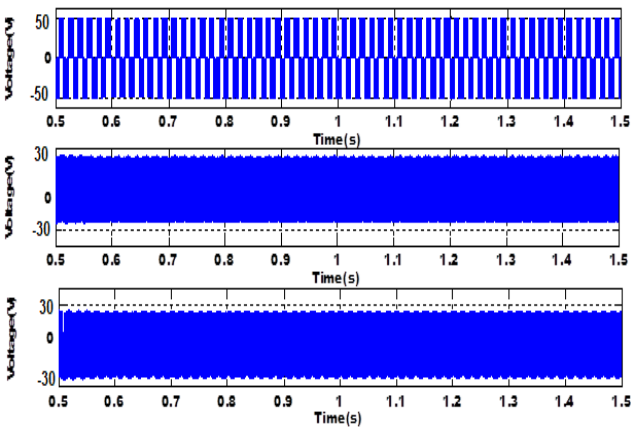


Fig.8 Diode-Assisted –SSDTI LOAD II waveform

The model is simulated for maximum modulation which is limited to 0.8. The output Current is balanced without any DC component. The phase Voltage Vab is unipolar ($+V_{DC}$, 0, $-V_{DC}$) and the other phase voltages Vbc and Vca are bipolar ($\pm V_{DC}/2$) because of the dc link capacitor sources.

V. EXPERIMENTAL RESULTS

The model of diode assisted six switch dual terminal inverter is implemented in hardware. The pulses to SSDTI are generated using Arduino/UNO. The hardware circuit is as shown in fig.9.The input supply to the circuit is 230V, 50Hz Further it is stepped down to a voltage range of 24V AC using step down transformer. The Rectifier circuit converts 24V AC to 20V DC. The diode capacitor network is operated with 20V input supply.Fig.10-12 represents the output voltage vab, vbc, vca and load current of diode-assisted SSDTI for load –I. Both the simulation and experimental waveforms are presented to validate the proposed model. It is identified that Diode-assisted SSDTI offers better performance compared to other boost derived topologies in terms of boost gain. The larger gain is exhibited by the proposed inverter by using a diode–capacitor network that can actively configure itself to perform parallel capacitive charging and series discharging to give an immediate voltage multiplication factor of 2.

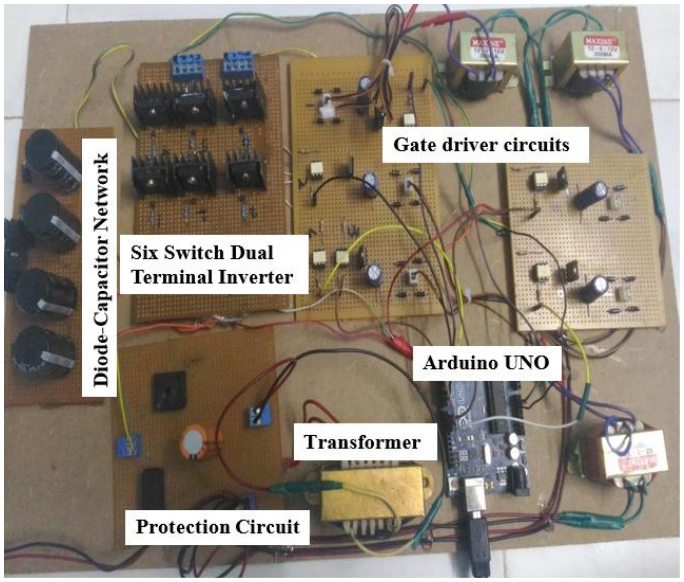
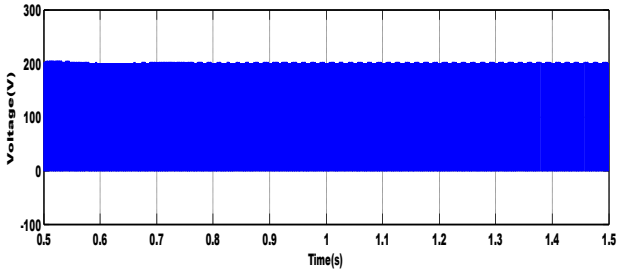


Fig.9 Experimental Setup of the Diode-assisted dual terminal inverter topology



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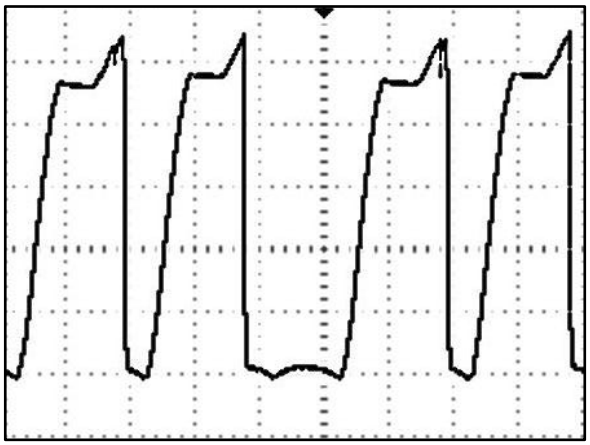
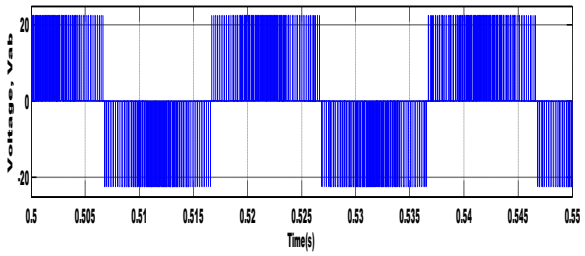


(b)

Fig.10 DC bus voltage of Diode assisted SSDTI (a) simulated (b) experimental



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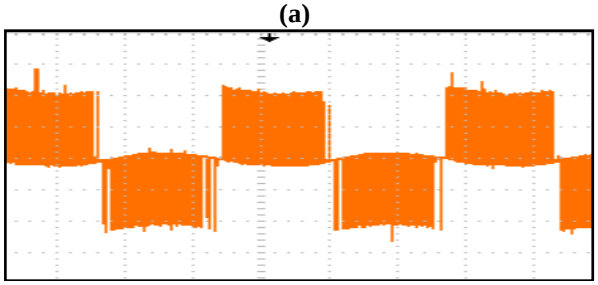

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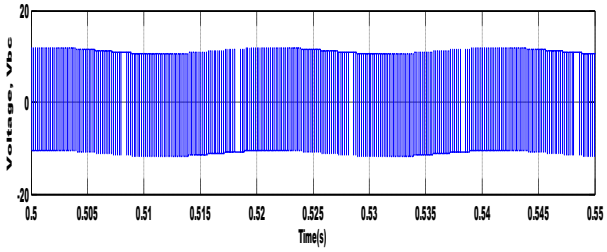

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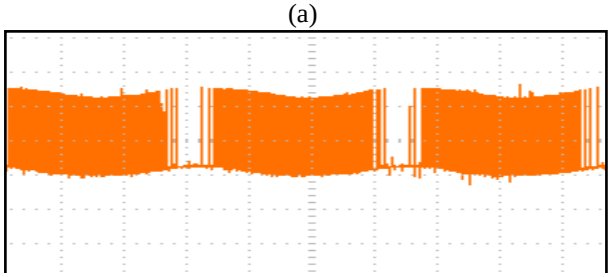

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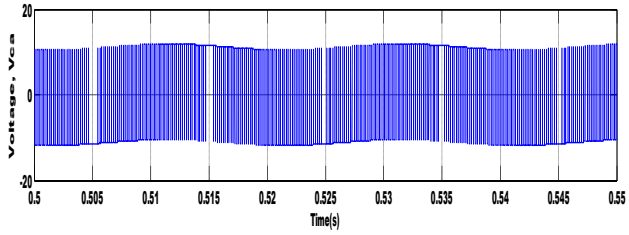

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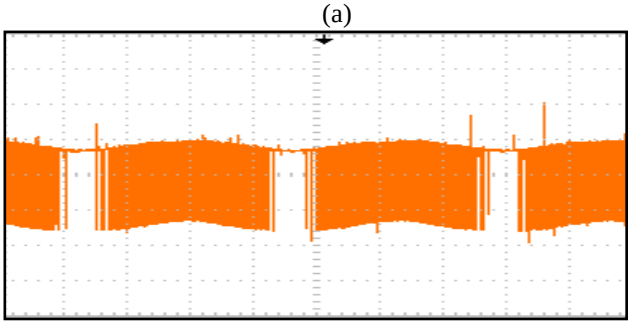
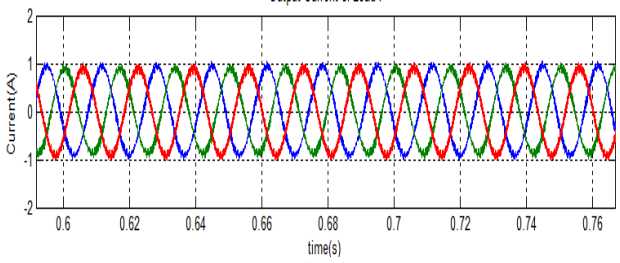


(b)

Fig.11 Line voltage for Load-I- Diode assisted-SSDTI (a) Simulated, (b) Experimental (20v/div-5ms/div)



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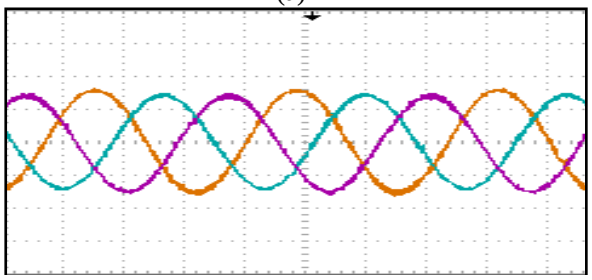

(b)

Fig.12 Load-I- Diode assisted-SSDTI (a) Simulated current, (b) Experimental

Table.1 Simulation Parameters

Parameters	Values
Switching Frequency	6KHz
f_1,f_2	50Hz,60Hz
m_1,m_2,D	0.5,0.5,0.8
L	15mH
C_1,C_2,C_3,C_4	470µF
V_{DC}(CUK,SEPIC)	40V
V_{DC}(DIODE-ASSISTED)	24V
R_{LOAD},L_{LOAD}	15ohm,15mH
B_{CUK} , B_{SEPIC}, $B_{Diode-Ass}$	5,5,10

VI. CONCLUSION

The simulation model of proposed three-phase SSDTI is developed in Matlab/Simulink. The small and medium power applications employ this inverter. Further high modulation indices benefits to lessen the system cost, improving the efficiency, decreasing the power loss and reduces the number of drive circuit thereby enhancing its reliability. The proposed diode-assisted SSDTI offers more voltage gain comparable to alternative buck-boost derived inverters. The simulation model of diode-assisted SSDTI is validated using a prototype model which substantiates the practicality of the suggested inverter. The proposed inverters can contribute to higher accuracy, higher efficiency in higher modulation indices, less conduction loss.

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