Data Encoding Techniques to Reduce the Switching Activity and Crosstalk Delay of On-chip Data Interconnects

M. Chennakesavulu, T. Jayachandra Prasad, V. Sumalatha

Abstract*: *System on Chip (SoC) is providing not only many opportunities but also many challenges. Scaling has applied in SoC to accommodate many processing elements in single silicon area. Scaling has provided decrement in gate delay and the increment in interconnect delay. Coupling capacitance has formed when the spacing between the adjacent interconnects has decreased and it becomes dominant factor when the spacing between the adjacent interconnects has further decreased. Coupling capacitance caused to increment in coupling switching transitions and crosstalk. Coupling switching activity directly affects the dynamic power and crosstalk affects the reliability and performance. Coupling switching activity and crosstalk depend on data patterns travelled on interconnects. Hence, data encoding techniques are essential to alter the data, such way that to reduce the coupling switching activity and crosstalk. In this paper, three data encoding techniques are proposed to limit the switching activity and crosstalk delay in five-wire model. Performance of proposed data encoding techniques has compared to existing techniques. Moreover, efficiency of data encoding techniques is analyzed in terms self -switching activity, coupling switching activity, energy consumption, and crosstalk delay classes for 8-bit data.

Index Terms*: *Crosstalk delay, Data encoding techniques, Switching activity, System on Chip (SoC)

I. INTRODUCTION

Silicon technology drastically changes in recent times and it provides different challenges to designers. Now-a-days, SoC has emerged to incorporate many processing elements in single silicon die. Scaling is applied to optimize the SoC, but scaling decreases the gate delay and increases the interconnect delay. More number of interconnects are required to provide communication between the multiple processing elements. Parasitic capacitances are formed when the spacing between the adjacent interconnects is decreasing and these capacitances become more dominating while further decreasing the distance between the adjacent interconnects. Generally, parasitic capacitances between the adjacent interconnects are termed as coupling capacitance. Coupling capacitance caused to coupling switching activity and crosstalk which are directly affecting the dynamic power, reliability and performance of interconnects. Hence, overall performance of the SoC decided by interconnects. In recent processors, the share of interconnects in terms of dynamic power is 50% in total power of SoC and this share is expected to increase to 65% - 80% in coming years [22]. The network on-chip (NoC) design paradigm [6] is identified as the most prominent way to address the scalability and variability issues. In ultra-deep sub-micron technology, the on-chip communication issues more considerable than the remaining issues [6]. Communication subsystem highly impact on conventional design objectives like power dissipation, delay, reliability and area.

In the literature, some of the techniques are aimed to limit only self-switching activity or coupling switching activity or crosstalk delay classes. Few techniques are aimed to address the combination of switching activity and crosstalk classes. In this paper, we proposed three data encoding techniques which are aimed to reduce the self-switching activity and coupling switching activity and analyzed the effect of the proposed data encoding techniques on crosstalk classes in five-wire model. The rest of this paper is organized as follows. In Section 2, related works are briefly discussed; Section 3 describes an overview of the proposed data encoding techniques. In Section 4, the results of the self-switching activity, coupling switching activity, energy consumption and delay classes in five-wire model are presented and, performance of the proposed data encoding techniques is compared with other techniques. Finally, this paper is concluded in Section 5.

II. RELATED WORKS & CONTRIBUTIONS

In the coming few years, SoC with thousands of cores is expected [35]. In such a SoCs, power contribution of communication subsystem is predominating in the total power budget. Therefore, many researchers are aiming to reduce the power consumption of communication subsystem. Shielding [31] [12] and line to line spacing [16] [2] techniques are aimed to reduce the coupling switching activity but this techniques are almost double the area of interconnects. Data encoding techniques like bus invert (BI) [29] and INC-XOR [23] are aimed to reduce the only self-switching activity for random data patterns. Gray code [30], T0 [3], working-zone encoding [17], and T0-XOR [11] are also aimed to reduce the self-switching activity but for correlated data patterns. Application-specific approaches are presented in [4] [5] [1] [27] [36]. In [29], inversion of the data has been performed if the self-switching activity is greater than the half of the data size.

Data encoding techniques which are addressed only self-activity are not suitable for ultra-deep sub-micron technology where coupling capacitance is dominating factor than the self-capacitance.

Revised Manuscript Received on December 22, 2018.

M. Chennakesavulu, Research Scholar, Department of Electronics and Communication Engineering, JNTUA College of Engineering, Ananthapuramu, Working at RGMCET, Andhra Pradesh, INDIA.

T. Jayachandra Prasad, Professor, Department of Electronics and Communication Engineering, RGM College of Engineering & Technology, Nandayal (Andhra Pradesh), INDIA.

V. Sumalatha, Professor, Department of Electronics and Communication Engineering, JNTUA College of Engineering, Ananthapuramu, Andhra Pradesh, INDIA.

Hence, researchers are aiming to reduce the coupling switching activity. Coupling switching activity has been reduced using more extra control lines, for example, 23 numbers of control lines are used for 32-bit data [14]. The schemes presented in [34] and [9] use less number of control lines, but these techniques are use complex decoder logic. The technique presented in [34] has been selected either, even inverted data or odd inverted data based on which inverted data provided less coupling switching activity. In [9], the coupling switching activity is reduced up to 39%.

The scheme presented in [13] aimed to reduce the coupling switching activity. This technique has been considered two adjacent data bits and classified such data patterns based on coupling switching activity as Type-I (patterns which produces coupling switching activity as 1) and Type-II (patterns which produces coupling switching activity as 2). This scheme has been performed inversion if the sum of Type-I and Type-II transitions greater than or equal to half of the data size. In another coding technique presented in [21], every four bits are encoded as five bits. The occurrence of data patterns "101" and "010" has prevented using shielding. This technique reduces the Type-II transition, but it increases the data transfer time because for every four bits six bits are transmitted. Another technique which is presented in [20] reduces the switching activity by eliminating only Type-II transitions. Madhu et al. [15] proposed Dynamic coding method (DYNAMIC) which reduces the coupling transitions by inverting the sub-bus groups. NOVEL is a coding technique, which is similar to DYNAMIC code proposed by Samala et al. [25] by with a penalty of coupling transitions due to redundant bits. Radhakrishnan proposed Shift Invert Coding (SHINV) [18], which selects the least transition count among the full inversion, left and right shift by one bit position.

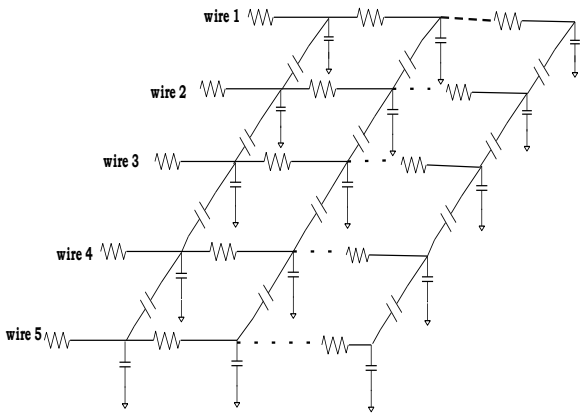

Fig.1 Distributed RC model for five wires.

A. Sathish et al [26] presented a new data encoding technique as a Bus regrouping method (BRG) uses the concept of mirror image data of the original data. A. Sathish et al [26] proposed a novel data encoding technique as BRG-HD which is based hamming distances between present data and data to be transmitted. Energy Efficient Spatial Coding Technique (EESCT) [24] selects the least coupling transition count among the XOR, XNOR, Swapping and normal data possibilities. Nimaja farzadeh et al. [19] presented three schemes. Scheme-1 initially counts Type-1 and Type-II transition of normal data and odd inverted data and it select the best data pattern (either normal data or odd inverted data) which provides less coupling switching activity. Scheme-2 counts the Type-I and Type-2 coupling transitions for normal data, odd inverted data and fully inverted data and finally it select best option which provides less coupling switching activity. Scheme-3 counts the Type-I and Type-II coupling transitions for normal data, odd inverted data, even inverted data, and fully inverted data and finally it select the best option which provides less coupling switching activity. But, these schemes are not considered self-switching activity.

Table 1: Classification of Patterns by signal expressions on wire 3 in Five-Wire Bus

Class C_i	Subclass K_i	Patterns
0	1	↑↑↑↑↑
	2	-↑↑↑↑, ↑↑↑↑-
	3	↑-↑↑↑, ↑↑↑-↑
1	4	-↑↑↑-, ↓↑↑↑↑, ↑↑↑↓↑
	5	--↑↑↑, ↑↑↑- -, -↑↑-↑, ↑-↑↑-
	6	↑-↑-↑, ↑↑↑↓↑, ↑↓↑↑↑
2	7	-↑↑↑↓, ↓↑↑↑-
	8	--↑↑-, -↑↑- -, ↓-↑↑↑, ↓↑↑-↑, ↑-↑↑↓, ↑↑↑-↓
	9	↓↑↑↑↓
3	10	--↑↑↓, ↓↑↑- -, -↑↑-↓, ↓-↑↑-
	11	↓-↑↑↓, ↓↑↑-↓
	12	- -↑-↑, ↑-↑- -, -↑↑↓↑, ↑↑↑↓-, -↓↑↑↑, ↑↓↑↑-
4	13	- -↑- -, ↑-↑-↓, ↓-↑-↑, -↑↑↓-, ↑↑↑↓↓, ↓↑↑↓↑, -↓↑↑-, ↑↓↑↑↓, ↓↓↑↑↑
	14	- -↑-↓, ↓-↑- -, -↑↑↓↓, ↓↑↑↓-, -↓↑↑↓, ↓↓↑↑-
	15	↓-↑-↓, ↓↑↑↓↓, ↓↓↑↑↓
5	16	↓↓↑-↓, ↓-↑↓↓
	17	--↑↓↓, ↓↓↑- -, -↓↑-↓, ↓-↑↓-
	18	--↑↓-, -↓↑- -,↑-↑↓↓, ↑↓↑-↓, ↓-↑↓↑, ↓↓↑-↑
	19	--↑↓↑, ↑↓↑- -, -↓↑-↑, ↑-↑↓-
	20	↑-↑↓↑, ↑↓↑-↑
6	21	↓↓↑↓↓
	22	↓↓↑↓-, -↓↑↓↓
	23	-↓↑↓-, ↑↓↑↓↓, ↓↓↑↓↑
	24	↑↓↑↓-, -↓↑↓↑
	25	↑↓↑↓↑

Crosstalk delay is a deciding factor to measure the performance of overall system performance. Crosstalk Avoiding Codes (CAD) are playing very important role to reduce the crosstalk classes. Forbidden Overlap Codes (FOCs), Forbidden Transition Codes (FTC), Forbidden pattern codes (FPC) and one lambda codes (OLCs) achieve a worst case delay of $(1 + 3\lambda)\tau 0$, $(1 + 2\lambda)\tau 0$, $(1 + 2\lambda)\tau 0$, and $(1+\lambda)\tau 0$, respectively.

CACs with equalization have been presented in [28] and two dimensional CACs are presented in [32]. The efficient encoder/decoder (CODEC) has presented in [7] [8] [33]. Generally two-wire models and three-wire models are used to estimate the crosstalk classes, but these models are not accurate to estimate the delay in ultra-deep sub-micron technology. Hence, five-wire model [10] has been derived to accurately estimate the delay. In five-wire model, data patterns are classified in to 25 sub classes and termed as K_i and again, these 25 subclasses are divided into 7 main classes as C_0, C_1...., C_6 based on delay offered by the subclasses on wire-3. Classification of data patterns on five-wire model shown in Table-1. This paper presents three data encoding schemes mainly aimed to reduce the self and coupling switching activity and effect of these proposed data encoding schemes on crosstalk classes of five-wire model shown in Fig.1 has been analyzed.

III. PROPOSED DATA ENCODING TECHNIQUES

In this section, we present the Overview of the proposed data encoding techniques and detail description of the proposed encoding scheme whose intention is to reduce power dissipation by means of minimizing the coupling transition activities at the links of the interconnection network.

A. Overview of the proposed data encoding techniques

Self and Coupling switching activities are the main source for power dissipation of interconnects. Therefore, proposed data encoding schemes aimed to reduce both the self and coupling activity factors. Let us first depict the power model that contains distinctive elements of energy dissipation of interconnects. The dynamic power dissipation by the interconnects is

$$P_{dyn} = \frac{1}{2}\{\alpha_S(C_S + C_L) + \alpha_C C_C\} * V_{DD}^2 * F_{CLK} \qquad (1)$$

Where α_S is the self-switching activity , α_C is the coupling switching activity , C_S is substrate capacitance , C_L is load capacitance, C_C is the coupling capacitance between two adjacent interconnects, V_{DD} is the supply voltage , and F_{CLK} is the operating clock frequency. Coupling transitions have classified as Type-I, Type-II, Type-III, and Type-IV in two wire models. Type-I coupling transitions are happening when one of the interconnect switches and other interconnect remains same. Type-II coupling transitions are happening when two interconnects are switched simultaneously in opposite. Type-III coupling transitions are happening when two interconnects switched simultaneously on it. Type-IV coupling transitions are happening when two interconnects are not switches. The effective switched capacitance between the two adjacent interconnects varies from type to type, and hence the coupling switching activity α_C is a weighted sum of different types as shown in eqn (2)

$$\alpha_C = W_1 T_1 + W_2 T_2 + W_3 T_3 + W_4 T_4 \qquad (2)$$

Where W_1 is the weight of the Type-I coupling transitions and it is equal to one , W_2 is the weight of Type-2 coupling transitions and it is equal to two, W_3 and W_4 are the weights of Type-III and Type-IV respectively and these equal to zero. Hence, Equation 2 becomes

$$\alpha_C = T_1 + 2T_2 \qquad (3)$$

Therefore, Equation 1 becomes

$$P_{dyn} = \frac{1}{2}\{\alpha_S(C_S + C_L) + (T_1 + 2T_2)C_C\} * V_{DD}^2 * F_{CLK} \qquad (4)$$

C_L is negligible as compared to C_S , so Equation 4 becomes

$$P_{dyn} = \frac{1}{2}\{\alpha_S C_S + (T_1 + 2T_2)C_C\} * V_{DD}^2 * F_{CLK} \qquad (5)$$

Therefore P_{dyn} α $\{\alpha_S C_S + (T_1 + 2T_2)C_C\}$. Here, three schemes named as Normal/Odd inversion by considering the self and coupling transitions (NOSC), Full/Normal/Odd inversion by considering the self and coupling transitions (FNOSC) and Odd/Even/Full/Normal inversion by considering the self and coupling transitions (OEFNSC).

B. NOSC data encoding technique

NOSC data encoding technique is a modified version of scheme-I that proposed in [19]. In this proposed scheme, first we calculated self-switching activity, Type-I coupling switching activity and Type-2 coupling switching activity in two possible ways: : i) between normal data to be transmitted and data which is travelling on interconnects ii) between odd positional inverted data which is to be transmitted and data which is travelling on interconnects. Estimation of self-switching activity, Type-I coupling switching activity and Type-2 coupling switching activity described in Function-1, Function-2 and Function-3 describes for 8-bit data. Total switching activity (sum of self, Type-I and Type-II activities) is estimated in two possibilities and finally data which provides less total switching activity is transmitted. NOSC data encoder produce signal 'INV' to convey the type of the inversion done by the encoder to the decoder to reconstruct the original data. The decoder has tested the 'INV' signal, if INV = '0', then decoder accepts the data as it is, if INV = '1', then decoder is first inverted the received data in odd positions and accepted. Algorithm-1 describes the NOSC encoding and Algorithm-2 describes the NOSC decoding.

C. FNOSC data encoding technique

FNOSC data encoding technique is modified version of the scheme-II that proposed in [19]. In this proposed scheme, first we calculated self-switching activity, Type-I coupling switching activity and Type-2 coupling switching activity in three possible ways: i) between normal data to be transmitted and data which is travelling on interconnects ii) between odd positional inverted data which is to be transmit and data which is travel on interconnects iii) between fully inverted data to be transmit and data which is travel on interconnects. Total switching activity (sum of self, Type-I and Type-II activities) has estimated in three possibilities and finally data, which provides less total switching activity, is transmitted. FNOSC data encoder produce signal 'INV' to convey the type of the inversion done by the encoder to the decoder to reconstruct the original data. The decoder has tested the 'INV' signal, if INV = "00", then decoder has accepted the data as it is, if

INV = "01", then decoder is first inverted the received data in odd positions and accepted, if INV = "11", then decoder is first inverted the received data and accepted.

Algorithm-3 describes the FNOSC encoding and Algorithm-4 describes the FNOSC decoding.

D. OEFNSC data encoding technique

OEFNSC data encoding technique is modified version of scheme III, which is proposed in [19]. In this proposed scheme, first we calculated Self switching activity, Type-I coupling switching activity and Type-2 coupling switching activity in four possible ways: i) between normal data to be transmit and data which is travel on interconnects ii) between data is inverted only in odd positions which is to be transmit and data which is travel on interconnects iii) between data is inverted only in even positions which is to be transmit and data which is travel on interconnects iv) between fully inverted data to be transmit and data which is travel on interconnects.

IV. RESULTS

In this section, performance of proposed data encoding schemes is analyzed in terms self-transition, Type-I coupling transition, Type-2 coupling transition, total coupling transition, and total transition. Effect of these proposed data encoding schemes on data pattern classes in five-wire model has analyzed. Energy and Delay of interconnects are estimated for proposed data encoding schemes. 1000 random input vectors with 8-bit data size are considered to analyze the performance of proposed data encoding schemes. Efficiency in terms of self-transition, Type-I coupling transition, Type-2 coupling transition, total coupling transition, and total transition has reported in this paper, where efficiency equal to $\left(1 - \frac{transition\ count\ with\ data\ encoder}{transition\ count\ with\ out\ data\ encoder}\right) \times 100$.

Table.2 presents different switching activities of data encoding techniques. Fig.2 describes the switching activity efficiency of proposed and existing techniques. NOSC data encoding technique has aimed to improve the performance of the scheme-1 proposed in [19] and this is justified by the results presented in the Table 2. NOSC data encoding technique has provided self-transition efficiency as 9.73%, Type-I transition efficiency as -14.95%, Type-II transition efficiency as 83.05%, total coupling transition efficiency as 53.07% and total transition efficiency as 43.12%. FNOSC data encoding technique has aimed to improve the performance of the scheme-2 proposed in [19] and this is justified by the results presented in the Table 2.

FNOSC data encoding technique has provided self-transition efficiency as 23.49%, Type-I transition efficiency as 7.13%, Type-II transition efficiency as 89.63%, total coupling transition efficiency as 64.39% and total transition efficiency as 55%. OEFNSC data encoding technique has aimed to improve the performance of the scheme-3 proposed in [19] and this is justified by the results presented in the Table 2. OEFNSC data encoding technique has provided self-transition efficiency as 51.2%, Type-I transition efficiency as 14.85%, Type-II transition efficiency as 97.75%, total coupling transition efficiency as 72.39% and total transition efficiency as 67.53%. Moreover, OEFNSC data encoding technique has provided better results than the existing techniques which are presented in this paper. Table 3A and Table 3B presents the effect of proposed and existing data encoding techniques on crosstalk delay classes of five-wire model. Energy consumption and Delay of interconnects are estimated from the calculated switching activity and crosstalk delay classes.

Table 2: Switching activity counts for different data encoding

	S.T	Type-I	Type-II	C.T	TT
UNCODED	21841	22416	50868	73284	95125
BINV	12939	22416	19706	42122	55061
BSHIFT	18978	23300	37852	61152	80130
EESCT	16394	47685	3586	51271	67665
DYNAMIC	16751	28534	16952	45486	62237
BRG	17098	33849	4426	38275	55373
BRG_HD	12408	27389	8128	35517	47925
SCH-1	19681	37156	11970	49126	68807
SCH-2	15115	29980	12604	42584	57699
SCH-3	18289	22784	7426	30210	48499
NOSC	19717	25767	8626	34393	54110
FNOSC	16712	20819	5280	26099	42811
OEFNSC	10659	19089	1146	20235	30894

Fig 3 describes the energy efficiency and delay efficiency of proposed and existing data encoding techniques. NOSC data encoding technique has provided energy efficiency as 48.79% and delay efficiency as 73.42%. FNOSC data encoding technique has provided energy efficiency as 60.35% and delay efficiency as 83.62%. OEFNSC data encoding technique has provided energy efficiency as 71.08% and delay efficiency as 89.9%. Overall performance of OEFNSC data encoding technique is much better than the all other data encoding techniques which are presented in this paper.

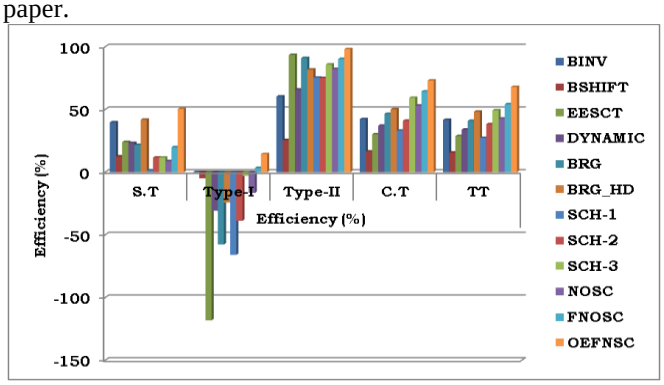

Fig 2: Switching activity reduction efficiencies of data encoding techniques

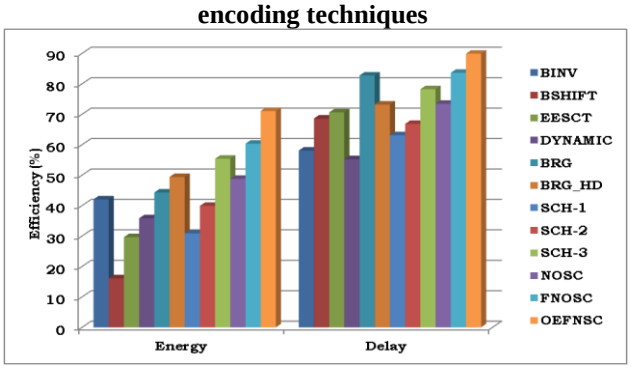

Fig 3: Energy and Delay efficiencies of data encoding techniques

Table 3A: Crosstalk classes C0, C1, C2, C3 and C4 for different data encoding techniques

	CLASS - C0			CLASS - C1			CLASS - C2			CLASS - C3			CLASS - C4		
	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15
UNCODED	0	0	3	3	27	53	0	4	0	0	0	217	935	490	9
BINV	0	0	0	0	4	43	1	10	0	30	0	367	511	196	0
BSHIFT	12	21	12	3	24	48	0	18	0	52	0	356	500	27	0
EESCT	0	0	3	33	60	19	0	100	0	199	0	459	1375	888	116
DYNAMIC	0	18	12	7	66	43	26	814	0	837	12	485	730	1270	307
BRG	1752	2187	857	311	408	1451	265	68	3	0	0	1129	716	119	30
BRG_HD	47	89	18	115	367	88	0	600	0	140	0	717	1144	673	0
SCH-1	308	563	8	93	1241	603	298	412	34	149	286	1565	1836	440	9
SCH-2	35	76	5	25	490	250	6	66	33	135	156	973	1596	404	1
SCH-3	1918	3067	30	473	1152	0	201	1155	1	220	8	213	955	370	0
NOSC	1146	1961	27	767	1849	0	655	541	21	278	404	630	1651	821	9
FNOSC	944	1679	0	568	1793	0	747	610	3	108	9	224	1432	113	0
OEFNSC	0	0	0	713	1135	0	0	724	0	56	0	114	873	286	0

Table 3B: Crosstalk classes C5 and C6 for different data encoding techniques

	CLASS - C5					CLASS - C6				
	K16	K17	K18	K19	K20	K21	K22	K23	K24	K25
UNCODED	500	377	1115	1954	40	21	1022	710	2068	2286
BINV	0	230	990	1856	22	0	62	544	663	0
BSHIFT	0	123	924	1217	0	0	98	377	50	0
EESCT	86	292	1205	654	0	0	67	92	41	14
DYNAMIC	302	1409	1575	217	87	0	80	240	123	0
BRG	0	6	91	268	117	0	31	24	6	0
BRG_HD	0	87	291	823	0	0	67	18	392	0
SCH-1	180	194	498	783	27	9	271	72	91	24
SCH-2	29	137	644	1252	3	0	175	70	83	45
SCH-3	0	149	377	380	3	0	51	16	141	12
NOSC	62	16	152	217	3	0	7	80	332	29
FNOSC	0	68	215	216	0	0	5	81	0	0
OEFNSC	0	47	76	41	0	0	5	3	0	0

V. CONCLUSION

In this paper, proposed data encoding techniques are independent of type of interconnects used and application handled by communication subsystem in SoC. Hence, these data encoding techniques are applicable to any type of interconnects to reduce the dynamic power dissipation of interconnects. The proposed schemes are to reduce not only the self-switching activity, but also the coupling switching activity that is especially liable for link energy dissipation in the deep sub-micron meter technology regime as compared to the previous encoding schemes proposed in the literature. Moreover, the proposed data encoding techniques are considerably reduces the crosstalk delay classes of five-wire mode, hence, these techniques are improves the performance of interconnects. An extensive assessment has accomplished to evaluate the impact of proposed data encoding schemes. Proposed data encoding techniques have provided better performance in all aspects.

REFERENCES

1. G. Ascia, V. Catania, M. Palesi, and A. Parlato, "Switching activity reduction in embedded systems: A genetic bus encoding approach," IEE Proc. Comput. Digit. Tech., vol. 152, no. 6, pp. 756–764, Nov. 2005.
2. R. Ayoub and A. Orailoglu, "A unified transformational approach for reductions in fault vulnerability, power, and crosstalk noise and delay on processor buses," in Proc. Design Autom. Conf. Asia South Pacific, vol. 2. Jan. 2005, pp. 729–734.
3. L. Benini, G. De Micheli, E. Macii, D. Sciuto, and C. Silvano, "Asymptotic zero-transition activity encoding for address busses in low-power microprocessor-based systems," in Proc. 7th Great Lakes Symp. VLSI, Mar. 1997, pp. 77–82.
4. L. Benini, G. De Micheli, E. Macii, M. Poncino, and S. Quer, "Power optimization of core-based systems by address bus encoding," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 6, no. 4, pp. 554–562, Dec. 1998.
5. L. Benini, A. Macii, M. Poncino, and R. Scarsi, "Architectures and synthesis algorithms for power-efficient bus interfaces," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 19, no. 9, pp. 969–980, Sep. 2000.
6. L. Benini and G. De Micheli, "Networks on chips: A new SoC paradigm," Computer, vol. 35, no. 1, pp. 70–78, Jan. 2002.
7. C. Duan, C. Zhu, and S. P. Khatri, "Forbidden transition free crosstalk avoidance CODEC design," in Proc. Annu. Design Autom. Conf., 2008, pp. 986–991.
8. C. Duan, V. H. C. Calle, and S. P. Khatri, "Efficient on-chip crosstalk avoidance CODEC design," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 4, pp. 551–560, Apr. 2009.
9. C. P. Fan and C. H. Fang, "Efficient RC low-power bus encoding methods for crosstalk reduction," Integr. VLSI J., vol. 44, no. 1, pp. 75–86, Jan. 2011.
10. Feng Shi, Xuebin Wu, and Zhiyuan Yan, "New crosstalk avoidance codes based on a novel pattern classification," IEEE Trans.VLSI systems, Aug.2012.

11. W. Fornaciari, M. Polentarutti, D. Sciuto, and C. Silvano, "Power optimization of system-level address buses based on software profiling," in Proc. 8th Int. Workshop Hardw. Softw. Codesign, May 2000, pp. 29–33.
12. M. Ghoneima, Y. I. Ismail, M. M. Khellah, J. W. Tschanz, and V. De, "Formal derivation of optimal active shielding for low-power on-chip buses," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 25, no. 5, pp. 821–836, May 2006.
13. K. W. Ki, B. Kwang Hyun, N. Shanbhag, C. L. Liu, and K. M. Sung, "Coupling-driven signal encoding scheme for low-power interface design," in Proc. IEEE/ACM Int. Conf. Comput.-Aided Design, Nov. 2000, pp. 318–321.
14. C. G. Lyuh and T. Kim, "Low-power bus encoding with crosstalk delay elimination," IEE Proc. Comput. Digit. Tech., vol. 153, no. 2, pp. 93–100, Mar. 2006.
15. M. Madhu, V. Srinivas Murty and V. Kamakoti, "Dynamic coding Technique for Low-Power data bus," Proceeding of IEEE computer Society Annual Symposium on VLSI (ISVLSI'03), 2003, pp. 252-253.
16. L. Macchiarulo, E. Macii, and M. Poncino, "Wire placement for crosstalk energy minimization in address buses," in Proc. Design Autom. Test Eur. Conf. Exhibit., Mar. 2002, pp. 158–162.
17. E. Musoll, T. Lang, and J. Cortadella, "Working-zone encoding for reducing the energy in microprocessor address buses," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 6, no. 4, pp. 568–572, Dec. 1998.
18. J. Natesan and D. Radhakrishnan, "Shift invert coding (SINV) for low power VLSI," IEEE Conference on Digital System Design, March, 2004, pp. 190-194.
19. Nima Jafarzadeh, Maurizio Palesi, Ahmad Khademzadeh and Ali Afzali-Kusha, "Data Encoding Techniques for Reducing Energy Consumption in Network-on-Chip," IEEE Transactions on very Large Scale Integration (VLSI) Systems, Vol. 22, No.3, 2014, pp. 675-685.
20. M. Palesi, G. Ascia, F. Fazzino, and V. Catania, "Data encoding schemes in networks on chip," IEEETrans. Comput.-Aided Design Integr. Circuits Syst., vol. 30, no. 5, pp. 774–786, May 2011.
21. P. P. Pande, H. Zhu, A. Ganguly, and C. Grecu, "Energy reduction through crosstalk avoidance coding in NoC paradigm," in Proc. 9th EUROMICRO Conf. Digit. Syst. Design Archit. Methods Tools, Sep. 2006, pp. 689–695.
22. M. S. Rahaman and M. H. Chowdhury, "Crosstalk avoidance and errorcorrection coding for coupled RLC interconnects," in Proc. IEEE Int. Symp. Circuits Syst., May 2009, pp. 141–144.
23. S. Ramprasad, N. R. Shanbhag, and I. N. Hajj, "A coding framework for low-power address and data busses," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 7, no. 2, pp. 212–221, Jun. 1999.
24. J.V.R. Ravindra, Navya Chittarvu, M. B. Srinivas, "Energy Efficient Spatial Coding Technique for Low Power VLSI Applications," International workshops on System on chip for real time applications, 2006, pp. 201-204.
25. NK Samala, D Radhakrishnan and B Izadi "A Novel deep submicron Bus Coding for Low Energy," Proceedings of the International Conference on Embedded Systems and Applications, pp. 25 – 30, June 2004.
26. A Sathish, "Efficient technique to minimize dynamic power and crosstalk delay on on-chip data bus in deep sub micron technology," Ph.D. dissertation, JNTUH, 2015.
27. R. Siegmund, C. Kretzschmar, and D. Muller, "Adaptive Partial Businvert encoding for power efficient data transfer over wide system buses," in Proc. 13th Symp. Integr. Circuits Syst. Design, Sep. 2000, pp. 371–376.
28. S. Sridhara, G. Balamurugan, and N. Shanbhag, "Joint equalization and coding for on-chip bus communication," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 16, no. 3, pp. 314–318, Mar. 2008.
29. M. R. Stan and W. P. Burleson, "Bus-invert coding for low-power I/O," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 3, no. 1, pp. 49–58, Mar. 1995.
30. C. L. Su, C. Y. Tsui, and A. M. Despain, "Saving power in the control path of embedded processors," IEEE Design Test Comput., vol. 11, no. 4, pp. 24–31, Oct.–Dec. 1994.
31. A. Vittal and M. Marek-Sadowska, "Crosstalk reduction for VLSI," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 16, no. 3, pp. 290–298, Mar. 1997.
32. X. Wu, Z. Yan, and Y. Xie, "Two-dimensional crosstalk avoidance codes," in Proc. IEEE Workshop Signal Process. Syst. Conf., Oct. 2008, pp. 106–111.
33. X. Wu and Z. Yan, "Efficient CODEC designs for crosstalk avoidance codes based on numeral systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 4, pp. 548–558, Apr. 2011.
34. Z. Yan, J. Lach, K. Skadron, and M. R. Stan, "Odd/even bus invert with two-phase transfer for buses with coupling," in Proc. Int. Symp. Low Power Electron. Design, 2002, pp. 80–83.
35. D. Yeh, L. S. Peh, S. Borkar, J. Darringer, A. Agarwal, and W. M. Hwu, "Thousand-core chips roundtable," IEEE Design Test Comput., vol. 25, no. 3, pp. 272–278, May–Jun. 2008.
36. S. Youngsoo, C. Soo-Ik, and C. Kiyoung, "Partial bus-invert coding for power optimization of application-specific systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 9, no. 2, pp. 377–383, Apr. 2001.