A Hybrid AVC and PDM Aided Full Bridge Resonant Converter for Induction Heating Application

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Abstract*: This article entrusts a hybrid asymmetric voltage cancellation (AVC) and pulse density modulation (PDM) switching scheme for full bridge resonant converter which can be applied for induction heating (IH) application. The single stage converter topology suggested in this paper is efficient compared to the conventional dual stage. The pulse generation for the converter is strategically performed by hybridizing AVC and PDM techniques. The inherent dead band in AVC technique facilities soft switching, in turn, reduces the switching losses, whereas PDM enhances the power control ranges without a change in switching frequency. IH application requires a wide range of power control with minimal losses. This research put forth an effort to hybridize AVC and PDM to enhance the control and conversion without a change in frequency. The work has been duly simulated in a simulation environment (MATLAB/Simulink) and also a hardware prototype has been realized. The results prove that the work is advantageous in many aspects.

***Index Terms*: Asymmetric voltage cancellation, induction heating, pulse density modulation**

I. INTRODUCTION

Induction heating (IH) or electromagnetic heating works on the principle of electromagnetic induction to heat the workpiece without any direct contact. The development of eddy current on the body of the workpiece creates the circulating current within the body of the metal causes the heating effect. The inherent advantages of this heating are high power conversion efficiency, high efficiency, no contamination of workpiece, lesser heating time constant etc. The inverter needed for IH application needs high switching frequencies varying from 20 kHZ to 100 kHZ [1-2] and the rating may be upto 500 kW. To feed power to the IH load, the commercial 50 Hz supply needs to be converted with high-frequency ac (HFAC). This can perform by two approaches: ac-dc-ac and ac-ac based converters topology [3]- [4]. In ac-dc-ac approach, commercial frequency supply is rectified with the uncontrolled rectifier, filtered using the bulky capacitor, HFAC inverter powers the IH load. In this approach, the source side power factor is reduced and more power losses due to the two-stage power conversion [5]. Various two stage topologies like a single switch, full bridge, and half-bridge are developed by the authors in [6]- [8], the advantages and disadvantages were discussed.

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Recently, the contribution of a single stage converter fed topologies is vital due to fewer losses and less requirement of components [9]. Matrix converter fed IH topology was developed by Ó. Lucia et.al., with lesser components [10]. This topology shows a good performance in dc link ripple reduction with high efficiency, but defining the switching pattern find hard for IH application. In [11], cyclo-converter with anti-parallel bidirectional IGBT was proposed by Hisayuki Sugimura. But, the system possesses a very low input power factor and high THD. The common capacitor dual half-bridge inverter was proposed in [12]. The rectification process is done by only two diodes which reduces the conduction loss. Power control with lesser switching losses remains an uphill task in IH based applications. Thus various modulation topologies were presented by the researchers to achieve the task. The most commonly used to technique was a pulse with modulation (PWM) which was used by various researchers. The main drawback of that scheme is hard switching, for dynamic load variations and limited power control range [13]. Pulse frequency modulation is developed by Park et. al. for induction jar applications, controlling the power output by varying the frequency of the switching pulses [14]. This system has a limited power control range and high electromagnetic interference. C. Carretero et. al. used phase shift control for shifting the phase of voltage and current to vary the output power [15]. Due to the variation in the phase angle, the semiconductor switches are operated in the hard switching mode. For fixed frequency power control, pulse density modulation (PDM) [16] and asymmetrical voltage cancelation (AVC) [17] control technique is generally preferred. In PDM control technique, the variation in the density of the control pulses is done by comparing the high-frequency pulses with low frequency. The interaction of low frequency causes more aquatics noise in the system. In this problem is overcome by using the AVC technique. In these technique, the switching frequency is maintained constant. The output power is controlled by varying the control angle. Thus, there will a provision for zero voltage switching operation. But, in this control scheme, there is more even harmonics on the source side because of the asymmetric operation. It is apparent from the literature that, tendering a novel control algorithm with lesser switching loss, a vast range of power control, without changing the switching frequency remains the uphill task in the research arena.

Hence this work put forth, the hybrid combination of AVC and PDM control technique to achieve the said task. The single stage inverter suggested here, boost the output voltage to match the load requirement with high power density. The posited control technique reduces the switching losses thereby the system efficiency is increased.

II. SYSTEM DESCRIPTION

A. Single stage converter topology

Fig. 1 shows the circuit of a single stage full bridge series resonance inverter (SRI). The topology comprised of two half-bridge inverter which delivers power to two IH loads (load 1 and 2). The Ls is the boost inductance, switches M_1 and M_4 forms half-bridge inverter 1 and switches M_2 and M_3 comprise half-bridge inverter 2. The IH load is modeled with an equivalent series resistor and inductor ($R_{eq,x}$ and $L_{eq,x}$ respectively) and the resonant capacitor $C_{r,x}$. The dc link capacitor C_s is used for filter the dc ripple. The boost operation in the SRI reduces the current flowing in the coil and the MOSFETs under the normal operating condition. This is so, due to boosting operation, the output voltage increases thereby the flowing through the coil decreases. Thus, the increase in output voltage reduced the losses thereby the efficiency of the system increases.

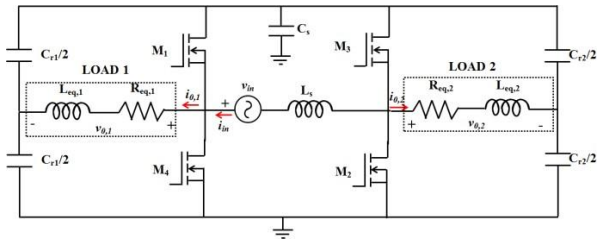


Fig.1. Single stage full bridge SRI [9]

B. Modes of Operation

Fig. 2 shows the equivalent circuit of the inverter when load 1 is active. During its operation, one part of half bridge arrangement is used to feed the IH load, whereas the other part acts as the boost rectifier. For load 1, the switches M1 and M4 are switched to yield high frequency ac voltage output (V0), whereas the switches M2 and M3 aids in rectifying the positive and negative cycles of the supply main respectively. The red arrow represents the direction of supply current and the green arrow represents the charging and discharging current of the capacitor.

Mode 1: In this mode the power switch M1 is turned on for t0 interval (DTs) and switch M2 remains in on state for the entire positive cycle of the supply voltage. The source current flowing path is Vin-load 1-Cr1/2-M2-Ls as shown in Fig 2(a). Similarly Cs discharges via M1-load 1-Cr1/2

Mode 2: In this mode, in addition to M2, M4 is also activated for t1 interval (1-DTs) and M1 is turned off. Thus the current flowing path is shown in Fig 2b. The source current flows through Ls-M2-M4-Vin and Cs charges with i0,1 via Cr1/2.

Mode 3: In this mode, the polarity of the main supply is reversed and therefore M3 act as a half wave rectifier for negative half cycle of the main voltage. Till t2 duration (DTs), the switch M1 is activated and the supply current flows through vin-M1-M3-Ls. Similarly i0,1 charges the Cs via M1. The illustrations of the current paths are shown in Fig 2c.

Mode 4: In this mode, along with M3, M4 is activated for t3 duration (1-DTs). During this period, Cs discharges via Cr1/2- load 1-M4 as shown in Fig 2d. Similarly, the supply current flows through v_{in}-C_s-M_3-Ls.

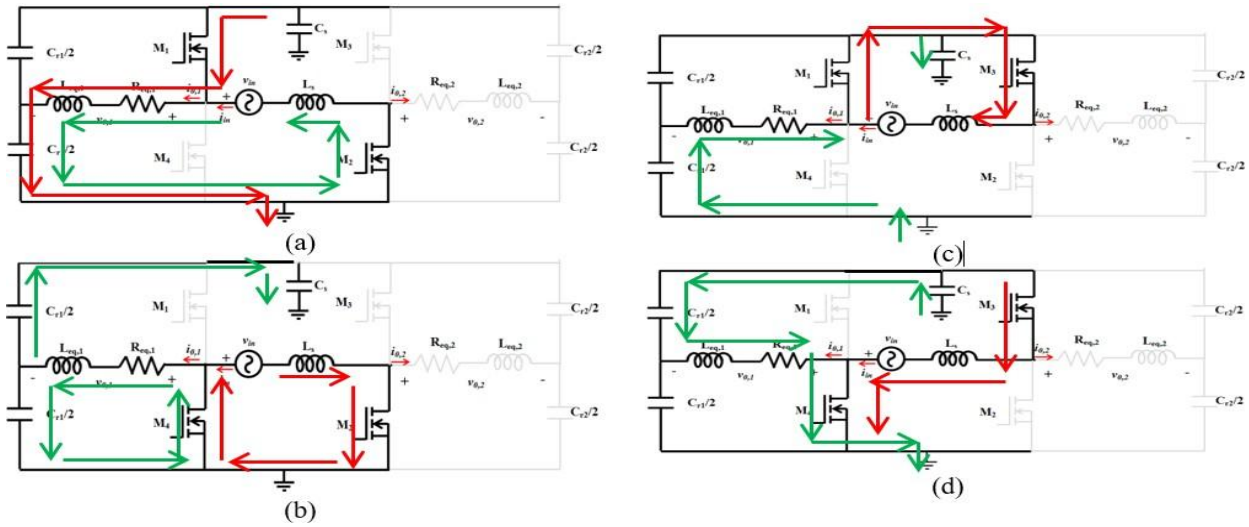


Fig. 2. Equivalent circuit of the inverter when load 1 is active, (a) mode 1& (b) mode 2 during positive power supply, and (c) mode 3 & (d) mode 4 during negative power supply

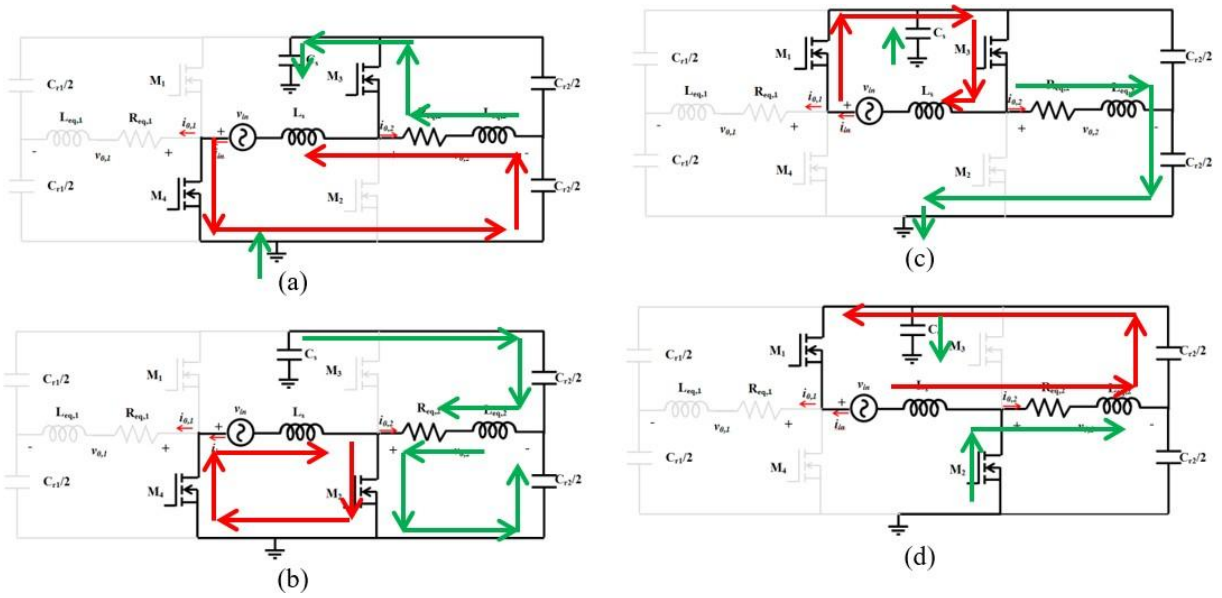


Fig. 3. Equivalent circuit of the inverter load 2 is active, (a) mode 1& (b) mode 2 during positive power supply and (c) mode 3& (d) mode 4 during negative power supply

Similarly, Fig. 3 shows the equivalent circuit of the resonant inverter when load 2 is active. The operation sequence explained for load 1 holds good for load 2. The operating waveforms during positive half cycle main and negative half cycle main are shown in Fig 4.

C. Modulation technique

The modulation technique plays a vital role in controlling the output power of the inverter with lesser losses. In the paper, hybrid modulation is proposed to control the output power with lesser losses. The hybridization of AVC and PDM control techniques results in better performance compared to the other. The pulse generation of the hybrid modulation technique is shown in Fig. 3. The PDM pulses are generated by comparing the high-frequency pulses with low-frequency pulses using the logical AND operator. Then the width of the positive or negative half cycle is reduced to certain control angle α. The produced pulses are given as switching pulses to the inverter switches to convert 50 Hz supply into HFAC.

III. SIMULATION RESULTS

The MATLAB Simulink software is used for simulating high-frequency AC power circuit with 100 W rating. Table 1 shows the design specifications of the AVC-PDM controlled single-stage series resonant inverter. High-frequency ac is produced by alternative turning on and off of the semiconductor switches (M_1, M_2, M_3, M_4).

Table 1 Design specifications

S.No	Parameters	Values
1	Input voltage	60V
2	Load resistance ($R_{eq,1}$ & $R_{eq,2}$)	2 Ω
3	Load resistance ($L_{eq,1}$ & $R_{eq,2}$)	0.05 mH
4	Capacitance ($C_{r,1}$, $C_{r,2}$)	1.3 µF
5	Source inductance	0.1 mH
6	Output power (P_{rated})	100 W
7	Resonant frequency	20 kHz
8	Switching frequency	22 kHz
9	F_{PDM}	20 Hz
10	Control angle (α)	30 °

In the AVC technique, there is a depletion in the positive half cycle or negative half cycle of the output voltage. Thus pulse to the switch M_1 is diminished to the control angle α while contrasting with the other switches as shown in Fig. 4. To control the output power, D_{PDM} is varied. The duty of the PDM signal is given by D_{PDM}, which defines the output power. For the variations in the D_{PDM}, the magnitude of the output power is reduced. The D_{PDM} is given by

The resonant frequency f_r of the series RLC resonant tank is given by

$$f_r = \frac{1}{2\pi\sqrt{L_{eq} C_r}} \quad (1)$$

$$D_{PDM} = \frac{T_{on,PDM}}{T_{oPDM}} \qquad (2)$$

$$P_{out} = D_{PDM} P_{rated} \qquad (3)$$

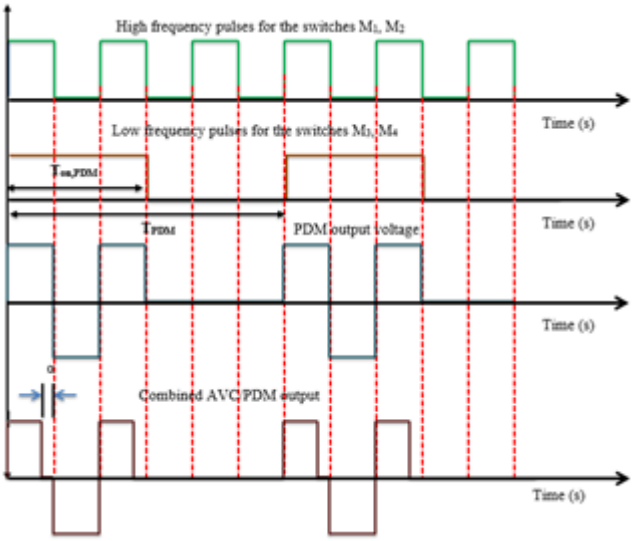


Fig. 3 Pulses generation of hybrid modulation technique

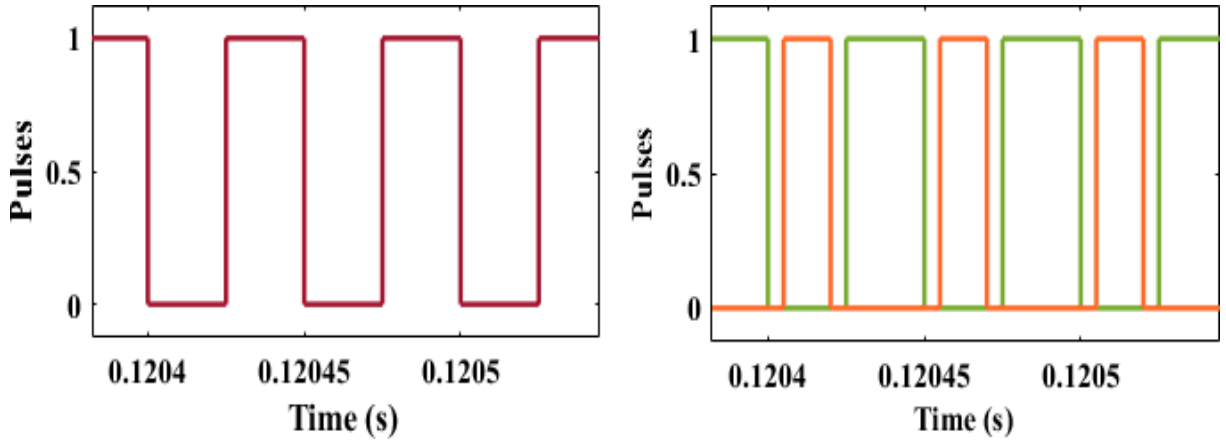


Fig. 4 switching pulses for α = 30

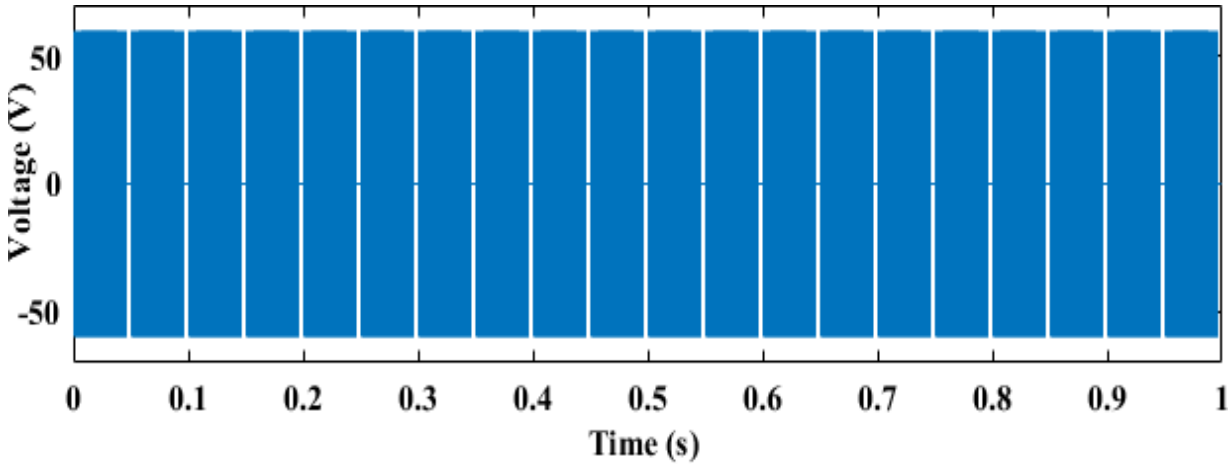


Fig. 5 Output voltage waveform with D_{PDM} = 90 % and α = 30°

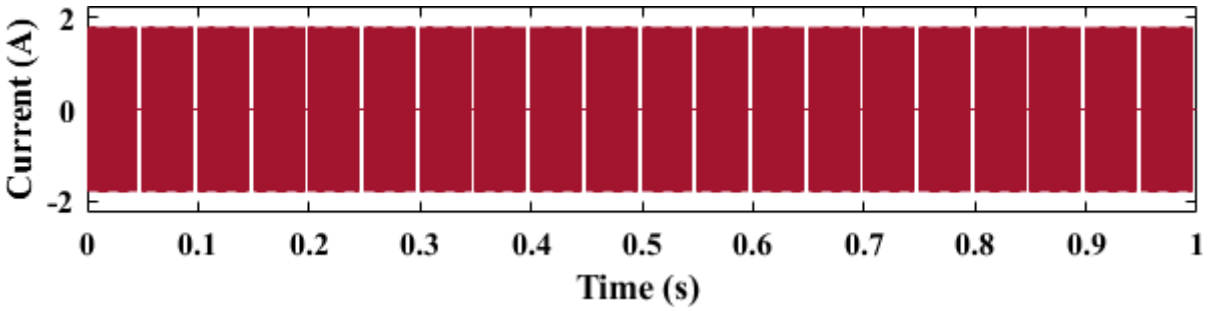


Fig. 6 Output current waveform with D_{PDM} = 90 % and α = 30°

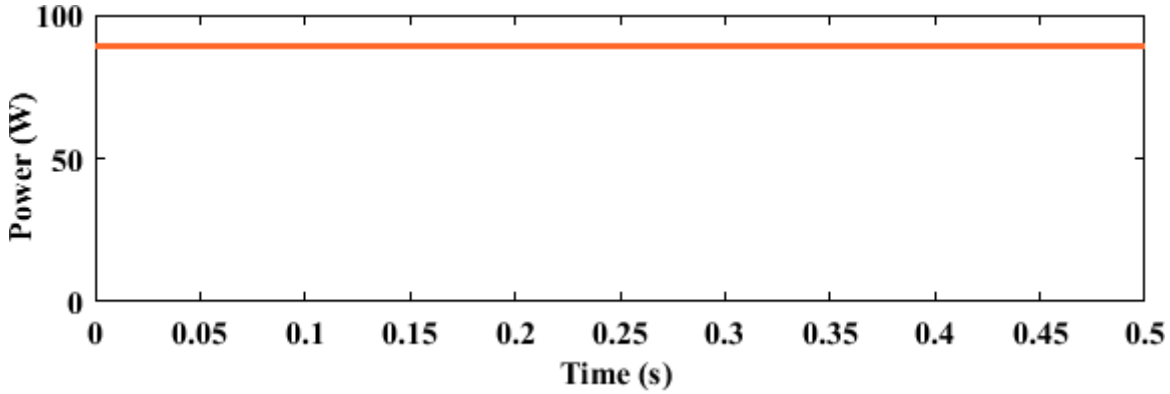


Fig. 7 Output power waveform with D_{PDM} = 90 % and α = 30°

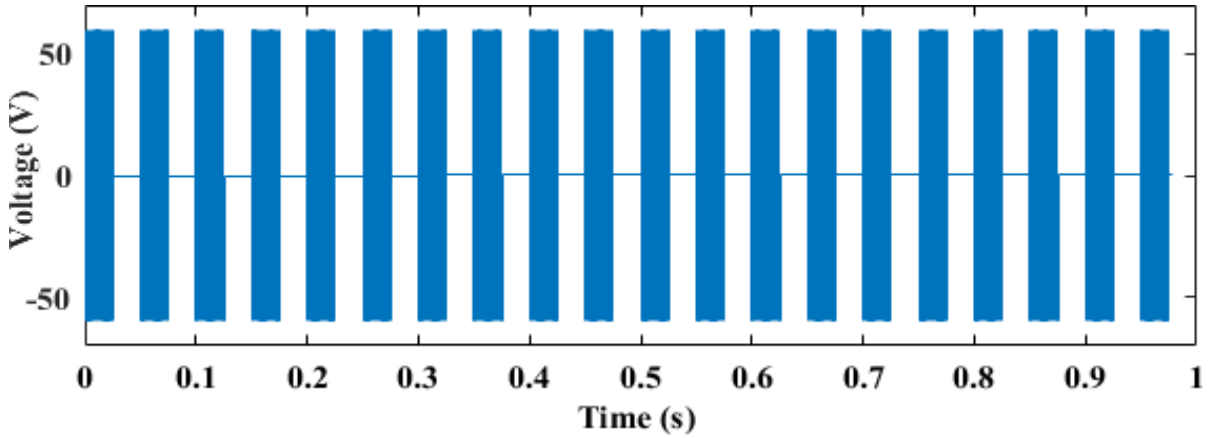


Fig. 8 Output voltage waveform with D_{PDM} = 50 % and α = 30°

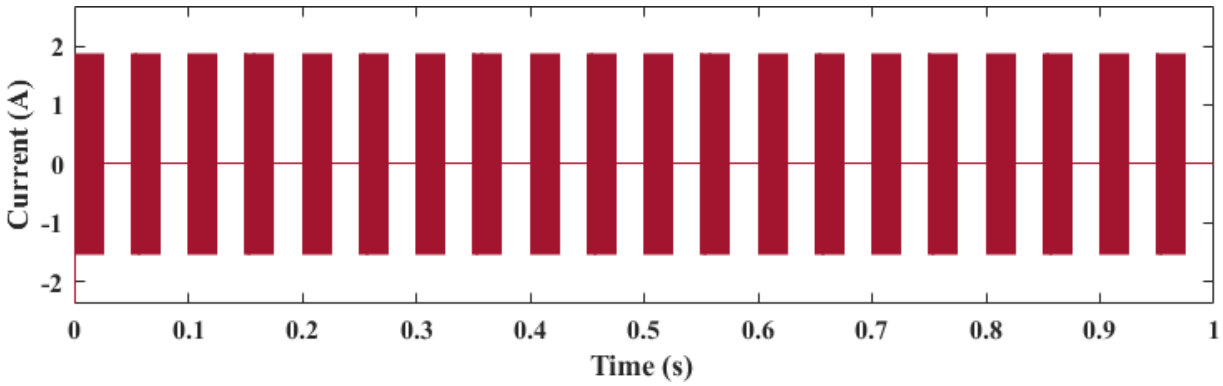


Fig. 9 Output current waveform with D_{PDM} = 50 % and α = 30°

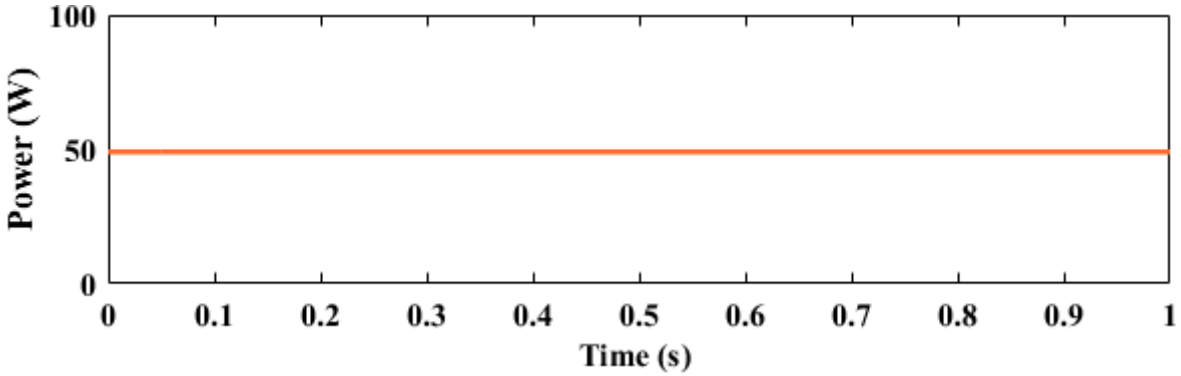


Fig. 10 Output power waveform with D_{PDM} = 50 % and α = 30 °

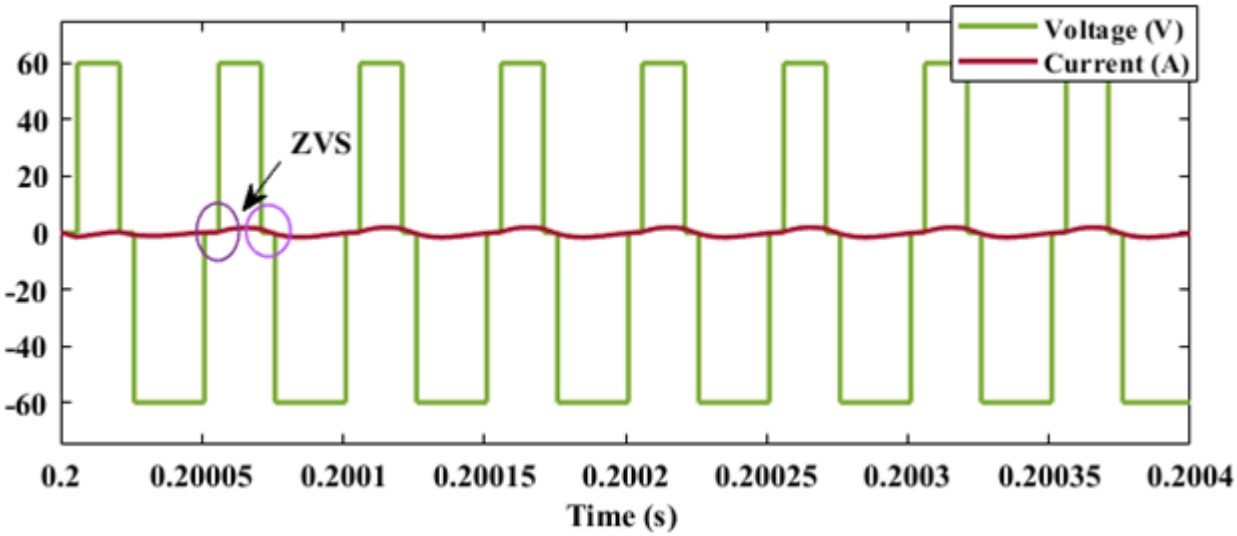


Fig. 11 Expanded view of load voltage and current waveform

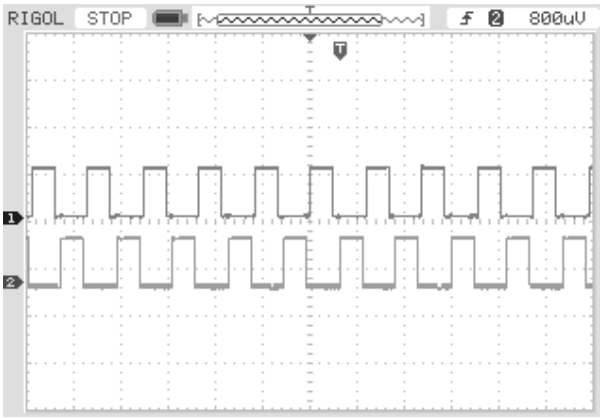
Thus, the variation in output power for various DPDM is simulated. Fig. 5 and 6 shows the output voltage and current waveforms with DPDM = 90 % and α = 30 °. It is observed that, at 90 % of the DPDM, the output power is 0.9 times the rated power. It is evident from Fig. 7. To evaluate the control techniques, the duty cycle is varied to DPDM = 50 %. The corresponding voltage, current, and power waveform are shown in Fig. 8, 9 and 10 respectively. It is observed that the net output power reduces, to 50 W with 50 % of DPDM. In the control scheme, as the frequency of the inverter is not varied, zero voltage switching is realized for the whole operating region. It evident from the enlarged view of the load voltage and current waveform as shown in Fig. 11.

IV. HARDWARE RESULTS

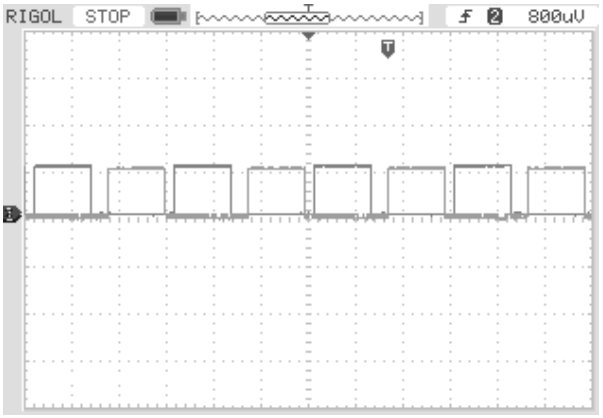
The experimental setup of the simulated system is developed for 100 W. Test setup of the single stage converter °corresponding voltage and current waveform are shown in topology with AVC-PDM control technique is shown in Fig. 12. The system realized for 90 W and 60 W set power. To get 90 W output power the value of DPDM should be chosen as 90 %. In all cases, the value of the control angle α is considered as 30°. The switching pulses for the inverter are shown in Fig. 13(a) and Fig. 13(b). the switching dead time is 0.005 µs. It is perceived from Fig. 13(b), that the width of the pulses is reduced to the switch switches M1 and M2. The Fig. 13(c). The enlarged view of the current and voltage waveform is shown in Fig. 13(d). The DPDM is varied from
90 % to 50 %. The corresponding voltage and current waveform are shown in Fig. 13(e). It is perceived that there is the discontinuous in the current and voltage waveform reduces the power output. Fig. 13(f) shows the soft switching waveform.

Fig. 12 Test setup of the single stage converter topology with AVC-PDM control techniques

Load 2 **Single stage converter Controller Load 1**

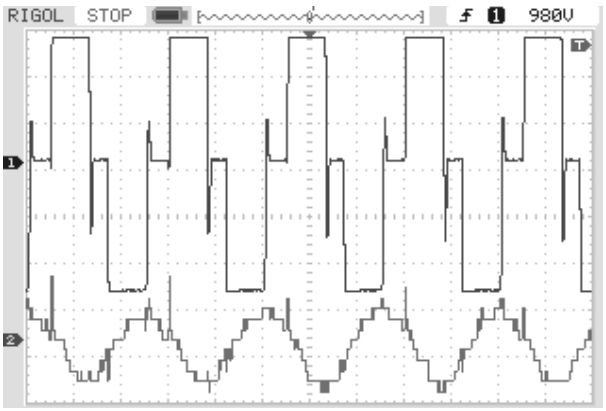


(a)

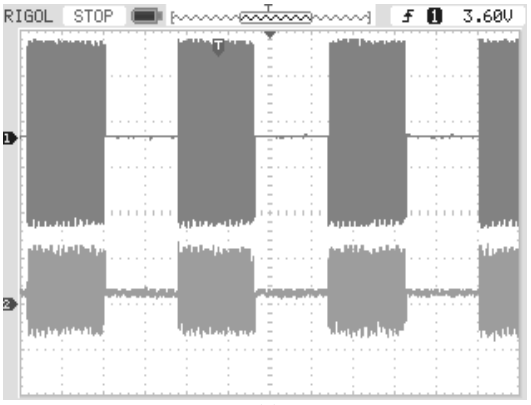


(b)

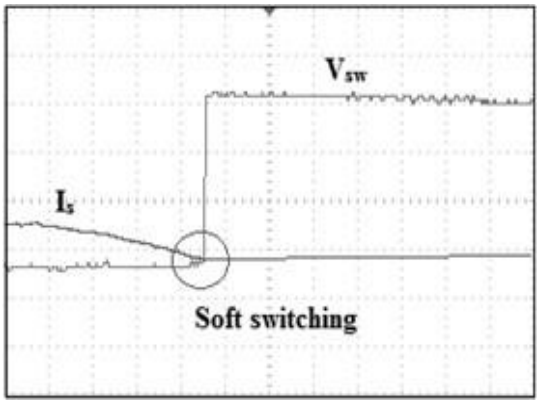
(c)



(d)



(e)



(f)

Fig. 13 Output waveforms (a) Switching pulses for the switches M_3 and M_4 (10 V/div, 50 µs) (b) Switching pulses for the switches M_1 and M_2(10 V/div, 20 µs) (c) Output voltage (40 V/div, 50 µs) and current waveform (1 A/div, 50 µs) with D_{PDM} = 90 % and α = 30 ° (d) Enlarged view of output voltage (40 V/div, 50 µs) and current waveform (1 A/div,
50 µs) (e) Output voltage (40 V/div, 50 µs) and current waveform (1 A/div, 50 µs) with D_{PDM} = 50 % and α = 30 ° (f) Soft switching waveform

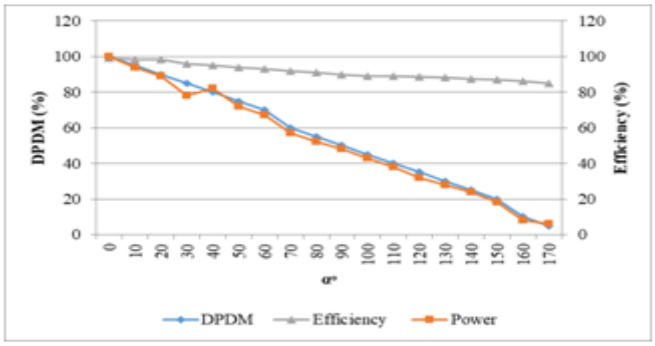


Fig. 14 Variation of efficiency and output power for various values of control angles and D_{PDM}

Table 2 Comparison of the single stage topology with conventional topology

Parameters	Converter topology in [18]	Single stage topology
Controlled switches	4	4
Uncontrolled switches	4	-
Number of load(s)	1	2
Efficiency at rated power	94%	97%
Power factor	0.85	0.92

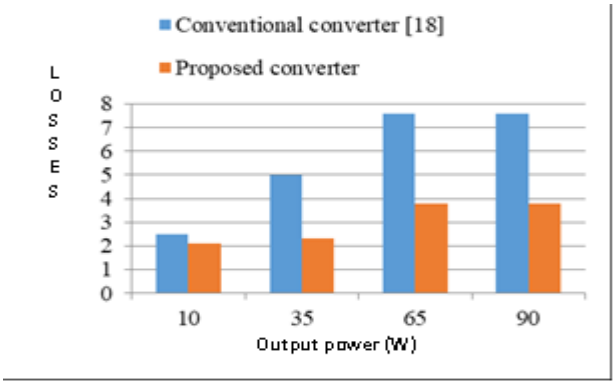


Fig. 15 Variation of inverter module losses for different values of output power

Variation of efficiency and output power for various values of control angles and D_{PDM} is shown in Fig. 14. It is observed that the output power can be variegated by controlling the D_{PDM} and α. Also, the system efficiency is higher when it is operated at rated power. And it decreases for increasing control angle and D_{PDM}. The comparison of the single stage topology with a conventional topology is shown in Table 2. Variation of inverter module losses for different values of output power is shown in Fig. 15. The single stage topologywith proposed modulation techniques results in higher efficiency with lesser module power losses.

V. CONCLUSION

In this work, the AVC-PDM based hybrid modulation technique is proposed for a single stage converter topology. As there is no variation in the switching frequency, ZVS is assured in the topology. The system efficiency is higher because of the lesser components and soft switching in the inverter. The regulation of the output power can be performed for various DPDM with lesser losses. Also, the variation of the output power from 0 % to 100 % is possible with changing the switching frequency. But determining the control angle finds hard, which is responsible for the switching loss. The further work can be extended for the closed loop system to regulate the output power as per the requirement.

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