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Vlsi Implementation of Image Fusion Using Pca Algorithm With Maximum Selection Rule

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Abstract: Nowadays, medical diagnosis is achieved by using the Digital Image Processing (DIP) techniques. Because, the role of DIP is more important in the medical field to identify the activities of the patients related to various diseases. Magnetic Resonance Imaging (MRI) and Computer Tomography (CT) scan images are used to identify the tissues in various organs of the human body. In brain medical imaging, the brain structural information without functional data will be given by MRI scan. But, CT scan image includes the functional data with brain activity. To improve the low dose CT scan, Principal Component Analysis (PCA) algorithm is used in this paper which is implemented on FPGA. The Maximum Selection Rule (MSR) is used to select the high frequency component from the image. Application Specified Integrated Chips (ASIC) and Field Programmable Gate Array (FPGA) performances analysed for the different methods. In 180nm technology, PCA-IF architecture achieved 5.145mm^2 area, 298.25mW power, and 124ms delay.

Index Terms: Application specified integrated chips, Field programmable gate array, Principle component analysis, Maximum selection rule.

I. INTRODUCTION

The process of combining two or more images into one image is called as image fusion. Based on the image stage, the fusion has been classified into two types, those are transform domain and spatial domain fusion [1]. Through which, all kinds of information possible to take from the different imaging modalities or different images [2]. IF is used in so many applications like medical, automated industry, engineering field, military, etc. [3]. Among all those fields, medical field application is more important in IF which helps to identify the human problems [4]. In medical, two major models like MRI and CT scan help to analyze the normal and abnormal tissue and internal structure of human body. Both MRI and CT contain some different information of the human brain [5]. MRI scan is used to identify soft tissues which detect the skull problems as well as CT scan is used for hard tissue to identify the bone structure [6]. There are many techniques used in literature for IF like pixel level based, decision level, and feature level based [7].

Many of the existing algorithms have been used for IF process such as Electrical Capacitance Tomography (ECT) algorithm [8], Non-Subsample Contour let Transform (NSCT) [9], sparse representation and decision [10], and Curvelet transform [11]. The main problem with these methods is information loss. To check the hardware utilization and improve the efficiency, the IF has been implemented in FPGA. The way of implementation is also different in FPGA. In FPGA, multi model method [12], and configurable pixel level [13] methods have been implemented for IF process. The hardware utilization of these methods is high. To overcome these problems, PCA algorithm with the maximum selection rule is implemented in this paper. These methods are implemented in FPGA architecture to improve the efficiency of the IF. At last, FPGA and ASIC performances are improved in proposed method compared to conventional methods.

II. LITERATURE REVIEW

A. Mishra, S. Mahapatra, and S. Banerjee [13], presented Modified Frei-chen based image fusion method. This method was utilized in Structural Similarity (SS), and contrast in Night Vision (NV) based two scale decomposition. This method achieved 48%, 15%, and 100% of improvements in total edge transfer, SS, and NV. This architecture was implemented in the Xilinx tools which consume 4% of resources. This proposed method was analyzed in synopsis tool with 90nm CMOS technology. This algorithm provides less accuracy and less fusion efficiency.

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D.P. Bavirisetti, and R. Dhulli [12] proposed two scale image fusion using saliency detection. This method was used for Saliency extraction process, which can highlight the significant information. This works gave better results compared to multi-scale fusion technique. This method failed to process the medical images perfectly.

M. Pemmaraju, S. C. Mashetty, S. Aruva, M. Saduvelly, and B. B. Edara [12] presented wavelet based image fusion using FPGA. This proposed method was implemented in Xilinx EDK 10.1 using Spartan 3E. This FPGA contains combinational blocks which are flexible for high speed application. This architecture contains memory, flip flops, and LUT. This proposed method was applied to multi focus image fusion. DWT doesn't provide stationary outputs and low frequency component has less efficiency.

Y. Yang, Y. Que, S. Huang, and P. Lin [16] proposed multi model based image fusion based on fuzzy logic. With the help of type 2 fuzzy, NSCT was analyzed using pre-registered source image for getting low and high bands. Low frequency bands are used by local energy algorithm. The proposed fused image was taken with the help of inverse NSCT with all sub bands. The accuracy, contrast, and versatility were also evaluated. The main drawback of this method is low spatial resolution.

P.C. Bhaskar, and V.R. Munde [17] proposed image fusion using Non-sub sampled Shear-let Transform (NST) in FPGA implementation. Input image was separated into individual image co-efficient using NST. Different rules were applied to fuse the high and low bands. With the help of inverse NST, the fused image was taken. This proposed method was implemented in Xilinx system generator and MATLAB. The power value was reduced in proposed method. But, the hardware utilization of this proposed method is high.

III. PCA-IF ARCHITECTURE

Image Fusion is one of the important processes for obtaining more information from different images. The overall process of image fusion is shown in Fig.1.

- As both CT and MRI images are in pixel format, these files have to be converted in to bit file format.
- The input CT image is read into MATLAB and the pixel is converted to binary value. These binary values are stored in a text file.
- The same process is applied to MRI images also.
- Both CT and MRI image pixels are given to the PCA component which gives the fused image.
- PCA is implemented in Verilog and the final output is written in text file.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

In this section, the experimental result and discussion of the proposed methodology is detailed effectively in terms of performance measure. The performance of the proposed methodology was evaluated by ASIC and FPGA performances.

A. Experimental setup

- With the help of MATLAB, those binary values are converted to pixel which shows the fused image.

A. Maximum Selection Rule

In order to make the image more focused the pixel with large grey value is to be considered. The algorithm helps in choosing the in-focus regions by selecting the greatest value for each pixel, and results in a more clear focused output. Comparison is made for the pixel values of each image and the greatest pixel value is assigned to the corresponding pixel.

B. PCA architecture

The architecture of PCA is shown in Fig. 1 which contains control engine, covariance matrix, MUX, multiplier, adder, and comparator.

With the help of detected spike waveform, the covariance matrix is calculated. The covariance matrix is called as PC spike waveform. The MAC address is used for distilling and orthogonalization process to improve the PCA efficiency. Comparator and right shift are used to shift the procedure and level checking. The entire algorithm split into four processing units and the data is stored in register files. Finite State Machine (FSM) is used for scheduling and allocating the resources during the PCA processing. FSM is very effective for controlling the remaining signal [17].

These outputs are helpful to perform the image fusion. The fused architecture binary output is read in MATLAB for showing fused image.

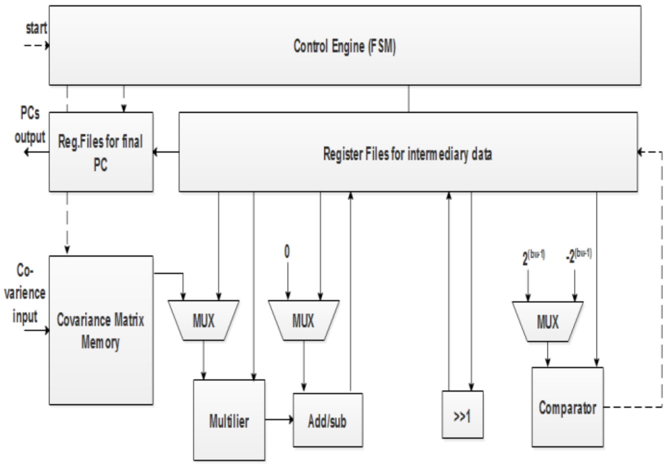

Figure.1. PCA architecture

The proposed approach experimented in a system comprising 4GB RAM with 3.30 GHz, i3 processor and 500GB hard disk. The architecture has been implemented using Verilog language. MATLAB tool is used to read the input image and to show the fused output. Modelsim 10.5 tool is used to write a Verilog code and verifying the timing diagram. Xilinx 14.4 is used for evaluating FPGA performances like LUT, flip flop, slices, and frequency. The

Cadence RTL compiler is used to calculate ASIC performances such as area, power, and delay.

C. Discussion

The input images (CT and MRI) are shown in Fig. 2 and Fig. 3. Which are taken from two different image modalities CT scanner and MRI scanner. These images are converted to binary which are shown in Fig. 4 and Fig. 5.

The ASIC performance of the different methods is tabulated in Table 1. In this table, values of ASIC performance of the Existing-I [15], existing-II [17],

existing-III [19], and PCA-IF are compared.

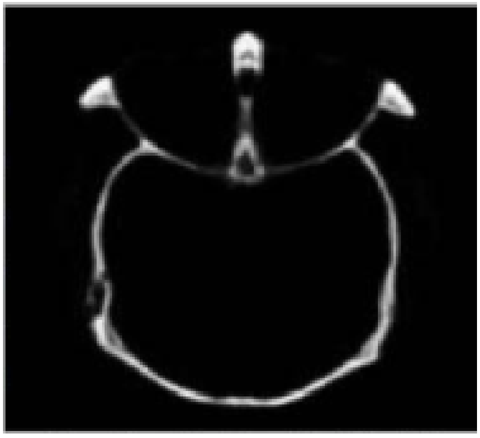

Figure.2. Input CT image

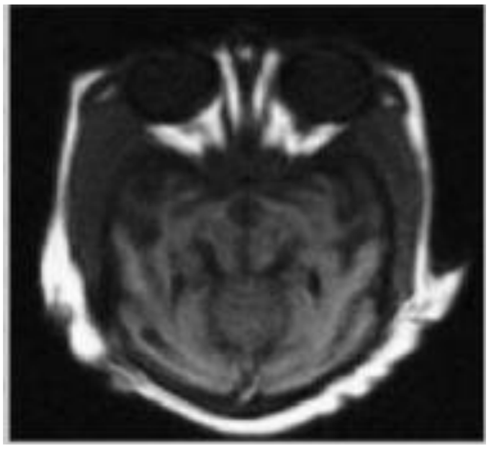

Figure.3. Input MRI image

```
10000011
01000001
11001100
00111011
01000001
10111011
10110101
10110011
00010011
01001110
00011000
01000110
11111001
11111010
```

Figure.4. Binary value of CT image

```
10001000
10011001
00111001
01110000
11111110
00101100
00110101
10001100
11001110
00101011
10110101
01110000
11111100
10100001
```

Figure.5. Binary value of MRI image

Table 1. Comparison of area, power, and delay for different methods

Technology	Method	Area (mm2)	Power (mW)	Dela y (ms)
180nm	Existing-I [l4]	8.471	387.1	180
	Existing-II [l6]	7.321	345.71	158
	Existing-III [18]	6.214	314.21	143
	PCA-IF	5.145	298.25	124
45nm	Existing-I [l4]	3.014	198.25	104
	Existing-II [l6]	2.987	168.12	101
	Existing-III [18]	2.158	148.687	98
	PCA-IF	1.982	111.21	91

The comparison of ASIC performances is tabulated in Table 1. Here, all the methods are implemented and the results are tabulated. All the methods are implemented in the cadence RTL compiler with 180nm and 45nm technology. From this table, it's clear that PCA-IF provides better

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performances when compared to previous existing architectures.

Table 2. Comparison of FPGA performances for different methods

Devices	Method	LUT	Flip flop	slices	Frequency
Virtex 4	Existing-I [14]	4038	4852	2857	250.3
	Existing-II [16]	4002	4657	2654	289.64
	Existing-III [18]	3541	4214	2011	314.21
	PCA-IF	3014	3987	1968	355.14
Virtex 5	Existing-I [14]	3104	4125	1964	185.41
	Existing-II [16]	3014	4032	1847	193.21
	Existing-III [18]	2987	3987	1752	255.14
	PCA-IF	2741	3789	1648	287.96

The FPGA performances are tabulated in table.2. In this table, Virtex 4 and Virtex 5 devices are used to evaluate LUT, flip flop, slices, and frequency.

These values are shows that the PCA-IF architecture achieves better FPGA performance parameters. The hardware utilizations are evaluated from this FPGA performance. The RTL schematic diagram of PCA is shown in Fig. 6. Finally, the fused image is shown in Fig. 7. This RTL schematic was taken from the Xilinx tool.

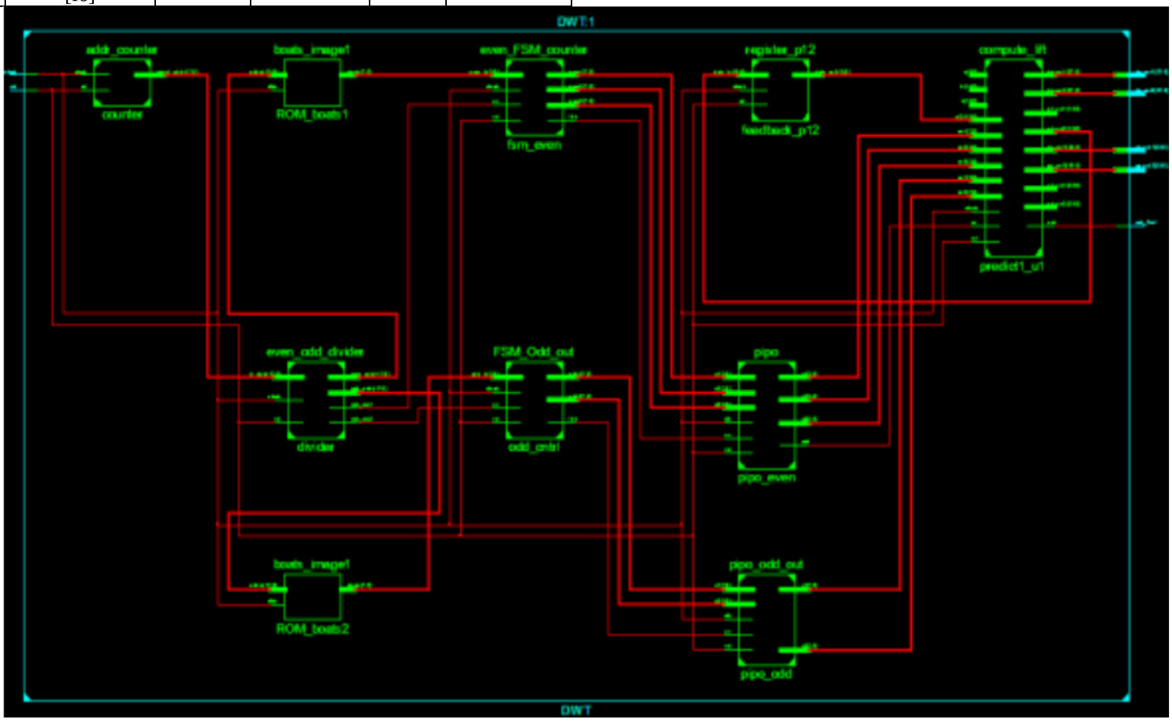

Figure.6. RTL schematic diagram of PCA

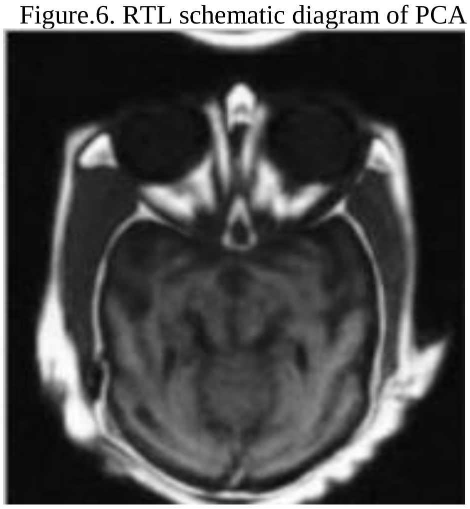

Figure.7. Fused image

V. CONCLUSION

The proposed architecture has been designed effectively in order to reduce the hardware utilization. In this work, PCA-IF architecture has been designed to perform the image fusion. In this work, medical images like MRI and CT have been used in the fusion process to obtain more information. The hybrid VLSI architecture provided better fused image compared to previous works. The PCA-IF architecture was implemented using Verilog code. PCA method with maximum selection rule was used to reduce the power and area consumption. The ASIC and FPGA performance were analyzed for different architectures. In 180nm technology, PCA-IF architecture achieved 5.145mm^2 area, 298.25mW power, and 124ms delay. In Virtex 4, the proposed architecture achieved 3014 LUT, 3987 flip flop, 1968 slices, and 355.14 MHz frequency. In the future, different kind of optimization algorithm will be designed to improve the ASIC and FPGA performances.

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