# High Speed Multiplier Design Using Kogge Stone Adder

**R.Arun Sekar, D.Ganeshkumar, A. Rajendran, S.Sasipriya**

***Abstract:*** ***The multipliers are the heart of any high-speed computational devices. The multipliers are fully made up of combinational circuits. They have a large circuit design with high gate density, in fact high transistor density. This large active area provides space to have large power dissipation. Obviously, this provides a concern to reduce power dissipation in the multipliers. In this work a high-speed multiplier is designed based on the fast-parallel prefix adder as Kogge stone adder. Different adders are compared with respect to the speed of operation and Kogge stone is the best among the different adders. As Vedic multiplier is considered as the fast multiplier, the adder part in this Vedic multiplier is replaced by Kogge stone adder to form the hybrid high speed Vedic multiplier. This Proposed hybrid Vedic multiplier proved to be efficient in terms of power, delay and Power delay product.***

***Index terms: Carry Skip Adder (CSKA), Carry Look ahead Adder (CLA), Carry Save Adder (CSA), Carry Select Adder (CSLA), Kogge Stone Adder (KSA), Vedic Multiplier (VM).***

## I. INTRODUCTION

Growth is a focal limit in math exercises subject to this assignment, for instance, Multiply and Accumulate (MAC)and inner thing are among a bit of the regularly used Computation Intensive Math Functions (CIAF)currently realized in various Digital Signal Processing (DSP)applications, for instance, convolution, Fast Fourier Transform (FFT), isolating and in chip in its math and justification unit. Since increase overpowers the execution time of most DSP estimations, so there is a need of quick multiplier. At this moment, increment time is so far the prevalent factor in choosing the direction procedure length of a DSP chip[16]. The enthusiasm for quick getting ready has been extending a direct result of developing PC and banner taking care of utilizations. Higher throughput calculating assignments are fundamental to achieve the pined for execution in various progressing sign and picture taking care of uses[17]. One of the keys calculating exercises in such applications is enlargement and the progression of snappy multiplier circuit has been a subject of eagerness over decades[18,19,20,21]. Diminishing the time delay and power usage are extraordinarily central necessities for a few applications. Different adders[1]-[3] are compared based on their area, speed and power.Fast parallel adders [4] called Kogge stone adder is used in the analysis of different adders.This work presents assorted multiplier models. In this paper a direct 16-bit Vedic multiplier is proposed which relies upon UrdhvaTiryakbhyam (Vertically and Crosswise) Sutra of the Vedic Math's. Two parallel numbers (16-bit each) are expanded with this Sutra. The essential thought of this paper is that the control use of the circuit and minimize delay of the proposed plan.

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## II. ADDER ARCHITECTURES

### A. Carry skip adder

In the carry skip adders, the bits can engender the whole distance from even a tiny bit position to most piece position under specific conditions. It is otherwise called carry by-pass adder [5],[6]. Consider the condition in which the twofold info sets to be included have no less than one '1' esteem and furthermore the carry input Cin = 1. If this condition holds, the carry input is engendered to the complete and the yield Cout = 1. Generally, the carry in info is undulated all the through the adders to produce the carry yield. The proliferating procedure is finished by the carry skip chain appeared in Figure 1. The Figure 1 contains the fundamental ripple carry adder and the carry skip square. The carry skip square examines the above said condition and play out the skipping activity.

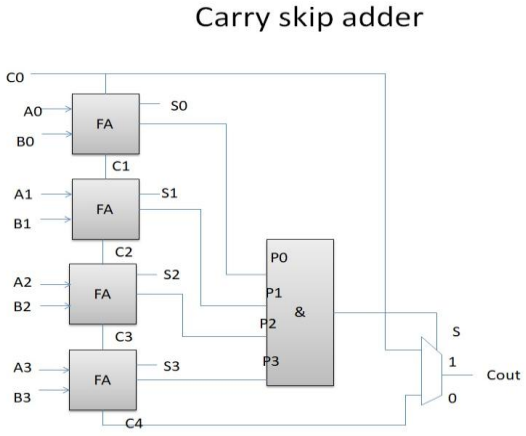


**Fig.1**-bit Carry Skip Adder

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### B. Carry lookahead adder

In the ripple carry adder and the carry skip adder, the engendering of the carry is the tedious factor.

The Carry Look-Ahead Adder [7] gives an answer by ascertaining the

carry signals dependent on the paired contributions to be included.

The outcome is the decrease in the carry proliferation time.

In the full adder, two transitional signs, Carry Propagate (Pi) and Carry Generate (Gi), can be characterized as,

$Pi = Ai \oplus Bi$ (2.1)

$Gi = AiBi$ (2.2)

The carry spread and carry produce signals depend just on the sources of info Ai and Bi. Presently the entirety and carry yields can be characterized as,

$Si = Pi \oplus Ci$ (2.3)

$Ci+1 = Gi + PiCi$ (2.4)

Condition (2.4) demonstrates that the carry flag will be stated just in two moments if:

i) $Ai = Bi = 1$ (2.5)

ii) $((Ai = 1)$ or $(Bi = 1))$ and $Ci = 1$ (2.6)

In view of Equation (2.6), the carry yields of every adder stage can be communicated based as

C0 = input carry

C1 = G0 + P0C0

C2 = G1 + P1C1 = G1 + P1(G0 + P0C0) = G1 + P1G0 + P1P0C0

C3 = G2 + P2C2 = G2 + P2G1 + P2P1G0 + P2P1P0C0

The 4-bit adder is developed with carry look forward rationale is appeared in figure 2. It has three phases. The principal arrange produces the Pi and Gi factors. In view of these data sources the carry look-ahead adder creates the carry signals for the third stage. The third dimension produces the last total yield.

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**Fig. 3**-bit Carry Look-ahead Adder

### C. Carry Select Adder

The carry select adder [8] diminishes the engendering delay utilizing parallel calculation. The yield bits are pre-processed for both conceivable carry input qualities. At that point right yield is chosen from these two yields utilizing a multiplexer. Figure 3 demonstrates the carry select adder with each stage contains a couple of 1-bit adder and a multiplexer. The adder in the best computes the whole having the carry contribution as '0'. The adder in the base ascertains the entirety having the carry contribution as '1'. The real carry chooses between these two yields utilizing multiplexers.

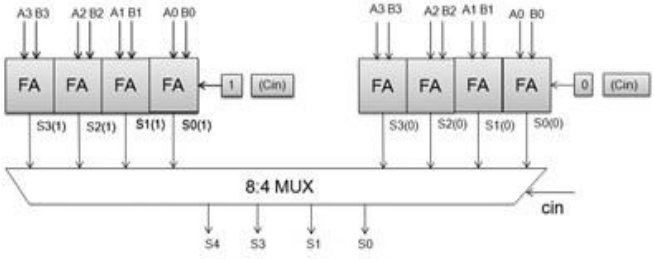


**Fig.2**bit Carry Select Adder

### D .Carry save adder

Carry save adder [9] is a rapid adder. The schematic diagram of carry save adder is shown in the figure 4. A carry save adder comprises of stepping stool of remain solitary full adders. It expends three n bit information whole numbers to be included and delivers n bit entirety and carry. Carry save adder comprises full adders with no carry fastening. A carry save adder is a quick claiming there is no carry engendering inside each full adder cell. Carry save adder is utilized to figure fractional items in whole numbers duplications. A Carry-Save Adder shown in figure 4 is only a lot of one-piece full adders, with no carry affixing. In this way, a n-bit CSA gets three n-bit operands, to be specific a(n-1)..a(0), b(n-1)..b(0), and cin(n-1)..cin(0), and creates two n-bit outcome esteems, sum(n-1)..sum(0) and cout(n-1)..cout(0). The most vital utilization of a carry save adder is to compute the halfway items in whole number increase. This considers models, where a tree of carry save adders is utilized to figure the halfway items quick. One 'ordinary' adder is then used to include the last arrangement of carry bits to the last halfway items to give the last increase result. For the most part, a quick carry lookahead or carry select adder is utilized for this last stage, to acquire the ideal execution.

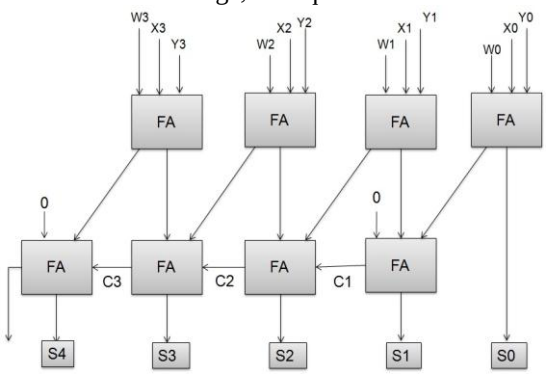


**Fig.4** bit Carry Save Adder


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**E . Kogge stone adder**

Kogge stone adder [10] is a parallel prefix type of carry look forward adders.

It comprises of four vertical stages, every vertical phase of Kogge stone adder creates an engender and produce bit.

It is considered as the quickest adder and it is broadly utilized in businesses for superior of arithmetic circuits. In Kogge stone adder carrys are registered quick by processing them in parallel at the expense of expanded territory. Kogge stone adder is adder which is having low delay.The schematic of Kogge stone adder is shown in the figure 5.

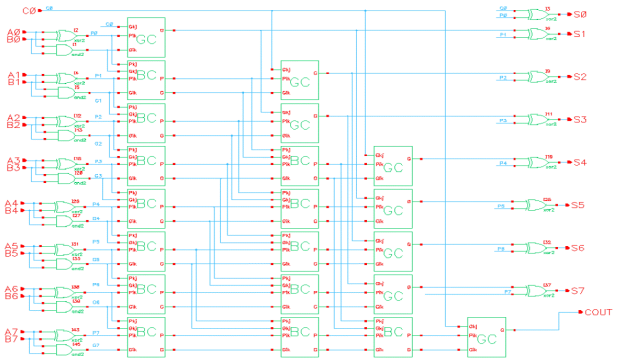

**Fig.5** Kogge Stone Adder

## III. MULTIPLIERS

The most basic type of the increase comprises of joining two numbers, the multiplier and the multiplicand, to shape the last item. The essential augmentation can be accomplished through the conventional paper and pencil technique, disentangled to radix 2.'

**A.Multiplication Algorithm**

From the above dialog it very well may be reasoned that the augmentation of two paired numbers has now changed in to the expansion of two twofold numbers. Considering this the increase of two double numbers might be detailed as pursues,

i) If the Least Significant Bit of the multiplier is '1', the aggregator (at first set as '0') is included with the multiplicand.

ii) Shift the multiplier and aggregator one piece to one side.

iii) If the Least Significant Bit of the multiplier is '0', at that point just move the multiplier and aggregator one piece to one side.

iv) Repeat steps (i) to (iii) till every one of the bits in the multiplier are inspected.

There are two strategies to include the incomplete items produced in the multiplier. To start with, the sequential adder is the one in which the halfway items can be included a sequential way. The other strategy is the one in which the incomplete items are produced in the parallel way and after that additional utilized a few strategies.

**B.Power Optimization in Multipliers**

Power decrease in multipliers [11],[12] should be possible at all plan levels beginning from the innovation level to the framework level. In the multipliers, the incomplete item age, decrease and last stages are structured as a combinational plan. They have a huge plan with high entryway thickness, in certainty high transistor thickness. Clearly this huge dynamic region gives space to have extensive power utilization. In the combinational structure, the exchanging movement chooses the power scattering[22]. Consequently, the power scattering in the multipliers can be diminished by limiting the exchanging exercises. Another effective methodology is by decreasing the quantity of fractional items created in the multiplier structure and their wiring. Duplication is a fundamental necessity in the present high complex processors. Parallel increase is performed by a two-level activity, the age of the halfway items and their collection. In marked duplication, one methodology is to speak to the negative numbers in the sign and size structure. In this methodology duplicating the sign piece with whatever remains of the numbers needs unique thought and treatment. Though in the move and include calculations the negative numbers are spoken to in the two's supplement structure and the two-level task is finished.

**C. Vedic multiplier**

The utilization of Vedic science [13], [14] lies in the way that it decreases the normal counts in customary arithmetic to straightforward ones. This is so because the Vedic formulae are professed to be founded on the regular standards on which the human personality works. Vedic Mathematics is a philosophy of number juggling decides that permit progressively effective speed usage.

This is a fascinating field and introduces some compelling calculations which can be connected to different parts of building, for example, registering. Vedic science depends on 16 Sutras (or axioms) managing different parts of math like number juggling, variable based math, geometry etc. These sutras are intended for quicker mental computation. These Sutras alongside their short implications are enrolled underneath in order. These strategies and thoughts can be straightforwardly connected to trigonometry, plain and circular geometry, conics, analytics (both differential and necessary) and connected science of different sorts. The schematic of 4-bit Vedic multiplier is shown in figure 6.

The conventional Vedic multiplier were synthesized by the RTL compiler incorporating 180 nm,90 nm and 45 nm technology. In this the multiplier architecture and the transistor implementations were generated by the synthesis tool.

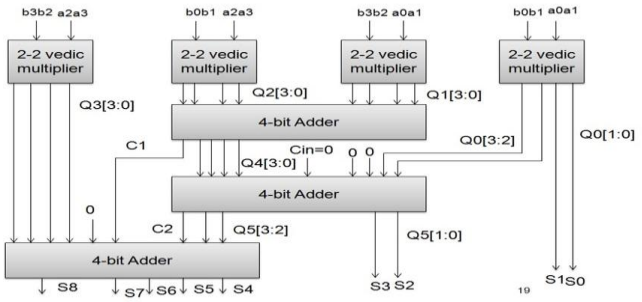


**Fig. 6** Schematic of 4-bit Vedic multiplier**.**

## IV. PROPOSED HYBRID VEDIC MULTIPLIER

The multipliers [15] are the core of any fast-computational gadgets. In the multiplier circuits, the measure of the multiplier chooses the quantity of adders being utilized. Consequently, the power utilization relies upon the quantity of adder squares utilized and the methodology pursued to interface the adder squares to play out the increase activity. Since all the constant applications utilize the multipliers as their center component, the multipliers are the significant power devouring squares. Ordinarily bigger squares are constructed utilizing different littler squares and power streamlining is centered around these littler squares. The proposed hybrid Vedic multiplier, the 4-bit adder is replaced by Kogge stone adder and results are analyzed.

Then the proposed multiplier design was synthesized using the same technology and compared with the designs synthesized by the tool. The comparisons are made in terms of area, delay and power.

## V. RESULTS

The five different types of adders are compared in terms of area,power,delay and power delay product. It is seen that the Kogge stone adder is considered as the fastest adder though there is an increase in area. The energy for this adder(Power delay product) is also considered to be the lowest among the five adders which is compared. The simulation results of five different adders for 4-,8-,16- bit adders are shown in the following tables.

**Table 1**Different 4-bit adders comparison based on 45nm technology.

| Adders | 45nm | | | |
|---|---|---|---|---|
| | Area | Power (nW) | Delay (nS) | PDP |
| Carry skip | 7 | 2152.8 | 953 | 2051618.4 |
| Carry save | 8 | 2283.5 | 979 | 2235546.5 |
| Carry lookahead | 15 | 2415.23 | 735 | 1775194.05 |
| Carry select | 17 | 3120.4 | 987 | 3079834.8 |
| Kogge stone | 14 | 1936.38 | 606 | 1173446.28 |

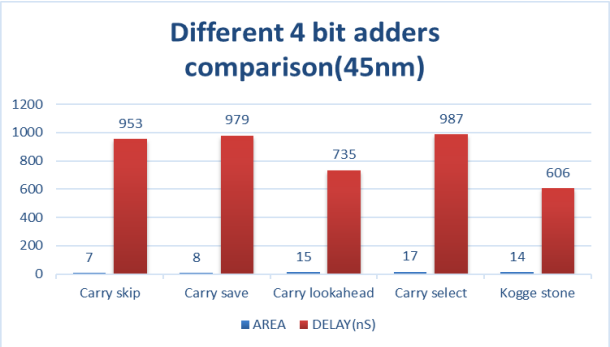


**Fig.7** Graphical representation of area and delay of different 4-bit adders(45nm)

**Table 2** Different 4-bit adders comparison based on 90nm technology.

| Adders | 90nm | | | |
|---|---|---|---|---|
| | Area | Power (nW) | Delay (nS) | PDP |
| Carry skip | 79 | 5431.7 | 1132 | 6148684.4 |
| Carry save | 142 | 5549.1 | 1170 | 6492447 |
| Carry lookahead | 119 | 4920.17 | 802 | 3945976.34 |
| Carry select | 174 | 6214.9 | 1164 | 7234143.6 |
| Kogge stone | 117 | 3710.15 | 705 | 2615655.75 |

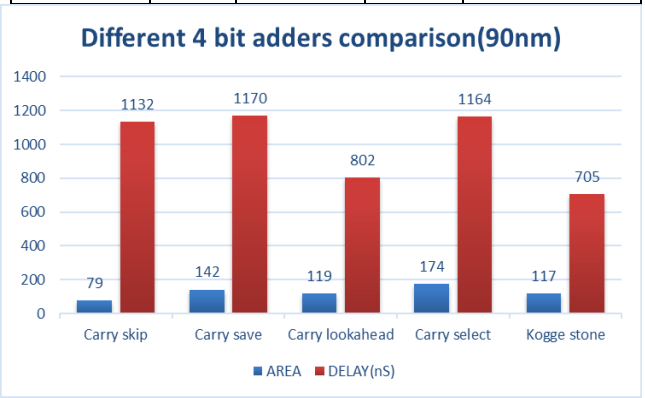


**Fig.8**Graphical representation of area and delay of different 4-bit adders(90nm)

**Table 3** Different 4-bit adders comparison based on 180nm technology

| Adders | 90nm | | | |
|---|---|---|---|---|
| | Area | Power (nW) | Delay (nS) | PDP |
| Carry skip | 369 | 15668.51 | 4417 | 69207786.6 |
| Carry save | 802 | 38386.15 | 1695 | 65064520.9 |
| Carry lookahead | 389 | 16926.73 | 3226 | 54605637.4 |
| Carry select | 602 | 28020.38 | 1510 | 42310767.8 |
| Kogge stone | 807 | 33277.94 | 1063 | 35374449.2 |

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**Fig.9**Graphical representation of area and delay of different 4-bit adders(180nm)

Table 1 to 3 shows the comparison different 4-bit adders based on 45nm,90nm and 180 nm technology. The simulation is performed in Cadence and results portrayed though there is an increase in area, the power and delay has been drastically reduced. Thus, the energy consumption by this Kogge stone adder is considerably reduced. Figure 7-9 shows the graphical representation of area and delay comparison of different 4-bit adders in 45nm,90nm and 180nm technologies.

**Table 4** Different 8-bit adders comparison based on 45nm technology.

| Adders | 45nm | | | |
|---|---|---|---|---|
| | Area | Power (nW) | Delay (nS) | PDP |
| Carry skip | 15 | 5420.732 | 1543 | 8364189.476 |
| Carry save | 21 | 4751.284 | 1102 | 5235914.968 |
| Carry lookahead | 22 | 3919.923 | 1524 | 5973962.652 |
| Carry select | 18 | 7370.279 | 1069 | 7878828.251 |
| Kogge stone | 42 | 5149.207 | 728 | 3748622.696 |

**Fig.10**Graphical representation of area and delay of different 8-bit adders(45nm)

**Table 5** Different 8-bit adders comparison based on 90nm technology.

| Adders | 90nm | | | |
|---|---|---|---|---|
| | Area | Power (nW) | Delay (nS) | PDP |
| Carry skip | 170 | 7070.337 | 2012 | 14225518 |
| Carry save | 253 | 11561.51 | 1282 | 14821852 |
| Carry lookahead | 189 | 7851.108 | 1581 | 12412601.7 |
| Carry select | 248 | 10903.48 | 1340 | 14610664.5 |
| Kogge stone | 316 | 13025.58 | 876 | 11410409.8 |

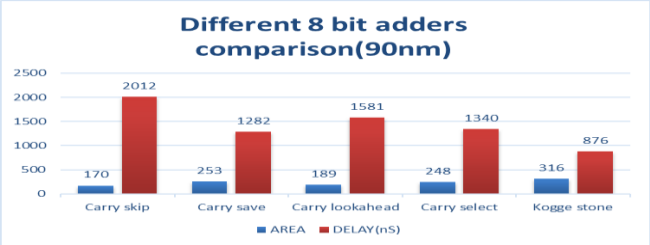


**Fig.11**Graphical representation of area and delay of different 8-bit adders(90nm)

**Table 6** Different 8-bit adders comparison based on 180nm technology.

| Adders | 180nm | | | |
|---|---|---|---|---|
| | Area | Power (nW) | Delay (nS) | PDP |
| Carry skip | 279 | 40384 | 1593 | 64331712 |
| Carry save | 492 | 42195 | 1612 | 68018340 |
| Carry lookahead | 356 | 17294 | 1144 | 19784336 |
| Carry select | 619 | 42357 | 1564 | 66246348 |
| Kogge stone | 353 | 16008.5 | 1096 | 17545316 |

**Fig.12**Graphical representation of area and delay of different 8-bit adders(180nm)

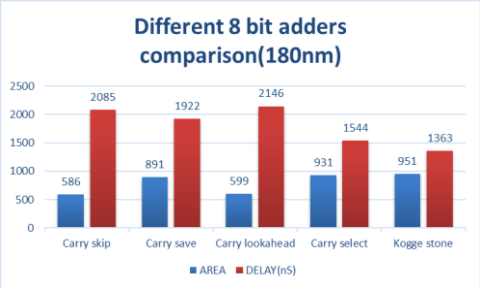


Table 4 to 6 shows the comparison of different 8-bit adders using 45nm,90nm and 180 nm technology. As the number of input bit increases the area increases which in turn increase the dynamic power of the adder. So, there is a slight increase in the total power. Since Kogge stone is the fastest adder, the delay is very low when compared to other adders. Thus, the overall energy consumed by this adder is also very low.Figure 10-12 shows the graphical representation of area and delay comparison of different 8-bit adders in 45nm,90nm and 180nm technologies.

**Table 7** Different 16-bit adders comparison based on 45nm technology.

| Adders | 45nm | | | |
|---|---|---|---|---|
| | Area | Power (nW) | Delay (nS) | PDP |
| Carry skip | 37 | 12316.81 | 3190 | 39290630.28 |
| Carry save | 168 | 28716.24 | 1334 | 38307469.5 |
| Carry lookahead | 162 | 16665.77 | 1546 | 25765281.97 |
| Carry select | 46 | 19267.13 | 1122 | 21617714.25 |
| Kogge stone | 114 | 13537.56 | 894 | 12102580.43 |

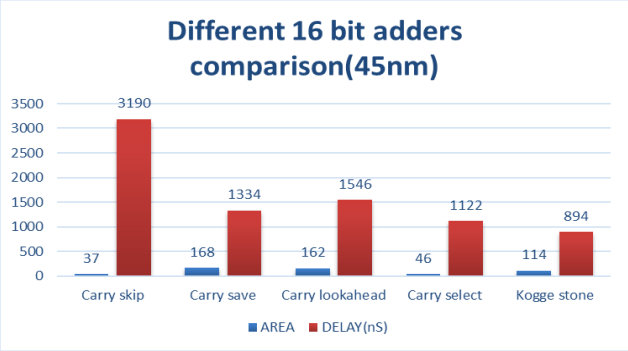


**Fig.13**Graphical representation of area and delay of different 16-bit adders(45nm)

**Table 8** Different 16-bit adders comparison based on 90nm technology.

| Adders | 180nm | | | |
|---|---|---|---|---|
| | Area | Power (nW) | Delay (nS) | PDP |
| Carry skip | 586 | 34915.22 | 2085 | 72798232 |
| Carry save | 891 | 38702.38 | 1922 | 74385971 |
| Carry lookahead | 599 | 35006.44 | 2146 | 75123827 |
| Carry select | 931 | 51328.77 | 1544 | 79251619 |
| Kogge stone | 951 | 45980.64 | 1363 | 62671614 |

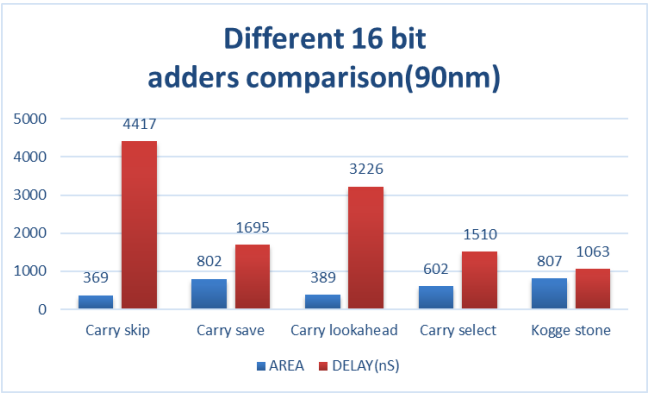


**Fig.14**Graphical representation of area and delay of different 16-bit adders(90nm)

**Table 9** Different 16-bit adders comparison based on 180nm technology.

| Adders | 180nm | | | |
|---|---|---|---|---|
| | Area | Power (nW) | Delay (nS) | PDP |
| Carry skip | 586 | 34915.22 | 2085 | 72798232 |
| Carry save | 891 | 38702.38 | 1922 | 74385971 |
| Carry lookahead | 599 | 35006.44 | 2146 | 75123827 |
| Carry select | 931 | 51328.77 | 1544 | 79251619 |
| Kogge stone | 951 | 45980.64 | 1363 | 62671614 |

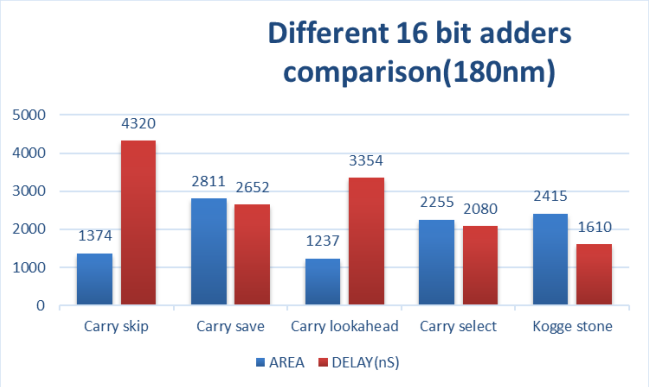


**Fig.15**Graphical representation of area and delay of different 16-bit adders(180nm)

Table 7 to 9 shows the comparison of different 16-bit adders using 45nm,90nm and 180 nm technology. As for the faster operation of the circuits, the delay of the adder used in the circuits should be low. The power delay product and delay of Kogge stone adder is the least when compared with the other four adders. So, this adder is utilized in Vedic multiplier for faster operationFigure 13-15 shows the graphical representation of area and delay comparison of different 16-bit adders in 45nm,90nm and 180nm technologies.

. **Table 10** Comparison of 4-bit Vedic multiplier with Proposed hybrid multiplier based on 45nm,90nm and 180nm technology

| | 45nm | | | |
|---|---|---|---|---|
| 4-bit | Area | Power (nW) | Delay(nS) | PDP |
| Vedic | 36 | 4480.007 | 1907 | 8543373.35 |
| proposed | 63 | 5092 | 1613 | 8213396 |
| | 90nm | | | |
| Vedic | 368 | 11613.898 | 2537 | 29464459.2 |
| proposed | 483 | 12171.823 | 2201 | 26790182.4 |
| | 180nm | | | |
| Vedic | 1259 | 51477.913 | 3147 | 162000992.2 |
| proposed | 1457 | 53199.59 | 2954 | 157151588.9 |

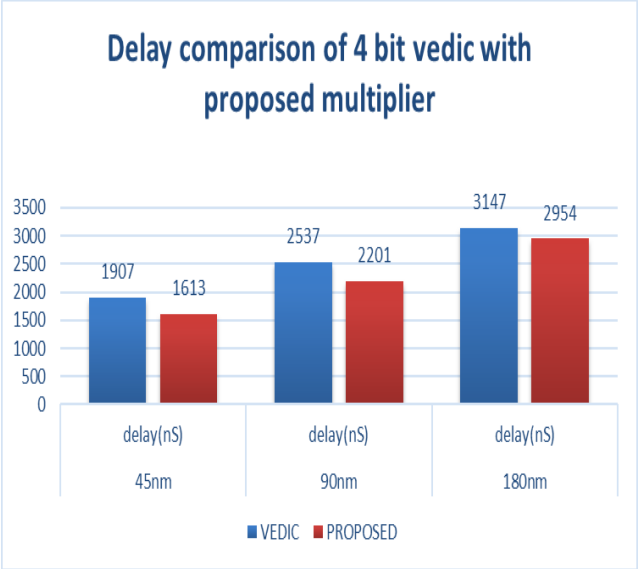


**Fig.16**Graphical representation of delay comparison of 4-bit Vedic multiplier with proposed multiplier

**Table 11** Comparison of 8-bit Vedic multiplier with Proposed hybrid multiplier based on 45nm,90nm and 180nm technology

| | 45nm | | | |
|---|---|---|---|---|
| 8-bit | Area | Power (nW) | Delay(nS) | PDP |
| Vedic | 268 | 36674.89 | 3826 | 140318137 |
| proposed | 284 | 37020 | 3467 | 128348340 |
| | 90nm | | | |
| Vedic | 1846 | 73575.366 | 4192 | 308427934 |
| proposed | 1907 | 79769.47 | 3663 | 292195569 |
| | 180nm | | | |
| Vedic | 5578 | 378887.01 | 5754 | 2180115827 |
| proposed | 6192 | 395074.34 | 4213 | 1664448211 |

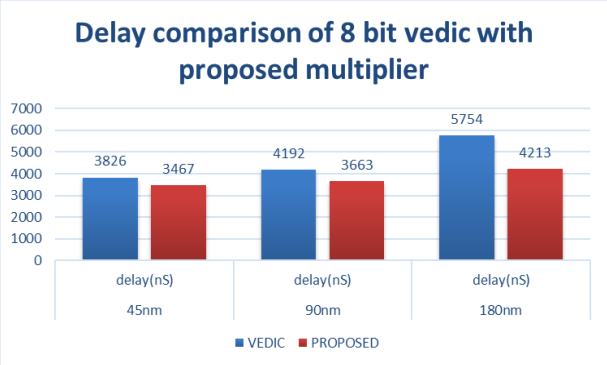


**Figure 17** Graphical representation of delay comparison of 8-bit Vedic multiplier with proposed multiplier

**Table 12** Comparison of 16-bit Vedic multiplier with Proposed hybrid multiplier based on 45nm,90nm and 180nm technology

| | 45nm | | | |
|---|---|---|---|---|
| 16-bit | Area | Power (nW) | Delay(nS) | PDP |
| Vedic | 384 | 27549.07 | 5404 | 148875185 |
| proposed | 396 | 28620.85 | 4938 | 141329733 |
| | 90nm | | | |
| Vedic | 2713 | 470913.4 | 5536 | 2606976605 |
| proposed | 2886 | 493046.65 | 5166 | 2547078989 |
| | 180nm | | | |
| Vedic | 8090 | 529624.99 | 6556 | 3472221428 |
| proposed | 8876 | 533508.53 | 5398 | 2879879034 |

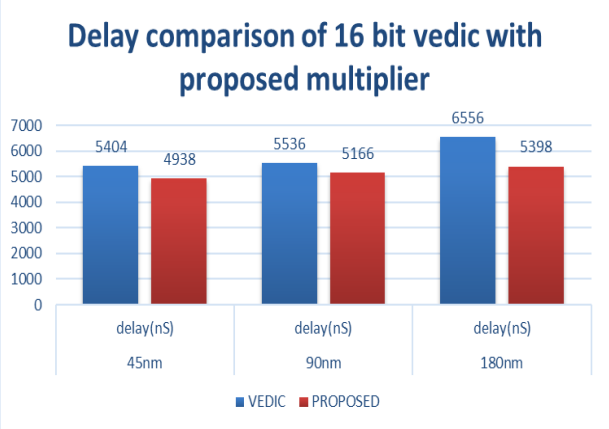


**Figure 18** Graphical representation of delay comparison of 16-bit Vedic multiplier with proposed multiplier

Table 10 to 12 shows the comparison of 4-,8- and 16- bit Vedic multiplier with the proposed hybrid Vedic multiplier for 45nm,90nm and 180nm technology. The proposed multiplier is faster when compared to the existing Vedic multiplier. The energy of the proposed multiplier is also proved to be noteworthy. Figure 16-18 shows the graphical representation of delay comparison of existing with proposed multiplier based on 45nm,90nm and 180nm technology.

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