Optimization of Multiplier Design in FIR Filters

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Abstract: ***To optimize the performance of transmitter and receiver circuits in communication, FIR filters play major role in many areas such as noise suppression, bandwidth selection and so on. During the realization of digital FIR filters, multipliers play a major role in processing digital signals. Performance of many arithmetic problems mainly depends on the speed at which a multiplication operation can be performed. So by changing the method of acquisition of partial products can produce change in speed, time and usage of area. From the study, multiplier design with Wallace tree structure is efficient at higher orders in comparison with array multiplier in both power and speed. Replacing array multiplier by Wallace tree multiplier in digital FIR filter contributes towards the attributes of VLSI DESIGN. The FIR filter with Multiplier functionality checking was done in MODELSIM and synthesis is done in Xilinx ISE.***

Index Terms: Array multiplier, Wallace Tree multiplier, FIR filter, ModelSim, Xilinx ISE.

I. INTRODUCTION

According to the motto of VLSI, each and every circuit that is of industrial use must be smaller, cheaper and faster. In order to achieve this, attributes of VLSI such as area, cost power and speed play a major part. VLSI generally means integrating number of complex circuits on a single chip. Along with the attributes of VLSI quality metrics too play a major part. They are cost, performance, functionality and robustness. One of the most important arithmetic operations is multiplication. It is performed by multiplier which outputs the result by repetitive addition. Repetitive addition involves more number of adders which results in increase in area, time and also power dissipation. This multiplier plays an important role in digital filtering processes. So it is necessary to optimize multiplying techniques to enhance the attributes of VLSI.

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II. DIGITAL FILTERS

Digital signal processing has numerous applications in the field of communication such as audio and video. Digital filtering is very much essential in bandwidth selection, noise reduction. These applications are very much based on the linear time invariant (LTI) systems. Digital filters are generally classified based on the impulse response of the system. They are Infinite Impulse Response (IIR) filter and Finite Impulse Response (FIR) filter. For linear phase applications FIR filter is more suited than IIR filter, because of the linear phase characteristics possessed by FIR filters. FIR filters are always stable because they are non-recursive in nature. FIR filter can be realized in two ways. But most commonly used are Direct form and Cascade form. Direct form is the most basic form of realization.

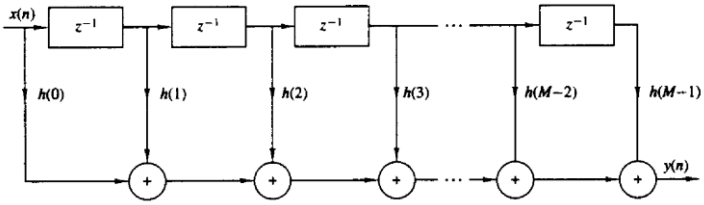

Fig 2.1 FIR Filter – Direct Form realization

FIR filter is expressed as $y(n) = \sum_{k=0}^{M-1} h(k)x(n-k)$
x(n) - input sequence
y(n) - output sequence
h(k) – coefficient of the filter

III. COMPONENTS OF FIR FILTER

From the above equation, the following components are required to design the FIR filter.

1) **Adder:** It is used to add the mutliplied version of the present and past input.
2) **Multiplier:** Multiplier is used to multiply the input signal and the coefficient. Array Multiplier and Wallace Tree multiplier can be used.
3) **Delay Element:** It is used to delay the input signal to get past vlues of the input sequence according to the clock cycle.D Flip flop is used as delay element.

IV. EXISTING SYSTEM

One of the important components of the FIR filter is Multiplier. Multiplier plays a major role in the timing constraint of the filter. By optimizing the partial product accumulation of the multiplier, timing metrics can be enhanced. Normally the FIR filter is realized by using array multiplier.

A. Design of Array Multiplier

Array multiplier operation is very much similar to the manual procedure for accumulating the partial products. The name array multiplier depicts that the number of adders used forms an array.

Generally a multiplier has two inputs, one input with X bits long and another input with Y bits long. Since this multiplication technique is more analogous to the manual generation of partial products, it requires Y × X two bit AND gates are required for generating Y partial products.

This Multiplier makes use of Y – 1 X-bit adders for adding the Y partial products which takes most of the area. A simple routing mechanism is sufficient for the proper alignment of the partial products.

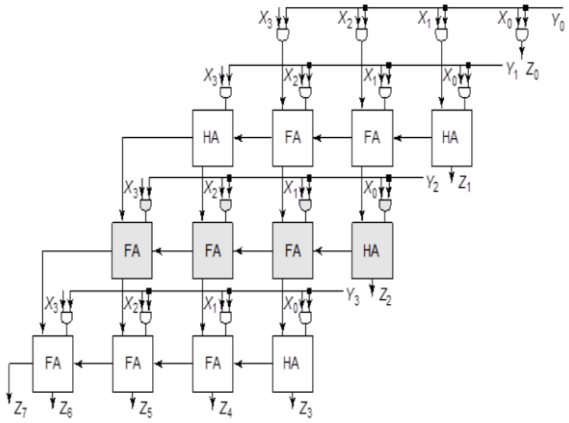

Fig 4.1 Structure of Array Multiplier

B. Design of FIR Filter with Array Multiplier

The designed array multiplier is being incorporated in the FIR filter realization. The incorporation of array multiplier is shown below.

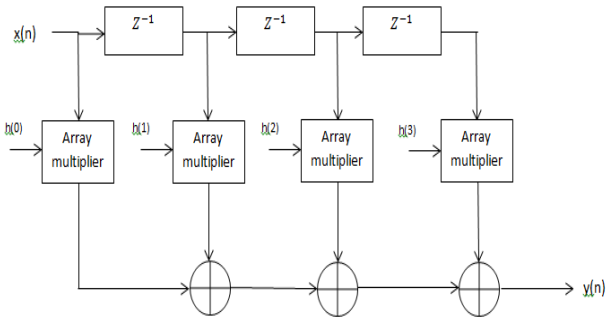

Fig 4.2 FIR Filter Structure with Array Multiplier

The above FIR filter with array multiplier is designed with the help of VHDL language which comprises of several modules and checked for its functionality in *MODELSIM* and synthesized in *XILINX ISE* with the target device as SPARTAN3E for generating reports. From the timing report the time required to get the output which is known as the delay time is found to be **4.04ns f**or **3 tap fourth order FIR filter**.

V. PROPOSED SYSTEM

To optimize the timing constraints from the existing system, several multiplying algorithms can be used. Here Wallace Tree Structure is being employed. The main use of Wallace tree structure is that, the number of adders required for the partial product accumulation is very much less in comparison with the Array Multiplier. Since the adders take much of the area in the multiplier, this structure helps in reducing the area because of lesser number of adders being used. However this structure becomes more efficient in higher orders of multiplication.

A. Design of Wallace Tree Structure

The main aim of the Wallace tree structure is to optimize the area by reducing the number of adders required to obtain the output of the multiplier. The partial product generation in this structure is similar to that of the array multiplier but the accumulation of partial products is different. The accumulation of partial products is initially done by inverting certain number of partial products to make a tree like structure which is shown in figure 5.1(b). Three half adders and three full adders are used up to the second stage of the structure which can be inferred from the figure 5.1.

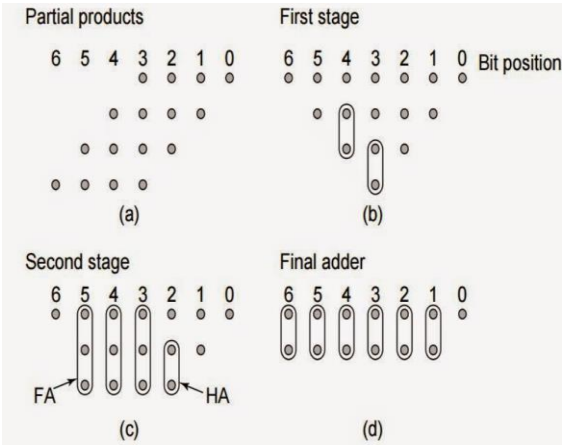

Fig 5.1 Formation of Wallace tree structure

Final addition is the last stage of the Multiplier. In this stage, any type of adder can be used based on the accumulation array.

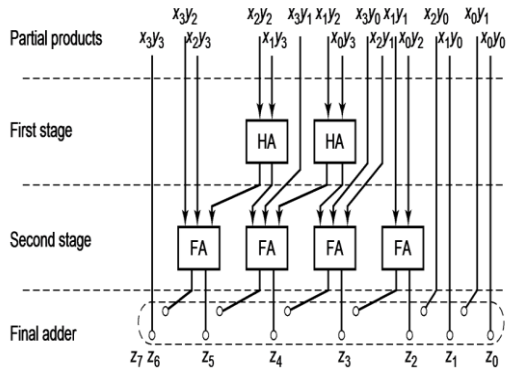

Fig 5.2 Four bit Wallace tree Multiplier

B. Design of FIR Filter with Wallace Tree Multiplier

The Wallace tree multiplier designed based on the above stages is incorporated in the FIR filter. The implemented structure is shown below.

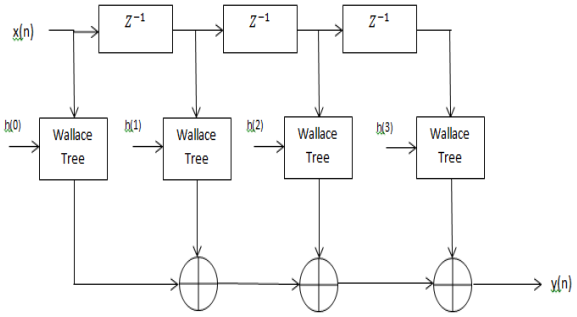

Fig 5.3 FIR filter structure with Wallace tree Multiplier

The above structure is designed using VHDL language with various modules interconnected with each other. The target device is same as that of the previous design. From the synthesis report obtained from XILINX ISE , the delay of the output is found to be **3.492** ns for the same **3 tap fourth order FIR filter**.

VI. Simulation Results

Simulation and synthesis are necessary to check the correct functionality of any system before Implementation.

A. Functionality of Multipliers

The functionality of both the multipliers is checked with the help of MODELSIM tool and the results are shown below.

a. Array Multiplier

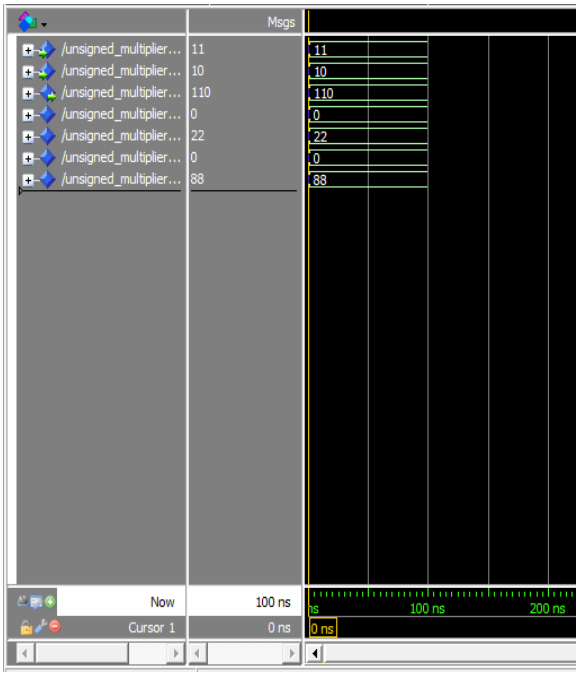

Fig 6.1 Functionality check of Array Multiplier

b. Wallace tree Multiplier

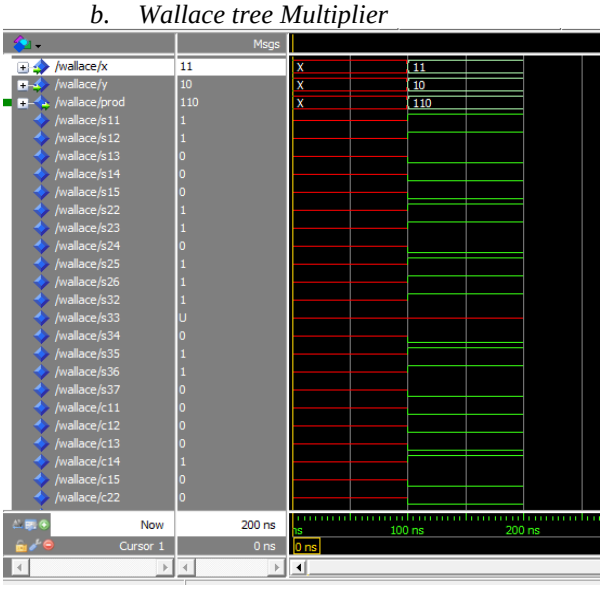

Fig. 6.2 Functionality check of Wallace Tree Multiplier

B. Functionality of FIR Filter with Multipliers

a. FIR filter with Array multiplier

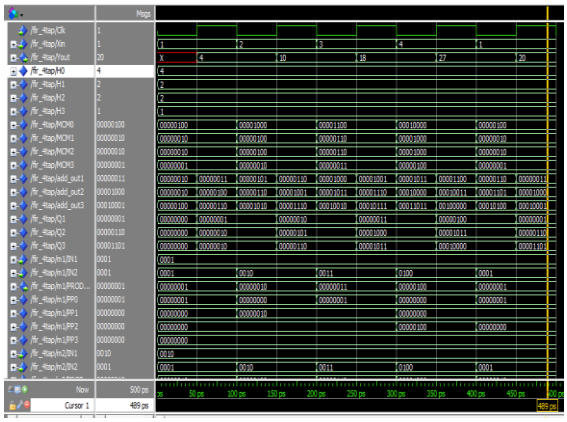

Fig 6.3 Functionality check of FIR filter with array multiplier

b. FIR filter with Wallace Tree Multiplier

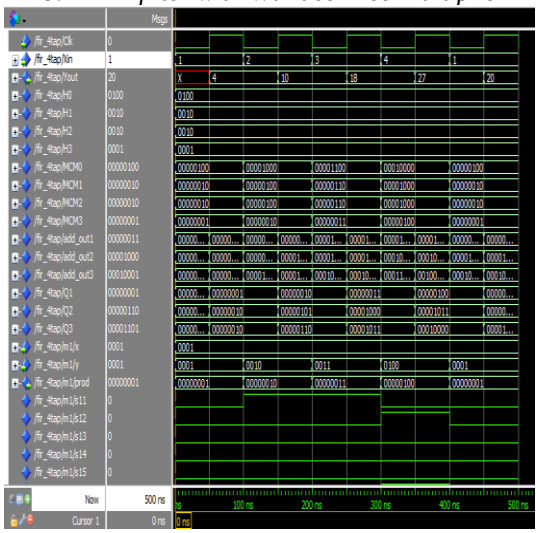

Fig 6.4 Functionality check of FIR filter with Wallace tree multiplier

C. Comparision of Synthesis results

Comparisons of the synthesis results between the two multipliers along with their respective FIR filter structures are necessary to understand the degree of optimization.

Comparison of the timing details of the multipliers are shown in the table below

Tap	Timing details	
	Array multiplier	***Wallace tree multiplier***
3	2.95ns	2.78ns

Table 1

From the above table, the delay time is very much close to each other. It is due to the smaller order (4^{th} order) of the multiplier being used.

Comparison of the timing details of FIR Filters are shown in the table below.

Tap	Timing details	
	FIR filter with Array multiplier	*FIR filter with Wallace tree multiplier*
3	4.04ns	3.492ns

Table 2

It is concluded from these tables that the FIR filter with Wallace tree structure uses minimum resources for efficient operation when compared to FIR filter with Array Multiplier.

VII. CONCLUSION

Even though Wallace tree multiplier uses minimum resources for implementation, realization of this multiplier is bit complex for lower orders. This is where the real challenge lies.

Since the design was developed in 90nm technology. The future scope of this study can be done in a reduced nanotechnology.

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