

Code acquisition and tracking of IRNSS signals

Anirudh Lanka, Aishwarya Shivani R., Amoolya R. Bayari, Suresh Dakkumalla, Shylashree N.

Abstract--- Navigation using the Indian Regional Navigation Satellite System (IRNSS) requires processing of the lowest raw data received from the corresponding satellites. The acquired Radio Frequency signal is subjected to a software based IRNSS receiver consisting of a Numerically Controlled Oscillator to convert from Radio Frequency Range to Intermediate Frequency Range for further processing. The converted signal is then subjected to various algorithms for achieving Code Acquisition, Locking and Tracking to complete the navigation. This paper discusses about building a software based IRNSS receiver to simulate the navigation behavior in real time. All the simulation codes are written in VHDL and in accordance with the Zynq-706 FPGA board. The simulation manifests that Serial Acquisition consumes the lowest resource, but is time exhausting with 41933 iterations. Whereas the PCPS technique requires only 41 (or 1023 for PFSS) iterations but uses higher order DSP processors.

Keywords— Code acquisition, Code tracking, carrier tracking, Parallel Frequency Space Search, Parallel Code Phase Search, Phase Locked Loop, Delay Locked Loop, Frequency Locked Loop

I. INTRODUCTION

With the objective of providing accurate position, navigation and timing throughout India, Indian Space Research Organization (ISRO) is developing Indian Regional Navigation Satellite System (IRNSS), with an operational name NavIC. It extends up to 1,500 km across the boundaries of India and comprises of 7. Transmission of navigation signals takes place through CDMA on L5 signal using BPSK modulation. The IRNSS offers two kinds of services – Standard Positioning Service (SPS) and Restricted/Authorized Service (RS) at L5 band (1176.45MHz) and S-band (2472.5 MHz) frequencies respectively. [1]

The IRNSS System is composed of three segments: space segment, ground segment and user segment. The ground segment is in charge of operation of IRNSS and maintenance. Operational responsibilities include supervision of constellation status, uploading of navigation data and modification of orbital parameters. The space segment consists of 7 satellites in which 3 are geostationary orbits and 4 are geosynchronous orbits. The geostationary satellites are located at 83°E, 32.5°E and 131°E and the geosynchronous satellites have longitude crossings of

111.75°E and 55°E. The user segment consists of various types of receivers capable of receiving L5 band and S-band frequencies.

There are typically two stages – code acquisition and code tracking in the code synchronization task.

Code acquisition is a process of searching for satellite signal through an uncertainty region until a correct code phase delay and Doppler frequency is found. The intention of performing acquisition is to detect and match the visible satellites with a locally generated replica to provide the values of matched carrier and code phase of satellite signals. [2, 4, 5] Code tracking is a process of keeping a trace of the code and carrier phase of a specific code. The purpose of tracking is to minimize the estimation error of delay between the received signal and the signal generated at the receiver. This delay estimation is obtained from the acquisition stage. [3, 5]

II. SIGNAL STRUCTURE

A. Transmitter

Signals are transmitted by the IRNSS satellites on two carrier frequencies called as L5 (1176.45 MHz) and S-band (2472.5 MHz) frequencies. The navigation information is transmitted as DSSS which is modulated by a unique PRN sequence belonging to the family of C/A codes of Gold sequence with 1023 bits. Each of these PRN codes is transmitted with the same carrier frequencies through CDMA scheme. [6]

With an intention of detecting and tracking a specific satellite, CDMA scheme should be used to find out the C/A code phase and Doppler frequency shift from the L5 carrier of a specific satellite so that a replica of PRN sequence and carrier wave can be generated at the receiver with the identified code phase and Doppler shift to bring down the desired navigation message to baseband. [7, 8] It is evident from Fig. 1 that the resulting L5 and S-band signals are generated from the same atomic clock with a reference frequency $f_o = 10.23$ MHz. This reference atomic clock provides timing to every other signal generator block in the system. The L5 signal is the resultant of the addition of bitwise XOR operation between C/A code and navigation and bitwise operation between Precision code (P) and navigation message. After their addition, they are modulated into BPSK onto the L5 carrier having a 90° phase offset between them.

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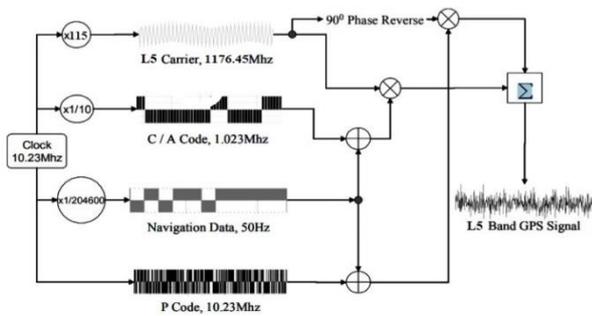


Fig. 1: IRNSS Transmitter

Fig. 1 depicts that the resulting L5 and S-band signals are generated from the same atomic clock with a reference frequency $f_0 = 10.23$ MHz. This reference atomic clock provides timing to every other signal generator block in the system. The L5 signal is the resultant of the addition of bitwise XOR operation between C/A code and navigation and bitwise operation between Precision code (P) and navigation message. After their addition, they are modulated into Binary Phase-Shift Keying (BPSK) onto the L5 carrier having a 90 degrees phase offset between them. [9]

B. Down Sampling

The initial step of the receiver takes place in the front-end section is to down-sample the Radio Frequency signal to Intermediate Frequency signal as depicted in Fig. 2. It is done because the L5 carrier frequency (1176.45 MHz) is out of range to handle most of the electronic components. Therefore, the RF signal should be down-converted to IF before processing through the receiver. The digital receiver also uses the narrow front-end system bandwidth to improve the performance. [2, 10]

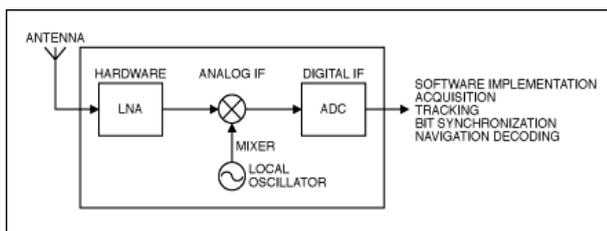


Fig. 2: Down conversion from RF signal to IF signal

III. COMPONENTS

A. PRN Code

The spreading sequences used in IRNSS system belonging to a unique family of PRN code are called as Gold codes. Every PRN code that is transmitted by a satellite is a product obtained from the modulo-2 addition of two maximum length sequences having a length $N = 2^n - 1$ (in case of IRNSS, $n = 10$, and $N = 1023$). [11-13] The C/A code has a chip rate of 1.023 MHz and is a bi-phase modulated signal. Each chip is 977 ns (1/1.023 MHz) long.

B. Numerically Controlled Oscillator (NCO)

NCO is a digital signal generator used to generate address into sine lookup table. It is a digital equivalent of Analog VCO. Based on the input phase word, the output frequency changes. The input phase word determines the output frequency of NCO. There are two kinds of NCO used:

The carrier NCO is used to generate complex sine and cosine signals whose frequency can be modified. Its primary purpose is to eliminate components from the IF carrier and strip away the Doppler frequency. The frequency control word or the phase word is an input that corresponds to the frequency to be generated. It utilizes the look-up table which is an easier and a faster way to realize carrier NCO. The look-up table utilizes the phase angle as an address to store the sine and cos values. The phase word is an input to the phase accumulator and as the accumulator receives the phase words, it drives a clock to start tabulating. Once the counted value becomes equivalent to the phase word value, it is added to the phase adder along with the initial phase. The phase accumulator and phase word are implemented using word length $N = 30$ while the address of the look-up table is 3 bits long. A clock frequency of 1.26 MHz is used to drive the carrier NCO. The number of bits J is determined for sine and cos outputs. A phase plane of 360° is divided into $2^J = K$ (in this case $J = 3$, thus $K = 8$) phase points. For every waveform, K values are calculated assigning one value per phase point. Each value represents an amplitude corresponding to a particular phase point. The rate at which the phase point traverses depends on the output frequency. Only the upper J bits of the holding register are used to access the address of waveform amplitude. The carrier NCO generates two output signals i.e. in-phase component (I-phase) and quadrature phase component (Q-phase).

The code NCO is used to generate a clock signal that is utilized to drive the C/A code. The code NCO design is similar to that of carrier NCO. It is driven by a clock whose frequency is 1.023 MHz. The frequency phase word is an input to the phase accumulator whose length $N = 26$ bits. The output of code NCO is the overflowing bit of the phase accumulator that is the 26th bit of the accumulator.

C. Correlator And Detection

The correlator constitutes the most important function of detection and demodulation in the receiver. The digital correlator consists of accumulate and dump in which the signals are multiplied and accumulated. After the multiplication of I and Q components with the PRN code, the signals are sent to the correlator to perform convolution, multiplication and squaring. The maximum index of the Accumulate and Dump block is 1023. The Accumulate & Dump performs averaging over one chip rate (adding 1023 values). The average can be positive or negative, but the energy structure after averaging is same as that of I and Q signals. In order to get the energy in absolute value, squaring operation is performed called as enveloping.

IV. SIGNAL ACQUISITION

A. Serial Search

One of the simplest algorithms in the CDMA system used for acquisition is the serial search acquisition. It is one of the classical methods in which the receiver serially searches for the code phase delay within the whole Doppler frequency range. Serial correlation refers to the similarity of the



incoming signal with the locally generated signal at the receiver. The primary objective of acquisition is to establish satellite visibility and find the values of carrier Doppler frequency and code phase of the satellite signals. The satellites in the space differ from each other by 32 PRN sequences. [14, 15] It is requisite to know the code offset and Doppler frequency to generate the replica at the receiver. Only when the incoming signal is aligned perfectly with locally generated replica, it is possible to eliminate the incoming code. The line-of-sight velocity of velocity of satellite is the reason for the Doppler Effect which results in lower or higher frequencies. This frequency may vary as much by ± 10 KHz. Knowing this Doppler frequency is however very crucial to generate a replica at the receiver. This signal can wipe away the incoming carrier from the signal. Firstly, the local oscillator generated two signals I-phase (I-phase) and Quadrature-phase signals (Q-phase). The Q-phase signal is 90o phase-shifted version of the I-phase signal. Alongside this, the C/A code having a code phase from 0 to 1022 is also generated. [16] The aim of acquisition is to match the Doppler frequency. After the down-conversion of the RF signal to IF signal, the IF signal is multiplied by the I-phase and Q-phase components. Next, a locally generated PRN corresponding to a particular satellite is multiplied to both the components. This is done in order to match with the code delay whose energy is spread over 1023 chips. A sample clock whose frequency 10 MHz is used to drive the entire receiver as shown in Fig. 3. These signals are sent to the correlator to perform the summing and envelope operations. The correlation power is high only if the Doppler frequency and code delay of the incoming signal matches with the locally generated signal at the receiver. The absolute value of the correlation power gives a sharp peak in the detection stage. This peak indicated the correlator output has exceeded the predefined threshold values.

The serial search is performing two kinds of sweeps:

- Frequency sweep
- Code phase sweep

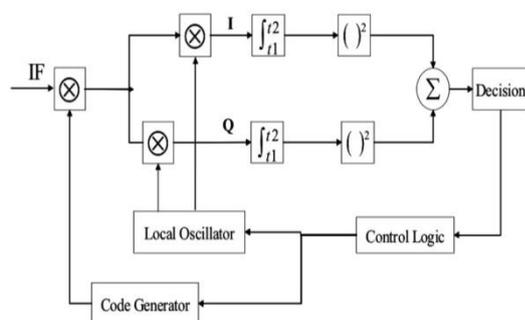


Fig. 3 Serial Acquisition

If the Doppler frequency does not correlate with the locally generated carrier, then all the possible serial search of $IF \pm fD_{max}$ are performed for 500 Hz steps. If the $fD_{max} = 10$ KHz, then receiver performs a serial search among $1023(2 * 10 \text{ KHz} / 500\text{Hz} + 1) = 1023 * 41 = 41943$ combination. On the other hand, if the code phase does not correlate with the locally generated code, then the code phase is incremented by half chip every step which

means serial search for 2046 chips is performed. This process performs for a very large number of combinations. Therefore, it is time consuming and exhausting search process which tends to be the main reason for its drawback.

B. Parallel Frequency Space Search

The first technique of Parallel Acquisition is the Frequency Space Search Acquisition method. As the name suggests, this method involves an FFT, thus parallelizing the shift in Doppler Frequency by ± 500 Hz until ± 10 KHz. Thus, the sole feedback parameter is the Code Phase Delay. Hence, the total number of iterations are only 1023 when compared to 41943 iterations in Serial Search method. The resource utilization and complexity stand intermediate to Serial Search and Parallel Code Phase Acquisition. Fig.4 depicts the schematic and flowchart of Frequency space search acquisition. [8]

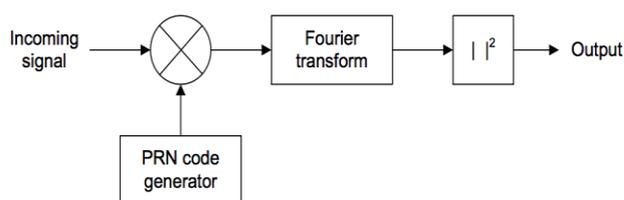


Fig. 4: Parallel Frequency Search Acquisition

C. Parallel Code Phase Search Acquisition

The second method of Parallel Acquisition using parallelization of one of the search parameters is the Parallel Code Phase Search method. This method uses parallelization of the code phase dimension, thus eradicating the delay of half chip after completing a cycle. [2, 7, 17] This method uses the multiplication-convolution duality property to realize this parallelization. The only feedback parameter is the Doppler Shift. In the PCPS algorithm, the incoming C/A code is transformed into frequency domain and multiplied with generated local replica and conjugated C/A code before subjecting for correlation. The output of correlator gives the delay required for locally generated C/A code to match with the IRNSS signal. The number of iterations to be performed are only 42 when compared to Serial Acquisition (which requires 42966 iterations). However, the resource complexity in case of Parallel Code Phase Acquisition is very high when compared to other methods. Fig. 5 provides the block diagram of Parallel Code Phase Acquisition.

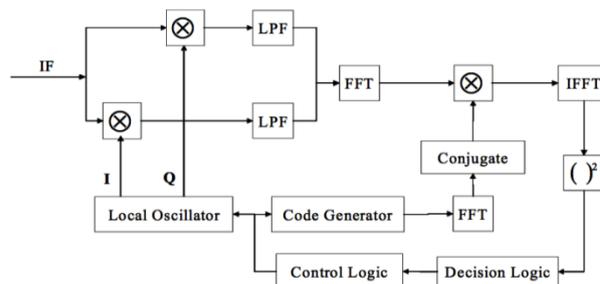


Fig. 5: Parallel Code Phase Search Acquisition

Once we obtain the values of Doppler shift frequency and the code phase from the acquisition stage, these acquired values are sent to the tracking system to keep a track of it and also to extract the navigation data. There are two methods to accomplish tracking namely, carrier and code tracking. Basically, the phase locked loop (PLL) are used tracking to track the carrier and the Delay locked loop (DLL) are used to track the code phase in carrier and code tracking respectively. [8] Fig. 6 provides the general block diagram of the entire tracking process.

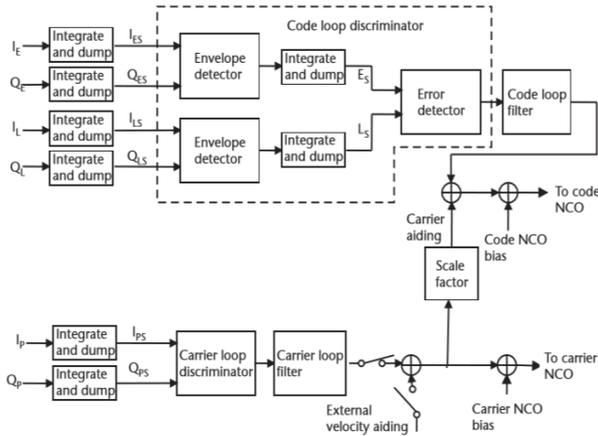


Fig. 6: Tracking System

A. Early-Prompt-Late Codes

Firstly, output signal after the multiplication of the C/A code with the incoming signal is used to generate three code replicas i.e. Early (E), Prompt (P) and Late (L) having a delay of $\pm 1/2$ chip. The original signal that is sampled is the prompt code, while early and late codes are time-shifted versions by half chip or less of the sampled signal. Fig. 7 illustrates the generation of Early, Prompt and Late codes.

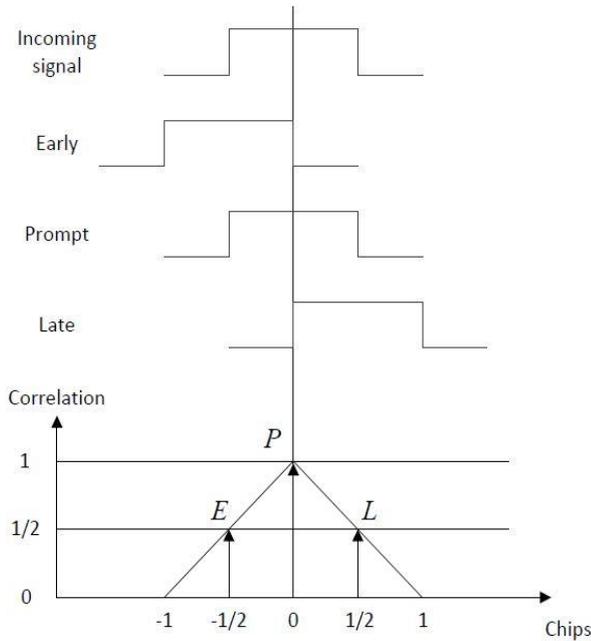


Fig. 7: Generation of Early, Prompt and Late codes

B. Code Tracking

The estimation of the code phase by tracking the code received is the purpose of code tracking. It uses Delay Locked Loop which consists of DLL discriminators and

loop filters to track the code phase. Firstly, the time-shifted codes (Early and Late) are multiplied with the In-Phase and Quadrature-Phase as shown in Fig. 8. These two product signals are accumulated and averaged using a correlator. To estimate the error signal that has to be adjusted with the locally generated replica, the output of correlator is passed onto DLL discriminator. Using a non-coherent DLL discriminator and loop filter using (1), calculates the error signal is calculated that is used as a feedback to adjust with the replica generated. When the error value is zero, then the IRNSS signal is synchronized completely with the locally generated replica.

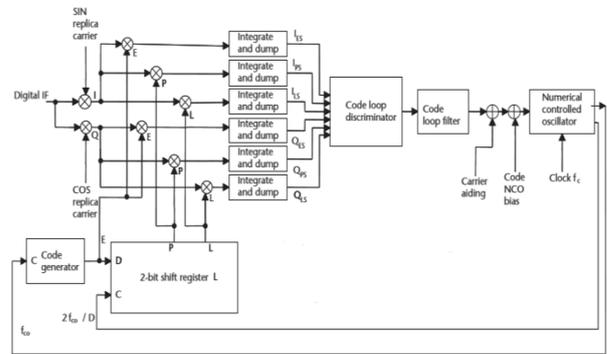


Fig. 8: Code Tracking Loop

$$D = \frac{1 \sqrt{I_{ES}^2 + Q_{ES}^2} - \sqrt{I_{LS}^2 + Q_{LS}^2}}{2 \sqrt{I_{ES}^2 + Q_{ES}^2} + \sqrt{I_{LS}^2 + Q_{LS}^2}} = \frac{1}{2} \frac{(E-L)}{(E+L)} \quad (1)$$

C. Carrier Tracking

In order to demodulate the navigation data, an identical replica has to be generated locally at the receiver. The Phase Locked Loop (PLL) consisting of PLL discriminators and loop filters as depicted in Fig. 9 is utilized to track the carrier frequency.

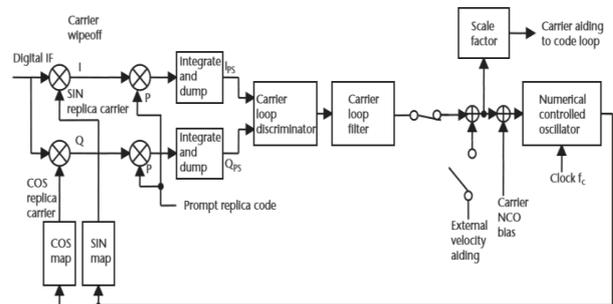


Fig. 9: Carrier Tracking

The phase error is computed by the carrier discriminator and loop filter of locally generated replica.

$$\text{Phase Error} = \tan^{-1} \frac{Q_{PS}}{I_{PS}} \quad (2)$$

The PLL uses active PI second-order filter. The error signal is fed back to the carrier NCO to adjust the frequency by the loop filter.

V. RESULTS

A. Comparison between serial and parallel acquisition

The Serial Search and Parallel Search implementations are identical until the component differentiation, after which Serial Search performs linearly and Parallel Search involves converting into Frequency domain before subjecting for further processing. Taking resource usage into constraint, Parallel Acquisition definitely has higher complexity and hence higher usage when compared to serial acquisition due to the involvement of FFT core. Additionally, since the Parallel search tests also several frequency bins simultaneously, it has a higher parallelism. Regarding the Parallel Code Search, it is known that performing a convolution using an FFT is more efficient than with traditional filters when the filter length is more than 64. However, when considering the complexity of implementation, Serial Acquisition surpasses parallel due to ease in its architecture as illustrated in Table 1.

Table 1. Comparison of different Acquisition Methods

Algorithm	Iterations	Complexity
Serial acquisition	41943	Low
Parallel Frequency Space Search	1023	Medium
Parallel Code phase Space Search	41	High

B. Communication blocks

1) Transmitter:

The Fig. 10 shows the simulation results of the transmitter block. The modulo-2 addition of the satellite data and C/A code is represented as ca_seq and data_seq whose product is RF_binary. RF_binary is transformed to NRZ form and then down-sampled to IF_sig after the multiplication with the local oscillator.

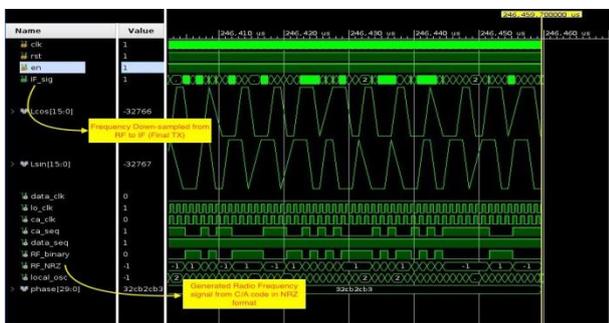


Fig. 10: Transmitter signal

2) PRN Code Generator:

The register 2 of PRN component is used to generate 1 KHz clock that is utilized to drive many blocks. The C/A clock is also used to generate the code replicas namely Early, Prompt and Late code having a difference of $\pm \frac{1}{2}$ chip duration as depicted in Fig. 11.

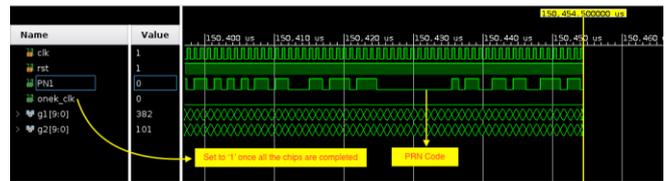


Fig. 11: PRN Code

3) Local Oscillator

The Fig. 12 depicts the generation of sine and cosine waveforms using a carrier NCO with the help of a look-up table. The step size is represented by the phase error used to generate a clock frequency of 1.26 MHz. The upper 3 bits of the accumulator which 30 bits is used as the address to find the corresponding amplitude of waveforms. The sine and cos outputs are passed on to other blocks as I and Q components represented integers.

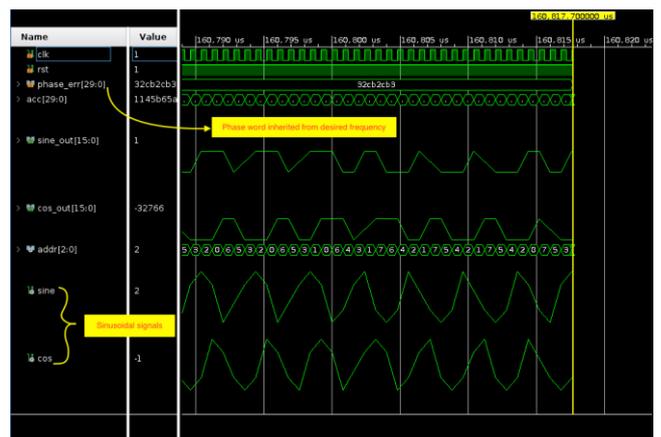


Fig. 12: Numerical Controlled Oscillator

4) Serial Acquisition

The data obtained from the RF front end is down converted to IF signal for further processing in the receiver. The sampling clock for the entire receiver processing is 10 MHz. The Fig. 13 illustrates the serial acquisition process. Once the signal is down sampled, the IF_sig is multiplied with the C/A code as well as outputs of local oscillator namely lo_sin and lo_cos. These signals are then transmitted into the correlator and finally to a decision block to check if the correlation value exceeded the pre-defined threshold. This implicitly means if the satellite is acquired or not. If the satellite is not acquired, then a delay of half chip is introduced in the C/A code generated by clk_2M as portrayed in Fig.13. This process is performed for 1023 chips until the satellite is acquired.

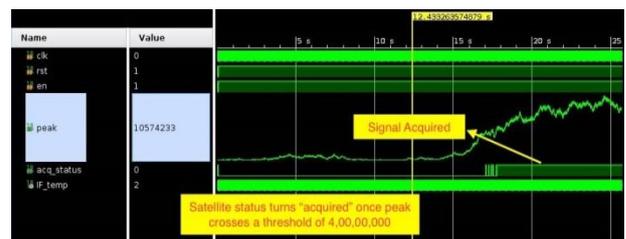


Fig. 13: Serial Acquisition Waveform



5) Parallel Acquisition

After down-sampling from RF to IF, the signal is directly parallelized based on the desired Parallel Acquisition method. For PCPS, the delay iterations of 1023 would be eliminated. On the other hand, if PFSS is used, the Doppler frequency shifts of +/- 500 Hz until +/- 10 KHz (41 iterations) would be eliminated. The Parallel Code Phase Acquisition waveform when simulated using MATLAB with 5 KHz Doppler shift and code phased delayed by 1000 chips is shown in the Fig. 14.

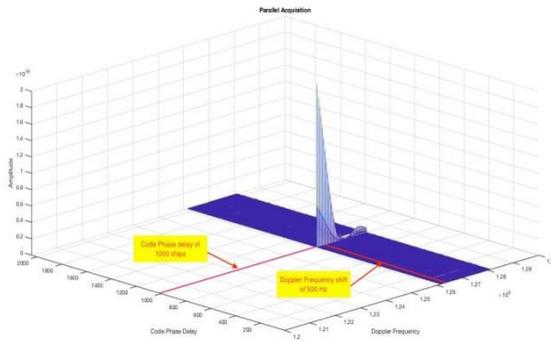


Fig. 14: Parallel Acquisition waveform

6) Tracking System

Typically, carrier and code tracking together constitute the tracking phase. Though they are implemented separately, they have to be merged together to work as tracking block. When the satellite status indicated as acq_status in Fig. 15 is acquired, the control logic transforms the acquisition mode to tracking mode to lock the carrier frequency and the code phase. During this transformation, the acquired carrier frequency during the serial acquisition is provided as an input to PLL block to generate the phase word. I_early, I_prompt, I_late, Q_early, Q_prompt, Q_late signals represent the product of advanced, replica and delayed versions of code phase with the local oscillator respectively. The PLL and DLL blocks of carrier and code tracking computes the error signal at every 1 ms. The discriminator uses the equations specified in the signal tracking section to compute the error and transfer the error signal to loop filter block to generate the phase word depicted as code_ph_pll and car_ph_pll using sfixed operations. During the course of tracking, the phase word from code_ph_pll and car_ph_pll is given to the code and carrier NCO which is used to generate the frequency respectively. Hence, the code and carrier NCO receive its phase word from the following 3 sources:

- Constant value (Before starting the acquisition toolbox)
- Doppler shifted value (Only for Carrier NCO and generated while acquisition)
- PLL or DLL generated phase word (After acquisition and while tracking).

The Fig. 15 depicts the complete IRNSS receiver indicating the transformation from acquisition to tracking.



Fig. 15 IRNSS Receiver system

VI. CONCLUSION

The research began with an overview of the IRNSS signal structure with extra attention to the theories of signal acquisition and signal tracking. The traditional and advanced acquisition methods were discussed. The acquisition is the first phase for processing of the IRNSS signal in the receiver. The goal of acquisition is to measure the code offset and Doppler frequency. The reality is that the receiver often does not know a priori which visible satellites are. A complete description of the process of acquisition and two popular methods that we could use is provided. The two important parameters produced by the acquisition are the carrier frequency and the initial C/A code phase. The serial search algorithm sequentially quests for a satellite at every possible code phase and Doppler frequency in the time domain. Since there is only need for additional and multiplication operations, time domain execution is straightforward. Since the serial search algorithm has to do a huge amount of glide correlation in a real-time IRNSS receiver, the biggest flaw of the serial search acquisition also appears to be this exhausting correlation. We could deduce that serial acquisition is a very simple algorithm, but presents many hurdles in the acquisition process, more specifically due to its time consumption.

To minimize the acquisition time, the alternative is to parallelize the search in the search grid for either the Doppler frequency or code phase. The downside of this method is that, it can require a higher order FFT, based on the sampling frequency and the coherent integration time, causing limitation for some implementations. Upon identification of the satellite comprising the signal with code phase and Doppler frequency, traditional receivers utilize code and carrier tracking loops to produce error signals that maintain the replica and obtained codes aligned and also maintain the receiver tuned to the correct frequency as changes take place in Doppler. For C/A code phase and carrier Doppler tracking, DLL and Costas PLL are used in the tracking loop respectively. At the specific and required rate, the data was generated locally using the communication blocks to detect the Doppler frequency and code phase.



It was further demodulated to extract the transmitted data using tracking loops. Several practical simulation scenarios were used to analyze the reliability of the proposed model.

Outcomes of simulation prove that our IRNSS receiver software performs reliable acquisition and tracking and offers an experimental platform for designing and developing new algorithms to improve the efficiency of IRNSS receivers. The proposed model lays the groundwork for several enhancements in the performance of the receiver in various aspects. Most importantly, the design optimization is required to minimize the resources. Adding the potential to track multiple satellite is highly advantageous. Once the IRNSS satellites attain the signals, most of it will switch to tracking mode due to the continuous alterations in Doppler frequency and code phase. Thus, collective monitoring of multiple IRNSS signals should be an active area of research. Also, latency has a great effect in the real-time situations. The obtained results can be used to model the timing constraints and resource allocation for an accurate synthesis. It is evident from the simulation that serial acquisition consumes 41933 iterations, when compared to 1023 in PFSS and 41 in PFSS to acquire the signal.

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