

# Design of Vedic Multiplier using GDI Method

P. Manju, P. B. Sreelakshmi, T. Madhavi

**Abstract:** Multipliers are the main building blocks for many of the fast processing systems [1]. The need for high speed multipliers increases as the need for high speed processors increases. Many multipliers have been developed to enhance the performances of the circuit. Among them Vedic multipliers are the rapid and powerless multipliers. Vedic multipliers are supported by Vedic mathematics and it consists of sixteen sutras or algorithms to perform logical operations. This paper focuses on designing Vedic multiplier using novel adder based on vertically and crosswise method of Vedic mathematics, which uses GDI technology and further it is compared with existing CMOS technology. Vedic multipliers are designed with 250nm technology and approved using Tannerv15.2. Simulated result proves that the Vedic multiplier using novel adder is more efficient.

**Index Terms:** Back End Tools, CMOS, delay, GDI (Gate diffusion input), logic family, Vedic multiplier

## I. INTRODUCTION

Multiplication is an important arithmetic operation for many applications like microprocessors, DSP and Communication. A huge number of adders are required for high order multiplication to perform partial product addition. The value for low-power and high speed multipliers has been increased due to the need for high speed processors [2].

An adequate multiplier has to consider there following characteristics accuracy, speed and area. Multiplication operation has mainly three steps, 1. Differential product generation, 2. Differential product reduction, 3. Finally the addition processes. Among the various forms of multipliers, Vedic multiplier is a rapid and powerless multiplier. Vedic multipliers are supported by the concept of Vedic mathematics and it consists of sixteen sutras or algorithms to perform logical operations. [2]. Using Vedic multiplier in the computing process helps to reduce the area of complexity, decapitation time, power etc.

Time delay is largely minimized for Vedic multipliers when the bit number extends 8X8 bits up to 16X16 bits, when considered to the rest of the multipliers. Vedic multipliers have the greatest advantage when considered to the remaining multipliers based on gate delays and periodicity of logical format. It consists of mental calculation technique which has been based on Vedas and also it consists of sixteen sutras or algorithms to perform logical operations.

Urdhva Tiryagbhyam (which uses vertically and crosswise technique), is the most broadly used sutra for the implementation of Vedic multipliers. In this text, the design of the Vedic multipliers using novel adder which uses GDI technology is explained and is further compared with the existing CMOS technology. They are compared based on

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their performances. This paper further organized as: Section II presents Vedic multiplier. Section III explains about GDI method. Section IV presents proposed Vedic multiplier. Section V exhibits about simulation results and also the conclusion is presented in Section VI.

## II. VEDIC MULTIPLIER

Veda is word derived from Sanskrit, which means knowledge or wisdom in ancient India. Vedic mathematics has been restored from the ancient text which is referred to as Vedas. Vedic mathematics is a booklet which is composed by Swami Bharati Krishna Tirtha and was promulgated in 1965. The booklet consists of intellectual procedure technique which has been based on Vedas and also it consists of sixteen sutras or algorithms to perform logical operations [3]. Urdhva Tiryakbhyam (which uses vertically and crosswise technique), is the most broadly used sutra for the implementation of Vedic multipliers. By using this sutra, when number of bits increases both area and delay increases slowly. Style of the Vedic multiplier lies in the fact that they can be used for solving bulky mathematical operations, thereby enhances the performances of the circuit. Figure 1 shows the structural diagram of Vedic Multiplier.

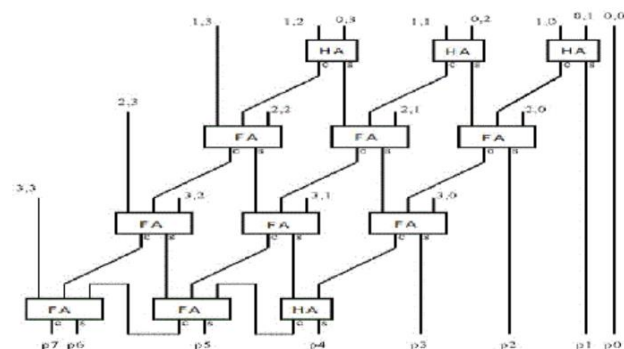


Figure 1 Block diagram of 4X4 Vedic multiplier

## III. GDI METHOD

Gate diffusion input (GDI) is a method used for describing the structure of low-power digital combinatorial circuit. Consumption of power, delay that is produced and complexity of the circuit are reduced using this technique; thereby it maintains less complexity in logical layout [4]. The GDI technique is implemented using two transistors for a deep range of complex logic design. This technology is applicable for the structure of rapid and powerless circuit, by maintaining the transistors less in number. The elemental structure of the GDI cell looks similar to the structure of the inverter based on CMOS, and also has relevant distinctions:

The GDI elemental cell consists of 3 inputs:

1. The GDI cell consists of three inputs, G represented as familiar gate input to NMOS and PMOS, P as the input to source or drain of PMOS, and N which is represented as input to source or drain of NMOS.
2. Both NMOS and PMOS bulks are associated to N or P (respectively), as it can be promptly based at distinguishing with a CMOS inverter

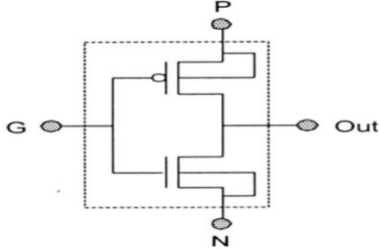


Figure 2 Basic GDI cell

GDI design method makes any complex function simple when compared with CMOS based design and standard PTL [5] [6]. In GDI implementation of the OR gate needs two transistors and XOR gate requires four transistors. While observing the improvement of the digital logic design it seems to be that GDI technique is superior when compared to other techniques because this method is easy to execute, cost efficient and is supported by multi-functional blocks [7].

IV. PROPOSED VEDIC MULTIPLIER

In this portion the operation and theoretical analysis of the proposed Vedic multiplier using novel adder has been carried out [8]. The whole circuit is constructed based on GDI technology. 10T is the number of transistors used in the working of each full adder.

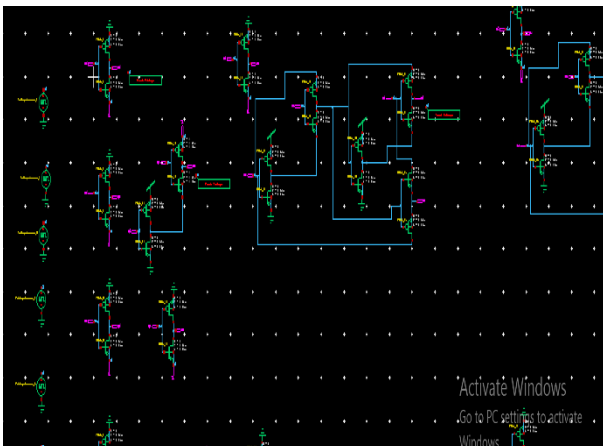


Figure 3 Schematic of GDI based 4X4 Vedic multiplier using Novel Adder

The proposed Vedic multiplier overcomes the disadvantages of the existing Vedic multiplier, by reducing the area of complexity of the circuit and also reduces time delay, so thereby improving the speed of operation [9][10]. The output product terms are obtained as P0 to P7. Schematic diagram of proposed Vedic multiplier using novel adder which uses GDI technology is demonstrated in the Figure 3.

V. SIMULATION RESULTS

In this portion, the implementation and theoretical analysis of the suggested design are observed. The analysis is carried

out at 250nm technology using Tannerv.15.2. The performance of the Vedic multiplier using novel adder based on GDI technique is determined in regards of delay and transistor count [11]. Tanner EDA tools are used for constructing integrated circuits. These tools let on entering schematic; performing SPICE simulation, for doing physical design and also to perform design rule checks (DRC) and then to do layout versus schematic (LVS) checks. Here are the 4 types of mechanisms used in this procedure:

1. S-edit - a schematic mechanism
2. T-spice - the SPICE simulation mechanism which is combined with S-edit
3. L-edit - a physical layout design mechanism to make layout
4. W-edit - the waveform tool

Figure 4 shows the output waveform of the modified Vedic multiplier applying novel adder based on the GDI technology. A and B are the inputs, as it is 4-bit the inputs are taken as A0A1A2A3 and B0B1B2B3. The output is obtained as 8bit product that is represented as P0 to P7 [12]. Total number of devices used is 145 and the time delay obtained is less than the existing multiplier that is 2.22ns. Thereby, speed of operation increases and gives high performance. Here multiplication inputs are given as 3 and 2 in binary value. The output obtained after multiplication is 6 in the form of binary. Comparison between the performance of the proposed Vedic multiplier to the existing one, based on their time delay and transistor count is shown in the Table 1.

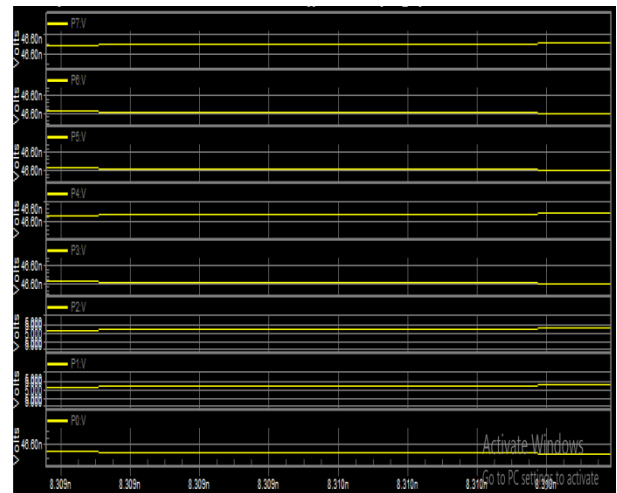
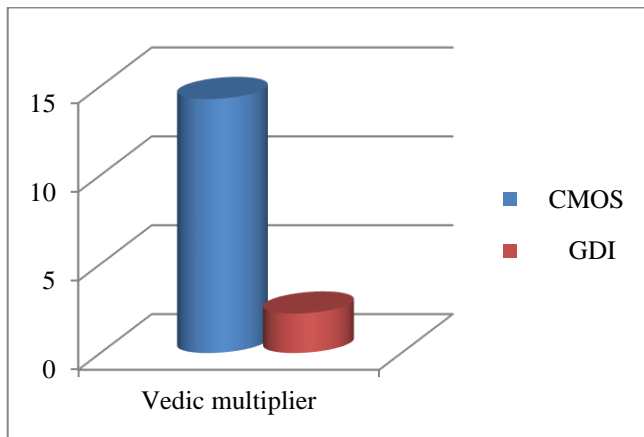


Figure 4 Output waveform of GDI based 4X4 Vedic multiplier using Novel Adder

Table 1 Performance Comparison of CMOS and GDI based Vedic multiplier

Multipliers	CMOS			GDI		
	No. of Transistors	Over head Delay	Total Delay	No. of Transistors	Over head Delay	Total Delay
Vedic	553	1.10 ns	14.29 ns	146	0.90 ns	2.22 ns



**Figure 5 Graph based on Performance Comparison of CMOS and GDI of Vedic multiplier**

Figure 5 show the graph based on the performance analysis of CMOS and GDI technologies in the Vedic multiplier. And it also proves that the proposed Vedic multiplier using novel adder based on the GDI technology is much better than the Vedic multiplier supported by conventional CMOS logic scheme.

## VI. CONCLUSION

The paper presents the Vedic multiplier based on Vedic Mathematics which uses Urdhva Tiryakbhyam sutra. The concert of 4-bit Vedic multiplier performed by the both CMOS and GDI method is implemented on Tannerv15.2 using 250nm technology. Using CMOS logic computational time delay of Vedic multiplier is found to be 14.29ns and the proposed Vedic multiplier using GDI technique time delay is found to be 2.22ns [13]. And also the area of complexity of the proposed Vedic multiplier based on GDI technique is reduced by 73.59% when considered to the Vedic multiplier supported by conventional CMOS logic scheme. Thereby, it concludes that the performances of the proposed 4-bit Vedic multiplier using GDI method is highly effective based on area of complexity and time delay when considered to conventional CMOS logic. In many applications the most essential requirement is to reduce time delay for improving the performance of the circuit and this proposed Vedic multiplier design is very much suitable.

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