Area and Interconnect length Optimization for VLSI Floor Planning Problem By using Harmony Search Algorithm

S. Venkatraman, M. Sundhararajan

Abstract: ***Floorplanning is that the terribly central stage in VLSI physical style for class conscious building module style methodology. Floorplanning affords early response that evaluates architectural choices, approximation of chip space, estimates delay; interconnect length and congestion caused by wiring. As technology advances, style complexness is increasing and therefore the circuit size is obtaining larger. Thus space of the circuit gets increase and tougher to minimizing the interconnect length. The VLSI floorplanning is that the NP onerous downside. So it's horribly troublesome to seek out the best solution. During this paper we tend to take into account, a multi-objective hybrid genetic algorithmic program primarily based floorplanning has been developed with novel crossover operators to handle the multi-objective floorplanning for Very Large Scale Integration application specific integrated circuits (VLSI ASICs). The Genetic algorithmic program (GA) with harmony search algorithm approach is employed for minimizing the whole space and interconnects length.***

Key Words: VLSI slicing floorplan, Harmony search Algorithm (HAS), Area and wirelength.

I. INTRODUCTION

The tense growth in technology for very large scale integration (VLSI) circuit style and manufacturing has managed to entire systems with multitudinous semiconductor device being placed on one chip. as a result of the high complexity of recent chip style, VLSI CAD tools are dynamic for delivering high VLSI system performance. for several problems in layout style, the machine complexity is NP-hard [1]. The long term nice growth of VLSI circuits will take into account the event of physical style automation tools. a conventional floorplanning formulation near decide the layout of a given set of modules, nominative no overlapping modules.

Supported the circuit style and additionally the hierarchy, an acceptable floorplan is decided. An immoral floorplan will cause wastage of die area and cant able to succeed fixed outline constraints [2]. The Harmony Search (HS) methodology could be a metaheuristic improvement algorithmic program proposed in [17] [19]. It mimics a musical improvisation method within which the musicians in an orchestra/band try and realize an ideal state of harmony through musical improvisations.

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Once musicians compose harmonies, they typically attempt varied potential combos of the music pitches stored in their memory. This algorithmic program was designed to mimic the approach a musician uses memory and therefore the past experiences to lead his/her to the note that leads to the foremost pleasing harmony once vie alongside the opposite musicians. HS is simple to implement and may easily be applied to resolve virtually any drawback that may be designed because the decrease or maximization of an objective performs. This type of economic explore for an ideal state of harmonies is said to the procedure of finding the optimum or near-optimal solutions for a tangle. Once resolution a selected problem, every musician is taken into account as a call variable. So, the right harmony means that the global or near-global solution[3]. In HS, every musician corresponds to a choice variable within the resolution vector of the problem and conjointly represents a dimension within the search area. Every musician (decision variable) incorporates a totally different instrument whose pitch vary corresponds to a choice variable's worth vary. A solution vector, conjointly known as associate degree improvisation, at sure iteration corresponds to the music at a selected amount, and also the objective perform corresponds to the audience's aesthetics. New improvisations are supported earlier remembered sensible ones that are keep within the arrangement known as the Harmony Memory (HM). A replacement resolution is temporary by exploitation 3 rules. They're (a) Play what he/she specifically is aware of (memory consideration) (b) Play by slightly adjusts the pitch (pitch adjustment) and (c) Play a new composition (random selection).The main control parameters of HS algorithm are harmony Memory (HM), Harmony Memory Size (HMS), Harmony Memory Considering Rate (HMCR), Pitch Adjusting Rate (PAR), and Bandwidth (BW). Here, HM is a memory location where all the solution vectors are stored; HMCR and PAR are parameters that are used to improve the solution vector.

Problem Description

Let M be the set of modules diagrammatic by M=, where N is that the amount of modules. each module mi is pictured by (Wi, Hi), where 1≤i≤N, wi is dimension of the module mi and Hi is that the height of the module mi. The magnitude relation of mi is outlined as Hi / wi. the area Ai of the module mi is given by wi *Hi. There ar 3 fully differing types of rectangular modules specifically soft modules, hard modules and pre-placed modules.

The soft modules have variable magnitude relation at intervals fastened vary and fixed space. In hard modules, every house and quantitative relation square measure mounted structure. the frilly description is given as follows: Slicing floorplan: A slicing floorplan is obtained by cutting the floorplan either horizontally or vertically repetitively. Fig.1 (a) represents slicing floorplan. A slicing tree can be a binary tree. The pre-placed module can be a one throughout that modules coordinates' area unit given by the floorplanner. Let H denotes set of hard modules, S denotes set of soft modules and P denotes set of preplaced modules[4]. Let M be the union of these 3 sets of modules. The illustration of floorplanning are exhausted 2 layout forms, specifically the slicing structure and non-slicing that's accustomed represent a slicing floorplan. Generally, there are 2 cut types, + and -. The + (-) represents floorplan horizontal (vertical) cut. Fig.1 (b) shows a slicing tree of floorplan.

Non slicing floorplan

Non slicing floorplan is more common than slicing floorplan. All the children of the given cell cannot be obtained by bisecting the floorplan. This is called non-slicing floorplan fig 2.

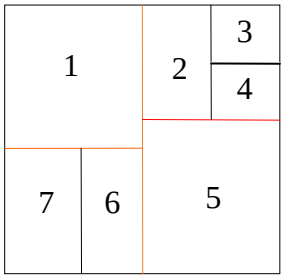


Figure 1: (a) slicing floorplan

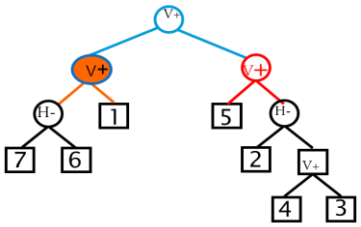


Figure 1: (b) slicing tree

Horizontal constraint graph and vertical constraint graph can be used to model a non-slicing floorplan. In a constraint graph, a node represents a module. The foremost aim of this paper to minimize the dead space (white space) & fix the module in fixed outline constraint. In this paper we dealt with slicing floorplanning [5]

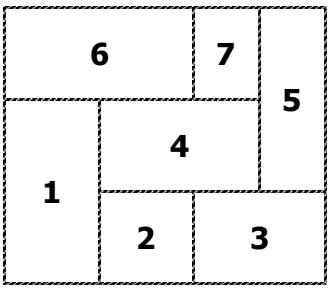


Figure 2: Non slicing floorplan

Representation of Floorplan

Polish Notation is employed to model Slicing Floorplans. The Binary Tree is employed to say a Polish notation, E= e1 e2...e2n-1 wherever ei € . Here, every range represents a module and H+, V- represents a horizontal and vertical cut severally within the slicing floorplan. The Polish expression is that the termination ordering of a binary tree, which might be obtained from the post-order traversal on a binary tree [6]. Polish expression length is 2n1, wherever n – is range of modules.

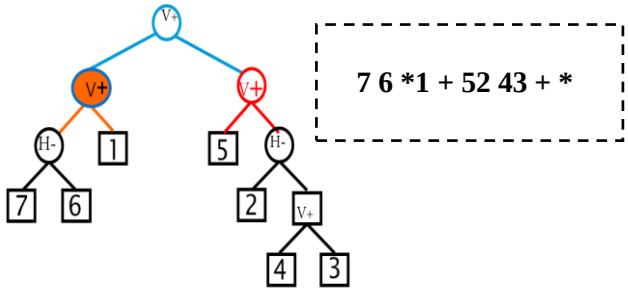


Figure 3: Polish Expression

II. PROPOSED METHOD

The main control parameters of HS algorithm are harmony Memory (HM), Harmony Memory Size (HMS), Harmony Memory Considering Rate (HMCR), Pitch Adjusting Rate (PAR), and Bandwidth (BW). Here, HM is a memory location where all the solution vectors are stored; HMCR and PAR are parameters that are used to improve the solution vector. The following steps are followed to implement proposed method

Step 1. Harmony Memory and Improvisation method

The core arrangement of HS could be a matrix of the most effective resolution vectors known as the Harmony Memory. The quantity of vectors that are at the same time processed is understood because of the Harmony Memory Size (HMS). It's one amongst the algorithm's parameters that have to be set manually. Memory is structured as a matrix with every row represents an answer vector, and also the final column represents the vector's fitness value. Within the HS formula, $\hat{H}$ represents the harmony and $f(\hat{H})$ denotes the melody of harmony $\hat{H}$. during an N-dimensional problem, the HM would be described as:

$$\begin{matrix} \hat{H}_1^1 & \hat{H}_1^2 & \hat{H}_1^3 \cdots & \hat{H}_1^n & | W_1 \\ \hat{H}_2^1 & \hat{H}_2^2 & \hat{H}_2^3 \cdots & \hat{H}_2^n & | W_2 \\ \vdots & \vdots & \vdots \cdots & \vdots & | \vdots \\ \hat{H}_{HMS}^1 & \hat{H}_{HMS}^2 & \hat{H}_{HMS}^3 \ldots . & \hat{H}_{HMS}^n & | W_2 \end{matrix}$$

Before improvement starts, the HM is initialized with HMS at random generated solution vectors. Based on the problem, these vectors may also be at random chosen around a seed purpose which will represent an area within the search area wherever the optimum is possibly to be found [18]. Every call variable is improvised one by one, and anybody of the 3 rules are often applied for any variable. The HMCR is one in all the HS controls however typically the HM is taken into consideration throughout improvisation. For traditional HS, memory thought implies that the selections variable's value is chosen directly from one in all the answer vectors within the hm. A random number is generated for every call variable. If it's less than the HMCR, the memory is taken into consideration; else, a price is at random chosen from the vary of potential values for that dimension. The Pitch Adjustment Rate (PAR) is set throughout initialization, and it controls the quantity of pitch adjustment done once memory thought is employed. Another random number is generated. If it's smaller than the PAR, the makeshift value is pitch adjusted using (1):

$$\hat{H}new = \hat{H}new + random\ ().\ BW \quad ---\ (1)$$

Ĥnew is that the new pitch-adjusted value, is that the previous value chosen exploitation memory thought, random () could be a random value between −1 and 1, and BW is that the bandwidth parameter. It the utmost variation in pitch adjustment and is one in all the parameters that has got to be manually set. Once a brand new value has been improvised, the memory is updated by comparison the new improvisation with the vector within the memory with all-time low fitness. If the new improvisation includes a higher fitness, it replaces the vector with all-time low fitness. This method of improvisation and update continues iteratively till some stopping criterion is consummated, or the utmost variety of iterations is reached.

Steps2: Harmony Selection (HS)

In this step, New Harmony vector is generated supported 3 rules, namely, memory consideration, pitch adjustment, and random selection. The value of a style variable are often chosen from the values keep in HM with a likelihood HMCR. It are often more adjusted by moving to a neighbor value of a specific value from the HM with a likelihood of PAR, or, it can be chosen at random from the set of all candidate values without considering the stored values in HM, with the chance of (1 - HMCR).

Table III- Results of the proposed algorithm in different iteration

bench mark circuit	HMS value	HS Area in mm2 (%)no of Iterations			
		100	200	1000	1500
Apte	30	48.95	48.85	48.5	47.7
	40	48.5	48.5	48.3	47.5
	100	48.6	48.98	48.43	47.63
	150	48.6	49.01	48.46	47.66
Ami 33	30	1.52	1.38	1.35	1.2
	40	1.835	1.75	1.35	1.25
	100	1.75	1.75	1.3	1.25
	150	1.85	1.75	1.3	1.24
Ami 49	30	2.51	2.75	2.79	1.99
	40	2.43	2.68	2.8	2
	100	2.59	2.68	2.8	2
	150	2.6	2.67	2.8	2
hp	30	10.98	10.16	10.05	9.25
	40	10.8	10.78	10.54	9.74
	100	11.08	10.68	10.3	9.5
	150	11.01	10.7	10.3	9.5

Step 3: Termination criterion

HS algorithm is terminated if the stopping criterion (maximum number of improvisations) has been met; else steps 2 and 3 are repeated.

Fitness function Evaluation

The main objective of the floorplanning is to minimize the total chip area and wire length[18,19]. The formula for calculating the total area and wire length of the chip that contains 'i' modules is given in (2):

$$Area = \sum_{i=1}^{n} (L(i) * W(i)) \quad -----(2)$$

$$Wire\ length = \sum_{i=1}^{m} W_L \quad ------(3)$$

$W_L = (Xmax - Xmin) + (Ymax - Ymin)$

Here Xmax and Xmin are the maximum and minimum x-coordinates of the HPWL (Half perimeter wire length) bounding box of the net.

Ymax and Ymin are the maximum and minimum y-coordinates of the HPWL bounding box of the net

By maximizing or minimizing the fitness values in every generation, the global optimum value may well be

found. The fitness operate for the proposed method is given in (5).

$$f(X) = \varphi * Area + \omega * Wire\ length - -(4)$$

ere, φ and ω values are treated as the weighting factors. In this proposed work φ and ω value is taken as 0.9, 0.3.

III. RESULT AND CONCLUSION

The proposed technique utilizes fixed die outline with exhausting rectangular modules for floor-planning. The experiments during this study create use of MCNC (Microelectronics Center of North Carolina MCNC 2004) benchmark circuits for the proposed floor-planners. Simulations are dispensed for the MCNC benchmark circuits specifically apte, ami33, hp, and Xerox. The performance of the Harmony Search algorithm is evaluated for VLSI floorplanning. In this work, the HMS value is taken as 40, 60 and 100,150. Table III and Fig 4 explains the proposed algorithm is run by 100, 200, 1000 and 1500 iterations. Table IV and Fig 5 shows the results of the proposed algorithm. Fig 5 compares the performance of the proposed work with other existing works.

The optimum result for the apte circuit is obtained when HMS value is 40 and 100. When HMS value is 100 the minimum area is achieved for ami33 circuit. For hp circuit, the minimum area is obtained in 1000th iteration with HMS value as 40. The minimum area for Xerox circuit is attained when HMS value is 30 and 100.

Table IV- Comparison of the proposed work with existing methods

Methods	apte	Ami33	ami49	Xerox	hp
B-tree	46.92	1.27	2.98	19.83	8.95
Hybrid Genetic	47.01	1.19	2.8	20.14	9.13
Simulated Annealing	48.47	1.23	2.7	20.42	9.48
Hybrid Simulated annealing	48.12	1.25	2.6	21.86	9.43
Particle Swarm Optimization	47.44	1.24	2.4	20.2	9.6
Harmony Search	46.7	1.28	2.5	20.64	9.01

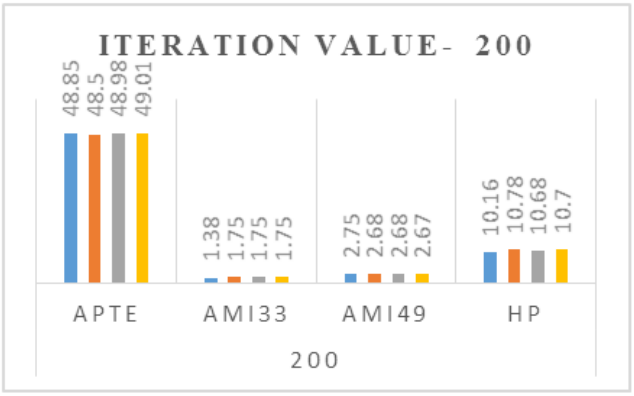


Figure 4: Performance of MCNC benchmark circuit with different iteration

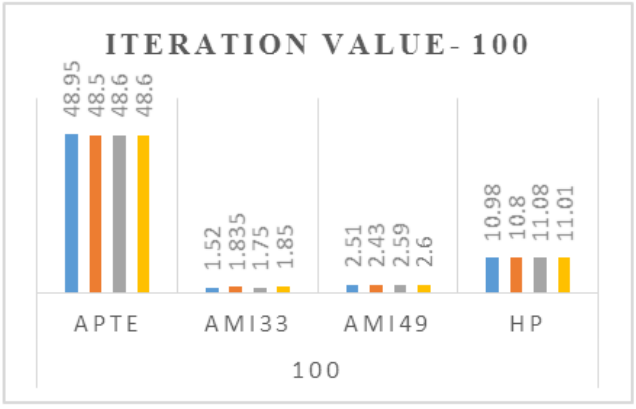
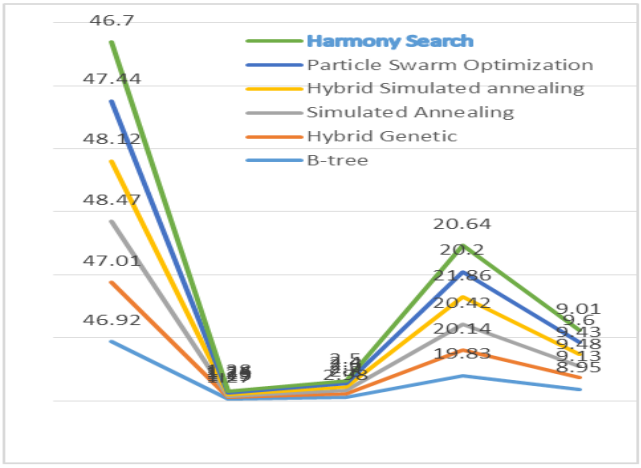


Figure 5: Comparison chart of the proposed work with existing methods.



VLSI floorplanning is an NP-hard problem. To solve this issue in an efficient way, harmony–encouraged Harmony Search algorithm is proposed in this paper. The simulation results shows good and reasonable solution for the slicing floorplan of hard and soft modules within fixed die constraints. From the results it is inferred that the performance of the proposed method is comparable to existing algorithms. When a number of iteration rises, the whole area of the floorplan gets minimized.

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