Amassed Simulation Edification of Modelsim and MATLAB by using Third Harmonic Injected Sine PWM Generation with Inverted Sine Carrier for Three Phase Inverter

Sreeja P[1], Dr.L.Padmasuresh[2] , Dr.P. Muthukumar[3]

Abstract: ***Simulation and real time implementation environments are the few deciding factors to decide the designing time for any power electronic conversion system especially for the inverters. Reshaping and rearranging of carriers based pulse width modulation has been perceived as an alluring power conversion strategy for DC-AC conversion. This article edifying the simulation and FPGA design environments by using new half controlled PWM switching strategy for three phase VSI through randomized inverted sine carrier variation and third order harmonic injected sine reference. The suggested switching technique enhancement the line to line voltage fundamental component with tiniest total harmonic distortion compare with the well-known Sinusoidal PWM techniques. The in-depth study of the suggested modulation technique and the way of implementation, is approved through MATLAB/Simulink and the switching pulses are creating from Modelsim digital environs. For real-time implementation Field Programmable Gate Array (FPGA) have employed and also this study shows the FPGA performance along with three phase inverter hardware results.***

Index Terms: Pulse width Modulation, Field Programmable Gate Array, Linear Feedback Shift Register, Total Harmonic Distortion.

I. INTRODUCTION

Power electronics has changed rapidly during the last twenty-five years and the number of applications has been growing, principally due to developments of the semiconductor devices and the chip technology [1-2]. The chips are aiding to generate the Pulse Width Modulation (PWM) pulses for power semiconductor switches [2]. The chip designs are broadly classified into two digital system design approaches for industrial control applications. 1. A software (sequential) design methodology on either Digital Signal Processors [1] (DSPs) or micro controllers along with embedded peripherals 2. A Hardware (parallel) approach, habitually having constrain to solve specific parts of complications requiring superior performance [3]. The Fabrication verified VLSI termed as Field programmable gate array (FPGA).

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Sreeja P, Department of EEE, Noorul Islam center for higher education, Thucklay, Tamilnadu, India,
Dr.L.Padmasuresh,Department of EEE, Baselios Mathew II College of Engineering, Sasthamkotta, Kerala,India
Dr.P.Muthukumar, Department of EEE, PVP Siddhartha Institute of Technology, Vijayawada, Andhra Pradesh,India

FPGA is establishing themselves as one of the favoured digital accomplishment platforms in a superfluous of current industrial solicitations, and continuation of developments are unceasingly being encompassed in the devices. As compared with DSPs and Microprocessors, FPGAs are progressed due to delightful advantage of fabrication technology focused to shrinking the size, vendors started to design soft processor cores that may be formed from standard FPGA resources, as well adapt embedded processors in their devices [3]. This tendency has seen a tremendous unceasing development, to the range that current solutions are uncountable.

The Power Electronics Inverters are widespread from the past fifty years due to the migration of DC drives to AC drives for many industrial applications [4]. The efficiency of the power electronic inverter is not only depends up on control techniques involved, also it depends upon how the control techniques are implemented by using digital design [5]. The hardware approach of such digital design was hardened by the insufficient awareness of the design tools and the corresponding technology, shortage of development of these tools, price and absence of several dedicated hardware functionalities.

MATLAB® is a multi-domain programming platform designed specifically for scientists and researchers [4]-[6]. The core of MATLAB is the MATLAB language, a matrix-based language permitting the most usual expression of computational mathematics and the MATLAB Simulink. The Power Electronics Tool box added from the version of MATLAB 1.0. Xilinx-Project Navigator tool manages the digital design files and allows to run processes to move the design from design creation through implementation to programming the targeted Xilinx® device[7]. ModelSim is a GUI based simulation and verification software for System Verilog ,VHDL, Verilog and mixed- language designs.

FPGAs stipulate the engineers with the ability of swiftly designing hardware circuits. And also increase in the configurable logic capacity of FPGA and decrease in cost of FPGAs have procured the designers to amalgamate FPGAs in their controller designs [13-14]. The PWM technique is a technique to control within the Inverters. The carrier and reference modifications are lead a role to improve the fundamental and decrease the Total Harmonic Distortion (THD) for any PWM based inverters [5-9].

In this article, third harmonic injected sine PWM generation with inverted sine carrier for three phase inverter taking as a case studies and also compared the performance with existing methods. In Section 2. Explains the MATLAB methods for three phase inverter simulation and interface with FPGA. Section 3. FPGA design and analysis of proposed PWM method and presented FPGA performance for each sub modules. In Section 4. Discussed about proposed SPWM Simulation and experimental results.

II. MATLAB ENVIRONMENTS FOR THREE PHASE INVERTER SIMULATION AND INTERFACE WITH FPGA PROPOSED METHOD

MATLAB Environments supports two practices to implement the three phase inverter design with control techniques in MATLAB.

A. Script File(.m file)

Script File or .m file can be written to send the PWM pulses through the I/O ports of the Computer. These I/O ports are sending PWM pulses to the three phase inverter through the external amplifier and isolator. The drawback of this method is, MATLAB should be in running mode in computer as long as the motor is running.

B. In Build Libraries (Simulink)

a. Simulation by using MATLAB in-build libraries alone:
The in-build libraries are called tool boxes[4]. The various tools are available in simscape power system tool box. These tool boxes helping to design three phase inverter and the PWM pulses generation. This method also having the same kind of drawback like the script file method. But this Simulink method is easy to understand and control.
b.Cosimulation-by using MATLAB in-build libraries along with Modelsim files: Co-simulation is a methodology to run one or more software's parallel [6]. The tool box called HDL-Cosimulation shown in Fig. 1. is act as an interface between Modelsim and MATLAB. VHDL based PWM generation can be developed and incorporated in Modelsim. These VHDL design files can be called and compiled from MATLAB environment. The 3Φ inverter is also designed in MATLAB Simulink environs. So the tool can easily interface with Modelsim generating PWM with MATLAB based three phase inverter.

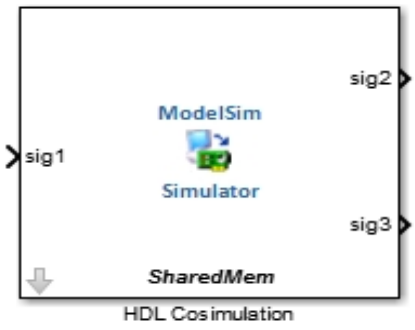

Fig.1. HDL Cosimulation tool box

The main advantage of this method is, there is no extra design time is required after the cosimulation. Targeting FPGA device information is not required while practicing cosimulation [7,9].

C. Simulation with System Generator(HDL Coder):

The HDL Coder is a MATLAB toolbox used to make synthesizable VHDL and Verilog codes for various FPGA and ASIC technologies. The drawback of this method is, the FPGA device information is required while generating the code.

III. FPGA DESIGN AND ANALYSIS OF PROPOSED PWM METHOD

PWM is the internal control method of the inverter, which governs the output voltage efficiently. Sinusoidal PWM is a method, which decides the ON and OFF period of the switches by comparing sinusoidal reference and triangular carrier[9]. Principally, the PWM methods can be classified into two groups, (i) By changing the reference waveform and (ii) Changing the carrier waveform. Discontinuous PWM ,centre Boosted PWM [7] and Third harmonic Injected PWM [6] are the sub divisions of first group. Whereas the Shape of the carrier and its frequency (Deterministic and non-deterministic) are decides the sub divisions of the second group [7]-[12]. Inverted sine carrier is the best replacement of triangle carrier and the random frequency of the carrier also given attraction from year of 2000 onwards[10]. Third harmonic injected SPWM is the attractive solution where the application needed high fundamental voltage at less modulation index[7]. In the proposed design illustrates the amalgamation of both third harmonic injected sine reference and random frequency inverted sine carrier with half controlled switching strategy (i.e PWM is generating only half cycle). The FPGA design of proposed method shown in Fig. 2. The proposed design can be targeted any FPGA device. This article targeted to XC3S500E-320f device. Fig. 2. shows that the digital implementation of the proposed work has been divided into three blocks. a. 3rd harmonic injected sine reference generation block, b. Inverter sine carrier generation block, c. Comparator and dead time insertion block.

A. 3rd harmonic injected sine reference generation block

The reference of 3rd harmonic injected sinusoidal PWM is based on the following equation

$$V_{ref} = m_a \sin(\alpha) + \frac{1}{3} m_a \sin(3\alpha) \quad (1)$$

m_a-> modulation index
α-> angle varies from 0° to 2∏.

It is the fraction of the reference voltage to the inverted sine carrier wave.

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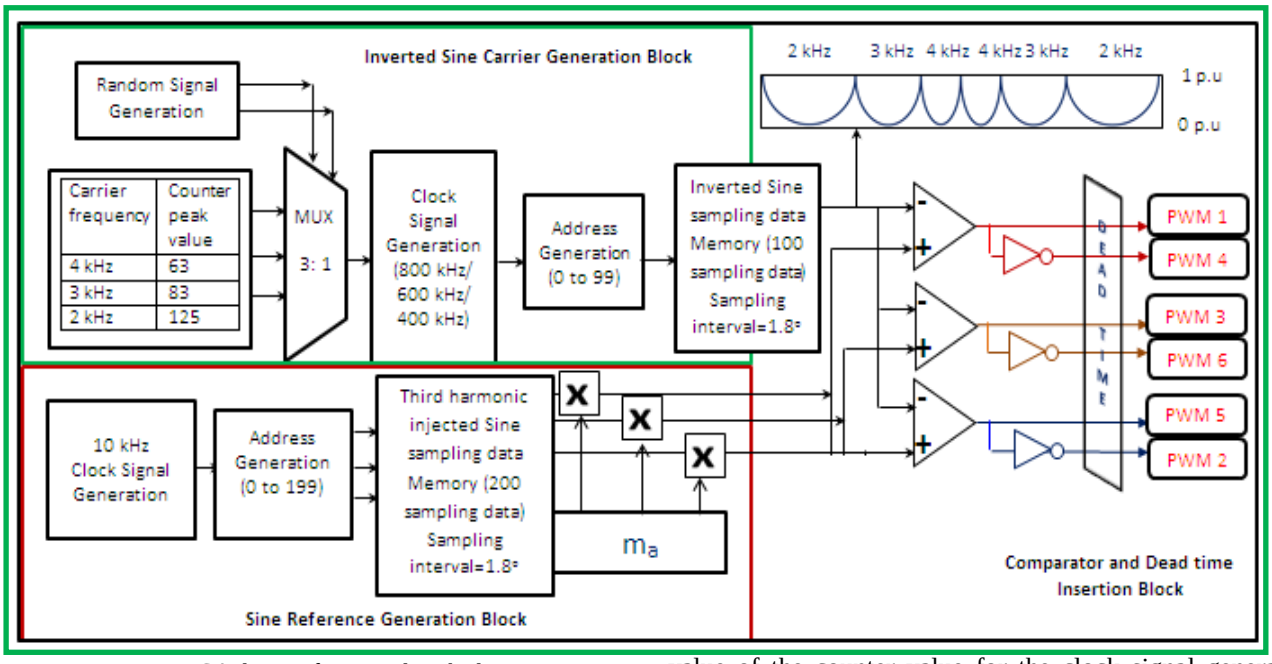

Fig 2. FPGA design of proposed method

In the FPGA based digital design environment, reference waveform has been generated based on the above equations (1). The reference design consists of 1. Address generation modules 2. Third harmonic injected Sine wave generation module 3. 10 kHz clock generation module and 4.multiplier components. In the first address generation module have an up counter starting from 0 to 199.These address will be generated and pointing to three memory location of the third harmonic injected sine wave memory. These modules receive the 10 kHz clock signal from the clock generators. The clock generator is a clock divider which is used to convert 50 MHz into 10 kHz. The method to generate the sine samples is shown in Fig. 3. Illustrates effectively. The output of the sine generation modules depicts in Fig. 3. With the advantage of FPGA programming, both sine waves are generated parallel. The resultant sine wave clearly depicts in figure 3. The sine wave sampling has been taken as per Fig. 4. Total samples for a cycle is 200. So that sampling duration is 360°/200, which will give 1.8°. The 10 kHz has been used to sample the 50 Hz sine data. The entire section occupies 1668 Look up table (LUT) out of 9312 available LUTs in the targeted FPGA device.

B. Inverted Sine Carrier (ISC) signal generation

The projected ISC is comprised of 5 modules. Namely, 1. Random bit generator 2. Multiplexer 3. Clock generator based on the divider principle 4. Address generation and 5.Inverted sine carrier generation.In the random bit generator module, two random bit has been generator based on the pseudo random binary sequence. It consists of two 8 bit linear feedback shift registers.The shift register data has been moved to the next most significant bit in every carrier frequency. These random bits will act as selector lines of the 3:1 multiplexer. The multiplexer is used to give the peak value of the counter value for the clock signal generator. The address has been generated from 0 to the peak value.

Thepeak value has been assigned is based on the below simple logic.

```
if R1='0' and R2='0' then
        Peak value= 63   // for 4 kHz carrier generation
else if R1='1' and R2='1' then
        Peak value= 125   // for 2 kHz carrier generation
else
        Peak value= 83   // for 3 kHz carrier generation
```

These peak values will decide the resultant clock generation which are 800 kHz, 600 kHz and 400 kHz from the base clock of 50 MHz. These clocks will generate the addresses from 0 to 99. This address points to the inverted sine carrier block. In the inverted sine carrier block comprises of inverted sine sample data which generate every positive edge of the resultant clock (800 kHz or 600 kHz or 400 kHz). The subsequent shape of the inverted sine as shown in Fig. 3. This design occupies 567 LUTs out of 9312 in the targeted device.

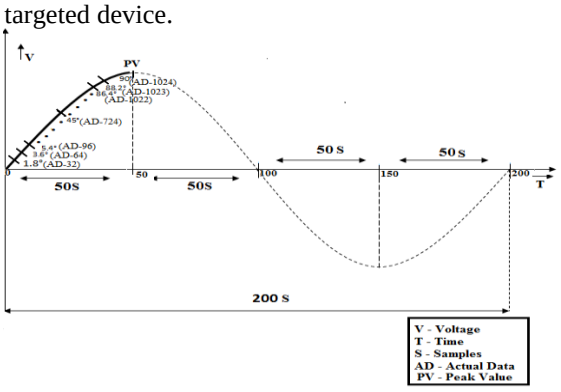

Fig. 3.Sine wave sampling representation

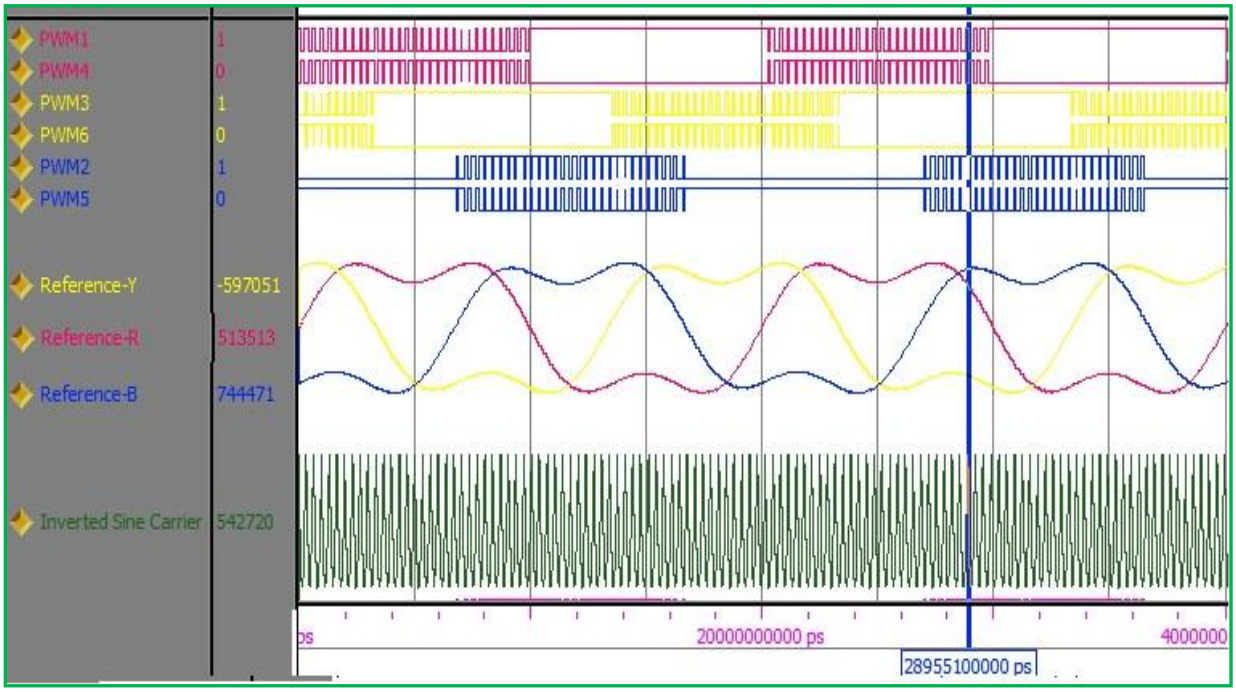

Fig 4. Modelsim simulation of proposed PWM method at modulation index m_a=0.8

A. Comparator and Dead Time Insertion Block

In this zone, the comparison between sine reference and inverted sine carrier has been taken which will decide the intersection point between two waveforms. This intersection will decide the ON and OFF of the inverter switches. Dead time insertion is used to avoid the shoot through fault between same leg switches in the three phase power circuit. 3.0 µseconds dead time has been inserted between switching.

This design occupies 100 LUTs out of 9312 in the targeted device. Combinational logics are occupied 1% of LUTs. Modelsim6.66 has been used for simulation of VHDL design. The simulation Waveform shown in Fig 4.The FPGA design of planned method is implemented and Cosimulated with MATLAB and the outcomes are summarized in next section.

IV. MATLAB-MODELSIM SIMULATION AND HARDWARE RESULTS

The proposed method is incorporated with three phase inverter (without filter) and the DC power is converted to AC power for three phase induction motor by using MATLAB R2015a shown in Fig 5. Three phase inverter receiving the gate pulses through HDL-cosimulation tool box from Modelsim6.6d.

In Simulink "powergui ->tools-> FFT Analysis" has been used to measure the fundamental voltage and THD line voltage. One 50 Hz fundamendal wave has been chosen for FFT analysis.In FFT has the option to select multiple number of waves for measuring THD and fundamental. 600 DC supply has been provided for DC input of the three phase inverter. ODE45 (Dormand prince) solver has been used for FFT analysis (ODE45 is regularly the function of choice among the ODE solvers. It matches methods of orders four and five to guesstimate error and determine step size. ODE45 is so accurate that its default behaviour is to use its interpolant to afford results at in-between points).The primary goal of the PWM is to regulate the fundamental component of the PWM waveform with respect to the applied DC voltage. This control on the fundamental component isexpressed in terms of a measure called modulation index (ma). Higher the value of "ma" lower will be the relative harmonic content. As ma decreases, there will be an increase in the relative harmonic content. The modulation index is defined as

$$m_a = \frac{V_1}{V_{dc}} \qquad (2)$$

where V1 is the peak value of the fundamental amplitude of the PWM waveform; Vdc the value of the applied input dc to the inverter.

The THD is demarcated as the fraction of the sum of the powers of all harmonic components to the power of the fundamental frequency component. The distortion of voltage/current waveforms can be measured by using THD formulation and give as

Fig 5. Three Phase Inverter design in MATLAB Simulink

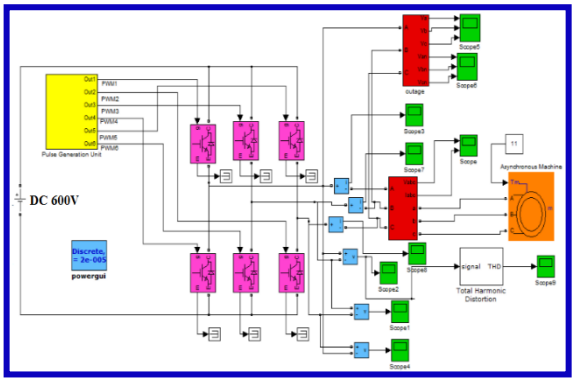

Table 1. Comparison of Fundamental and THD of predictable and proposed method.

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m_a	Parameters	Conventional Methods			Proposed Method
		sine reference			sine reference +3rd harmonic
		Triangle carrier	Inverted Sine		Inverted Sine
		Carrier Frequency 3 kHz		Carrier Frequency 2-4 kHz	
0.2	Fundamental	105.81	228.2	229.21	232.11
	THD	249.113	151.12	151.42	148.5
0.4	Fundamental	206.89	332.1	334.11	333.91
	THD	164.33	112.36	112.49	110.85
0.6	Fundamental	310.78	409.91	408.8	417.4
	THD	121.18	91.17	91.18	88.9
0.8	Fundamental	413.71	486.11	486.7	489.10
	THD	91.9	74.1	73.47	72.6
1	Fundamental	516.2	555.6	553.61	561.9
	THD	69.13	59.93	59.2	57.91
`1.2	Fundamental	571	591.51	594.61	612.8
	THD	58.88	51.93	51.63	46.56

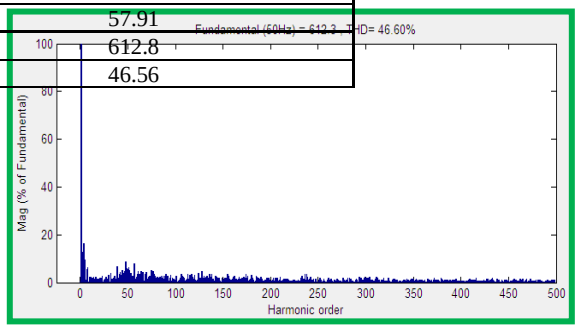

Fig. 7.Line Voltage Spectrum at m_a=1.2

$$\%\,THD = \sqrt{\frac{V_{2(rms)}^2+V_{3(rms)}^2+\cdots+V_{n(rms)}^2}{V_{1(rms)}^2}} \qquad (3)$$

where, V_1 is the root mean square (rms) value of fundamental amplitude of the output voltage and V_2, V_3,... are therms value of second, third harmonics.

Table 1 compares the Fundamental and THD of the conventional and proposed method from the modulation index 0.2 to 1.2. Table 1 depicts that the fundamental voltage of the proposed method is maximum from modulation index from 0.2 to 1.2 when compared with other conventional method. Interestingly, the basic SPWM method is giving less than half of the voltage while comparing with inverted carrier methods. This is clearly indicates the improvement of inverted sine carrier over triangle carrier. The fixed frequency/deterministic inverted sine carrier is also giving good performance over the fixed frequency trianglecarrier SPWM, even though, the harmonics are not accumulated at the multiples of the switching frequency which degrading the performance.But, When three phase inverter performanceis improved little bitwhile usingnondeterministic carriers (2-4 kHz).

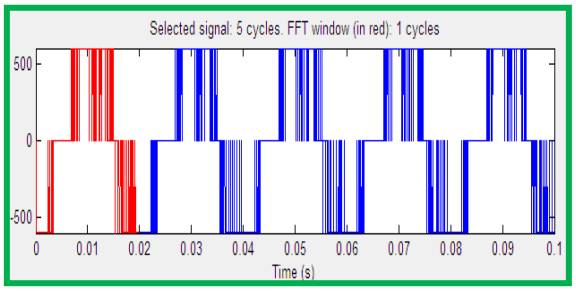

Fig. 6.Line Voltage of Proposed Method at m_a=1.2

The carrier frequency is randomly selected by using linear feedback shift register method. The improvement of third harmonic injected inverted sine carrier PWM is pronounced well from the modulation index 0.2 to 1.2 not only based on the fundamental voltage also based on the THD which are shown in table 1. FPGAs are a impeccable apt for many power sector engineering for power transformation due to its programmable nature. Seamless Configurable Logic Blocks(CLBs) are interconnected together by programming, which are form as a FPGA. The functionality requirements of a particular application can be breakthrough by FPGA programming. The FPGAs can be reconfigured at any point of time or can be make it as an one time programmable (OTP) device. FPGAs allow designers to alteration their plans last stage of the design development even after the end artefact has been manufactured and positioned in the arena. In addition, Xilinx FPGAs allow for field expansions to be completed remotely, eradicating the costs linked with re-designing or physically modernizing electronic systems [8]-[12]. The FPGA Utilization summary has been shown in Table 2. The static timing analysis of the FPGA design is performed by Timing analyzer, which is one of the product of FPGA manufacturer.

The combinational and sequential design timings are verified by using this tool and also this tool verifies setup time and hold time violations. The Place and Route of FPGA design is completed done by using FPGA synthesis tool called Project navigator. The increase in density and performance of FPGAs has resulted in an upsurge in power paid by the FPGA. Once the device has powered up, there are two main components to power consumption. 1. Static power: Primarily transistor leakage current. 2. Dynamic power: Switching in the FPGA core and I/O and determined by CV2f. In this proposed design consumes 105 mWatts. XPowerEstimator(XPE) tool has been used estimate the power dissipation of the design in the FPGA.

The Floor planning is the procedure of finding building blocks that should be placed adjacent together, and assigning space for them in such a way as to meet the sometimes differing goals of existing space, requiredperformance, and the aspiration to have the whole thing close together. Within the Xilinx chips it is habitually the case that the tiniest area design is also the supreme performance design. This wingsin the face of many design procedures, where area and speed are painstaking to be things that should be operated off against each other. The reason this is so is possibly because there are inadequate routing resources, and the more routing resources that are used, the sluggish the design will operate. Optimizing for minimum area authorisations the design to use less resources, but also agrees the sections of the design to be closer together. This leads to littler interconnect distances, less routing resources to be used, quicker end-to-end signal paths, and even faster and steadier place and route times.

Fig. 8. Shows the floor plan of the proposed FPGA design. This scheme has been inspected with the intended arrangements consists of inverter drive and FPGA.The inverter drive incorporated with diode rectifier module along with auto transformer and three phase induction motor which is shown in Fig. 8. Yokogawa Digital Storage oscilloscope will be used for all the inverter output measurements. The combination of auto transformer and rectifieris providing a DC voltage of 600 V to the inverter. As elucidated in previous sections that the traditional and proposed schemes PWM signals have been engendered by FPGA. The shoot through fault has been eliminated by providing the 4.0 µSeconds between the same leg switches, which is incorporated in the VHDL design itself. The PWM pulses and three phase hardware results are shown in Fig 10 and Fig. 11.

The proposed and conventional schemes are examined with the fundamental voltage frequency at 50 Hz. All the hardware results are examined from m_a ranges from 0.2 to 1.2. Fig. 16 shows the hardware spectrum of line voltage at ma=1.2. The fundamental voltage, THD of the ISCPWM is 612 Volts, 46 % respectively, which are the evidence of the proposed scheme.

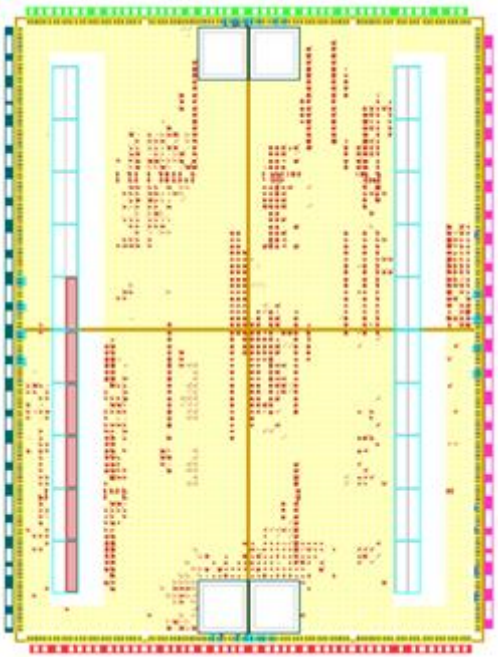

Fig.8. Floor plan of proposed PWM FPGA design

Fig. 9.

Experimental Setup

Table 2.Utilisation of FPGA Resources summary

XC3S500EResource Utilization Summary			
Logic Utilization	Used	Available	Utilization
No. of Slices	914	4656	20%
No. of Slice Flip Flops	652	9312	7%
No. of 4 input LUTs	1594	9312	17%
No. of Bonded IOBs	8	232	3%
No. of MULT18X18SIOs	9	20	45%
No. of GCLKs	4	24	17%

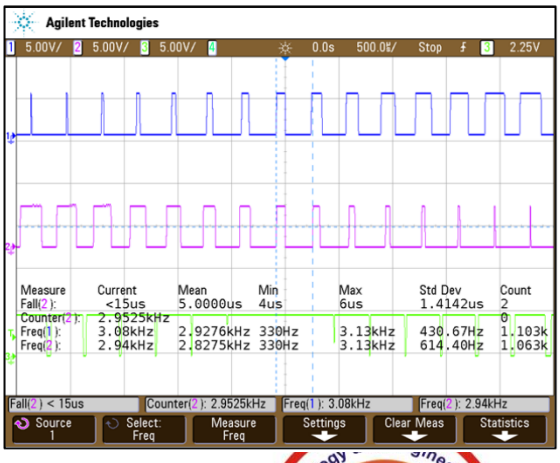

Fig. 10. PWM pulses in Agilent Digital storage oscilloscope

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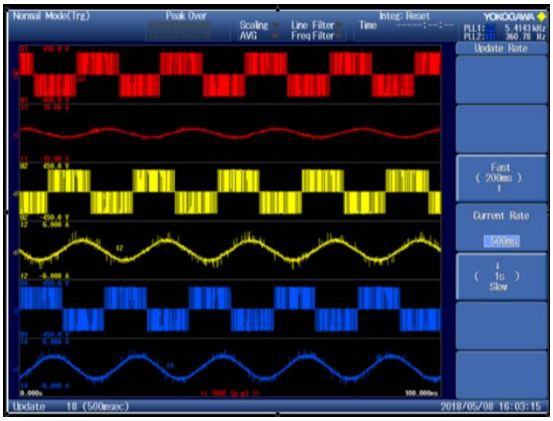

Fig. 11.

Three phase line voltage and current

Fig. 12. Experimental results of Harmonic spectrum for line voltage, m_a=1.2

V. CONCLUSION

In this article presents the varies styles of MATLAB and FPGA design to control three phase induction motor by using new third harmonic injected sine PWM with randomized inverted sine carrier for three phase VSI circuits. Table I précises the proportional performance of both the conformist and proposed PWM method. The simulation model of the inverter circuit is accomplished with PWM switching pulses generating by Modelsim FPGA simulator for various modulation index. In Table 1 says that as modulation index increases the fundamental voltage increases as expected but the method exhibits the double of the fundamental as compared with conventional method from the lower level of modulation indexes. The line-line voltage and the corresponding spectrum are shown in Fig 6, Fig. 7 and Fig 11 and Fig. 12 both simulation and hardware results respectively. The FPGA performances are analysed and given in section 4. The over FPGA designs are dissipates 105 mWatts including both static and dynamic power dissipation. This design elapsed the maximum of 18 ns.

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[1]**SREEJA P** received her B.Tech Electrical and Electronics Engineering from T.K.M College Of Engineering , Kollam, Kerala , India on 2008 and M.E Control and Instrumentation from Anna University, Tamilnadu, india in 2011. At present she is pursuing her Doctoral degree in the depart of EEE at Noorul Islam center for higher education, Thukalay, Tamilnadu, India.

[2]**Dr.L.Padma Suresh** received his B.E. Electrical and Electronics Engineering from Noorul Islam College of Engineering on 1999 and M.E. Process Control and Instrumentation in 2000 from Annamalai University and Ph.D. Electrical Engineering in 2010 from Dr.M.G.R University and Ph.D Computer Science Engineering from M.S. University. Presently he is working as Principal of Baselios Mathews II College of Engineering , Kollam, Kerala. He has 18years of diverse experience in teaching , Life member of ISTE, and Senior IEEE Member. His Research interests in Artificial Intelligence, Control Systems , Power Electronics and Image Processing.

[3]**Dr.P. Muthukumar** received his B.E. Electrical and Electronics Engineering from Noorul Islam College of Engineering on 1999 and M.E. Power Electronics and Drives in 2005 from Anna University and Ph.D. Electrical Engineering in 2017 from Anna University, Chennai-India. Presently he is working as an Associate Professor in EEE Dept. of PVP Siddhartha Institute of Technology, Vijayawada-India. He has 16 years of diverse experience in teaching and corporate industry and a member of IEEE and ISRD. His Research interests in Renewable Energy Sources, Power Electronics and Drives and VLSI.