Frequency Scaling Based Low Power ORIYA UNICODE READER (OUR) Design ON 40nm and 28nm FPGA

Amanpreet Kaur, Keshav Kumar, Amanpreet Sandhu, Amandeep Kaur, Abhishek Jain, Bishwajeet Pandey

Abstract— In the past, it was observed that at among all the 22 languages oriya script is also most vibrant and has been used across the entire country by Oriya community. Oriya Unicode reader is used for decoding the languages used in Indian states of Orissa. In our work we are implementing an energy efficient Oriya Unicode reader. This experiment is done on Xilinx 14.2 ISE Design Suit software for 28nm FPGA platform and results are being compared with 40nm FPGA. We have scaled the frequency of Unicode reader from 1THz to 1MHz. On comparison between 40nm and 28nm FPGA, it was observed that 28nm FPGA consumes least amount of power when operated at 1MHz-1THz frequency using SSTL18_I IO standard.

Keywords—Oriya Unicode Reader, Energy Efficient Design, FPGA,Frequency Scaling, Virtex 6,Artix 7.

1. INTRODUCTION

Gradually energy and power requirements are expanding throughout the world. Population growth and industrialization are the main causes of energy and power crisis. Considering all the aspects of engineering design, the following analyses have been done on Oriya Unicode Reader in order to develop an energy economical style that consumes less power as compared to the other Unicode Readers that are prevailing around these days. Similar analysis has also been done on Punjabi, Devnagri, Malayalam, and Gurumukhi Unicode Reader in order to create energy and power efficient devices [1-5]. Devanagari is a script of India, spoken by more than five hundred million folks. Previously Devnagari is employed as script of Gujarati and currently it is used to write Hindi, Sanskrit, Marathi, Sindhi. The Oriya Unicode includes 16-bit hexa codes for freelance vowels, dependent vowels, constants and completely unsimilar signs. During this experiment, the energy ability is analyzed at various range of frequencies at 28nm (Artix-7) and 40nm (Virtex-6) FPGA. Many other energy saving methodology such as voltage scaling[6], frequency scaling [7], change in IO standards [8], thermal scaling[9], capacitance scaling[10] used for energy efficient devices.

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2. EXPERIMENTAL SETUP

Fig. 1. shows Oriya Unicode Reader, this takes 16-bit data and a clock signal (c1) as a input and it diffentiates input in following category: dependent vowel, digit, digit sign , fraction sign, consonant, not valid sign, independent vowel, or some other sign in the range of Oriya script.

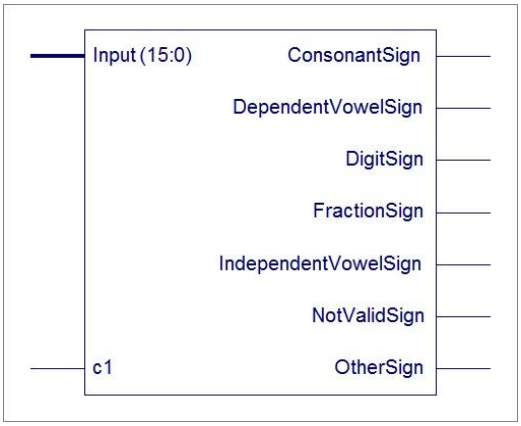

Fig.1: Schematic of Oriya Unicode Reader (OUR)

3. ENERGY EFFICIENT TECHNIQUES

3.1 Frequency Scaling:

In this work we have scaled down the frequency from higher level 1THz to lower level 1MHz. Seven different value of frequency has been taken to analyzethe power consumption of Unicode Reader. The different frequency which has been taken is shown in Fig. 2.

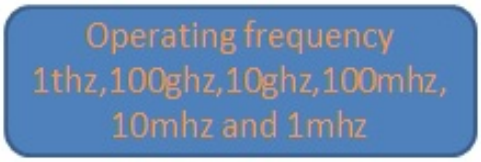

Fig.2: Different range of frequencies

3.2 FPGA Technology

As technology is improving day by day, now we can clustere millions and billions of transistor from a very few thousand of transistor which we can be clustered in past. In Fig. 3, we tend to analyze our device at two FPGA technology that are 40nm Virtex 6 FPGA and 28nm Artix 7 FPGA. Power analyzed is done for both FPGA and the FPGA which consumes the least amount of power is taken in account.

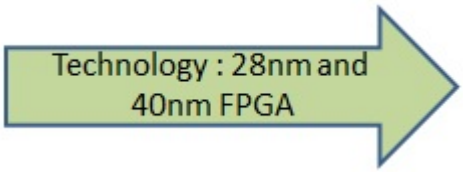

Fig.3: Different FPGA technologies`

4. POWER ANALYSIS & RESULTS

4.1 Clock power analysis

The amount of clock power dissipated when the device frequency is set for various frequencies in Artix 7 and Virtex 6 FPGA technologies is shown in Table 1 and Fig. 4.

Artix-7 Analysis: Figure 4 and Table 1 indicates that almost 100% of power can be saved if device is operated at a frequency of 1 MHz, 10 MHz and 100 MHz. Not only that 97.24% of power can be saved if the device operates at 10 GHz, instead of 1THz and 99.00% power can be saved if the device operates at 100 GHz instead of 1THz.

Virtex-6 Analysis: Figure 4 and Table 1 shows that almost 100% power can be saved if device operates at a frequency of 1 MHz , 10 MHz, 0.1000 MHz and 1000 MHz . Also 99.89% of power can be saved if the device operates at 1000 MHz instead of 1THz and 99.00% power can be saved if the device operates at 10 GHz and 100 GHz instead of 1THz.

Table 1: Clock power analysis of Virtex-6 and Artix-7

FREQUENCY (Hz)	TIME (ns)	ARTIX7 (W)	VIRTEX6 (W)
1 MHZ	1000 NS	0.0001	0.0001
10MHZ	100 NS	0.0001	0.0001
100 MHZ	10 NS	0.0001	0.0001
1000 MHz	1 NS	0.0001	0.0001
10 GHZ	.1 NS	0.002	0.003
100 GHZ	.01 NS	0.01	0.013
1 THZ	.001 NS	0.008	0.109

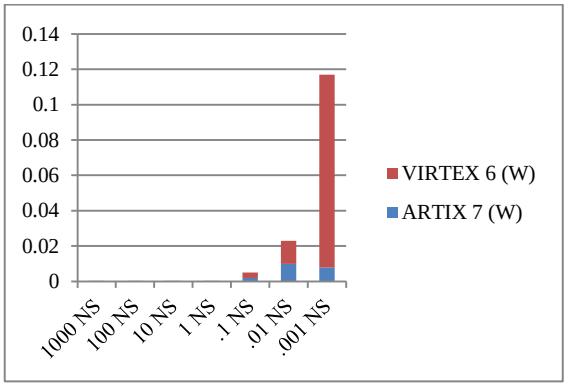

Fig. 4: Graph showing power analysis between Virtex 6 and Artix7

4.2 Logic Power Analysis

The amount of Logic power dissipated when the device is operated at various operating frequencies on Artix 7 and Virtex 6 FPGA family is shown in table 2 and figure 5.

Artix-7 Analysis:Figure 5 and Table 2 shows that almost 100% power can be saved if device operates at a frequency of 1 MHz , 10 MHz. 99.98% of power saved if the device operates at 0.1000 MHz and 1000 MHz instead of 1THz and 89.99% power can be saved if the device operates at 100 GHz in case of 1 THzinstead of 1THz.

Table 2: Logic power analysis of Virtex 6 and Artix7

FREQUENCY (Hz)	TIME (ns)	ARTIX 7 (W)	VIRTEX 6 (W)
1 MHZ	1000 NS	0.0001	0.0001
10MHZ	100 NS	0.0001	0.0001
100 MHZ	10 NS	0.001	0.003
1000 MHz	1 NS	0.006	0.033
10 GHZ	.1 NS	0.057	0.336
100 GHZ	.01 NS	0.571	3.357
1 THZ	.001 NS	5.708	33.573

Virtex-6 Analysis: Figure 5 and Table 2 that almost 100% power can be saved if device operates at a frequency of 1 MHz , 10 MHz. Also 99.99% of power can be saved if the device operates at 0.1000 MHz and 1000 MHz instead of 1THz and 98.9% power can be saved if the device operates at 10 GHz and 90% at 100 GHz instead of 1THz.

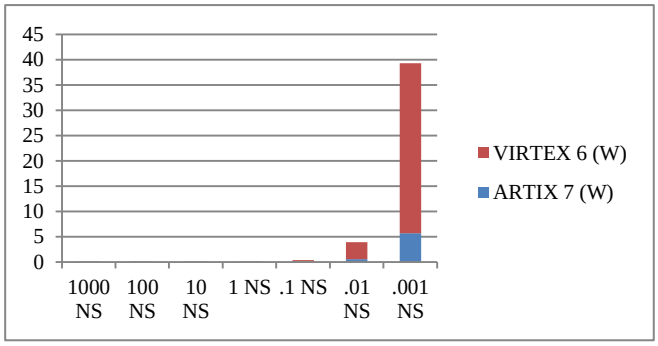

Fig.5: Logic power analysis between Virtex 6 and Artix7

4.3 Signals Power Analysis

The amount of Signal power dissipated when the device is operated at different frequencies on Artix 7 and Virtex 6 FPGA technologies is shown in table 3 and figure 6.

Artix-7 Analysis: Figure 6 and Table 3represents that almost 100% power can be saved if device operates at a frequency of 1 MHz , 10 MHz and 100 MHz. Also 99.91% and 98.96% of power can be saved if the device operates at 1000 MHz and 10 GHZ instead of 1THzand 89.95% at 100 GHzinstead of 1THz.

Table 3: Signal power analysis of Virtex 6 and Artix7

FREQUENCY (Hz)	TIME (ns)	ARTIX 7 (W)	VIRTEX 6(W)
1 MHZ	1000 NS	0.0001	0.0001
10MHZ	100 NS	0.0001	0.0001
100 MHZ	10 NS	0.0001	0.0001
1000 MHz	1 NS	0.001	0.002
10 GHZ	.1 NS	0.012	0.018
100 GHZ	.01 NS	0.116	0.171
1 THZ	.001 NS	1.155	1.701

Virtex-6 Analysis: Figure 6 and Table 3indicates that almost 100% power can be saved if device operates at a frequency of 1 MHz , 10 MHz and 100 MHz. Also 99.88% and 98.94% of power can be saved if the device operates at 1000 MHz and 10 GHZ instead of 1THzand 89.94% at 100 GHzinstead of 1THz.

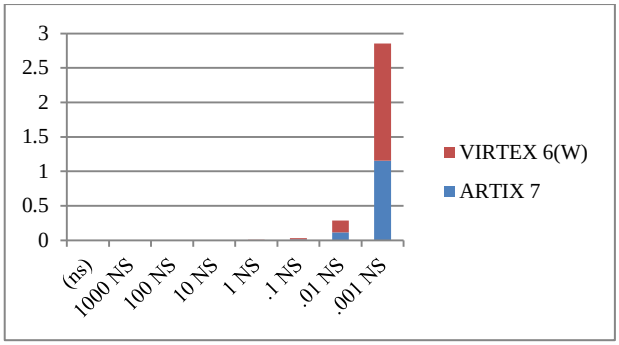

Fig.6: Signal power analysis between Virtex 6 and Artix7

4.4 IO Power Analysis

The amount of IO power dissipated when the device is operated at different frequencies on Artix 7 and Virtex 6 FPGA technologies is shown in table 4 and figure 7

Artix-7 Analysis: As shown in figure 7 and table 4 that almost 100% power can be saved if device operates at a frequency of 1 MHz, 10 MHz. Also 99.99% and 99.90% of power can be saved if the device operates at 0.1000 MHz and 1000 MHz instead of 1THzand 99% and 99.95% at 10 GHz and100 GHzinstead of 1THz.

Virtex-6 Analysis: Figure 7 and Table 4 represents that almost 100% power can be saved if device operates at a frequency of 1 MHz , 10 MHz. Also 99.98% and 99.90% of power can be saved if the device operates at 0.1000 MHz and 1000 MHz instead of 1THzand 98.99% and 89.99% at 10 GHz and100 GHzinstead of 1THz.

Table 4:IO power analysis of Virtex 6 and Artix7

FREQUENCY (Hz)	TIME (ns)	ARTIX 7 (W)	VIRTEX 6 (W)
1 MHZ	1000 NS	0.0001	0.0001
10MHZ	100 NS	0.0001	0.0001
100 MHZ	10 NS	0.002	0.006
1000 MHz	1 NS	0.02	0.059
10 GHZ	.1 NS	0.201	0.591
100 GHZ	.01 NS	0.01	5.909
1 THZ	.001 NS	20.104	59.086

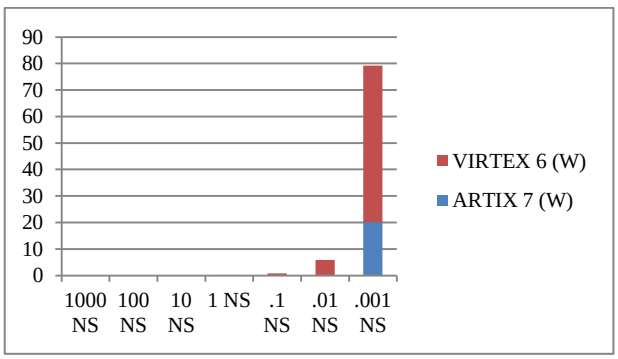

Fig.7: IO power analysis between Virtex 6 and Artix7

4.5 Leakage Power Analysis

The amount of Leakage power dissipated when the device is operated at different frequencies on Artix 7 and Virtex 6 FPGA technologies is shown in table 5 and figure 8.

Artix-7 Analysis: Figure 8 and Table 5 indicates that almost 89.91% power can be saved if device operates at a frequency of 1 MHz , 10 MHz,0.1000 MHz and 1000 MHz . Also 89.92% and 88.43% of power can be saved if the device operates at 10 GHz and 100 GHzinstead of 1THz.

Virtex-6 Analysis: Figure 8 and Table 5 represents that almost 20.82% power can be saved if device operates at a frequency of 1 MHz , 10 MHz and 100 MHz. Also 20.69% and 19.53% of power can be saved if the device operates at 1000 MHz and 10 GHz instead of 1THzand 5.4% at 100 GHzinstead of 1THz.

Table 5: Leakage power analysis of Virtex 6 and Artix7

FREQUENCY (Hz)	TIME (ns)	ARTIX 7 (W)	VIRTEX 6 (W)
1 MHZ	1000 NS	0.082	1.293
10MHZ	100 NS	0.082	1.293
100 MHZ	10 NS	0.082	1.293
1000 MHz	1 NS	0.082	1.295
10 GHZ	.1 NS	0.083	1.314
100 GHZ	.01 NS	0.094	1.544
1 THZ	.001 NS	0.813	1.633

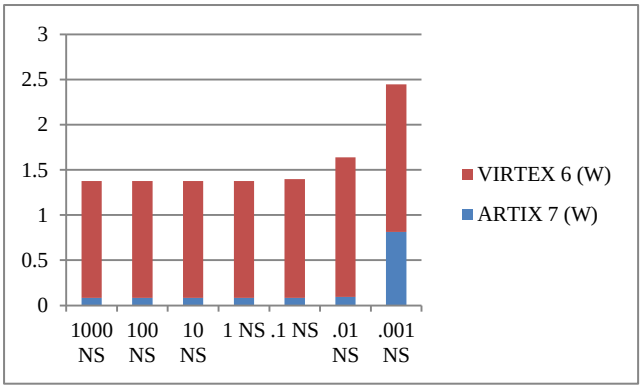

Fig.8:Leakage power analysis between Virtex 6 and Artix7

4.6 Total Power Analysis

The amount of Total power dissipated when the device is operated at different frequencies on Artix 7 and Virtex 6 FPGA technologies is shown in table 6 and figure 9.

Artix-7 Analysis:Figure 9 and Table 6 shows that almost 99.70% power can be saved if device operates at a frequency of 1 MHz and 10 MHzAlso 99.69% and 99.60% of power can be saved if the device operates at 0.1000 MHz and 1000 MHz instead of 1THzand 98.72% and 97.12% at 10 and 100 GHzinstead of 1THz.

Virtex-6 Analysis:Figure 9 and Table 6shows that almost 98.65% power can be saved if device operates at a frequency of 1 MHz and 10 MHz Also 98.64% and 98.55% of power can be saved if the device operates at 0.1000 MHz and 1000 MHz instead of 1THzand 97.64% and 88.56% at 10 and 100 GHzinstead of 1THz.

Table 6: Total power analysis of Virtex 6 and Artix7

FREQUENCY (Hz)	TIME (ns)	ARTIX 7 (W)	VIRTEX 6 (W)
1 MHZ	1000 NS	0.082	1.293
10MHZ	100 NS	0.082	1.294
100 MHZ	10 NS	0.085	1.302
1000 MHz	1 NS	0.11	1.389
10 GHZ	.1 NS	0.356	2.261
100 GHZ	.01 NS	0.802	10.994
1 THZ	.001 NS	27.868	96.102

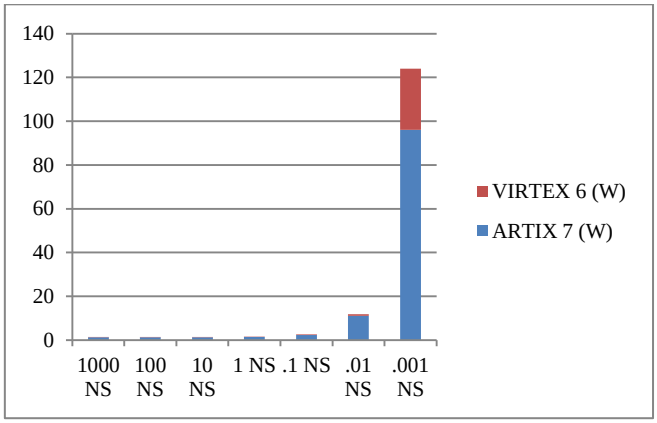

Fig.9: Total power analysis between Virtex 6 and Artix7

5. CONCLUSION

In our work it is observed that there is an excellent savage in total power consumption, if we have a tendency to scale down the frequencies from 1THZ to 1MHZ. Rather than using 40nm technology FPGA, we can use 28nm technology FPGA for better power saving.Hence we can conclude that maximum amount of power (static similarly as dynamic) savings can be achieved by operating the device at a frequency of 1MHZ and Artix-7 (28nm) FPGA technology.

6. FUTURE SCOPE

The Oriya Unicode reader is implemented on Virtex-6 and 28nm FPGA for our proposed methodology. Therefore, this reader can be analyzed on 20nm ultra scale FPGA, 14nm FPGA, System on Chip (SOC) and 3D ICs. Here 6 and 7 series of FPGA's have been used. We can further implement Unicode reader on Lattice FPGA, SEcube and FPGA Families other than Xilinx. This Unicode reader is intended for Oriya. In future, we will work for unicode reader of other twenty one official languages of India. Another energy economical techniques like electrical phenomenon, thermal scaling, capacitance scaling and clock gating can even be used for Oriya language.

REFERENCES

1. B.Pandey et. al. "Simulation of HSTL IO standard based energy efficient Punjabi Unicode reader on FPGA" IEEE International Conference on Computational Intelligence and Communication Networks,(CICN) 2014.
2. T.Das, et al, "Low Power Devnagari Unicode Checker Design Using CGVS Approach", International Conference on Recent Advances in Mechanical Engineering and Interdisciplinary Developments (ICRAMID), 2014, Kanyakumari, India.
3. A.Kaur, et al, "SSTL IO Standard Based Tera Hertz & Energy Efficient MALAYALAM Unicode Reader Design and Implementation on FPGA", In Special Edition of "Managing Information Technology", Vol.6, No.48, 2015.
4. N. Kaur et al, "LVCMOS IO Standard Based Low Power Devanagari Unicode Reader on FPGA", In Special Editionof "Managing Information Technology", Vol.6, No.39, February, 2015.
5. A.Kaur, et al, "Thermal aware energy efficient GurmukhiUnicode Reader for Natural Language ", 9th INDIACom IEEE Conference , 11th-13th March, 2015.
6. S. M. M. Islam, et. al. "Simulation of Voltage Scaling Aware Mobile Battery Charge Controller Sensor on FPGA", "Advanced Materials Research", ISSN:1022-6680, Vol. 893 (2014) pp 798-802, February 2014.
7. R. Kaur, S. M. M. Islam, T. Kumar, B. Pandey, M. M. E. Noor and S. M. T. Siddiquee, "Frequency Scaling Based Energy Efficient Mobile Battery Charge Controller Sensor Design on FPGA", "Advanced Materials Research", Modern Achievements and Developments in Manufacturing and Industry, Vol. 984 - 985, pp. 1057-1062.
8. S.Gargrish et al, "IO Standard Based Energy Efficient Devanagari Unicode Reader on 28 nm FPGA",In SpecialEdition of "Managing Information Technology", Vol.6, No.39, 2015.
9. A.Uddin, et al. "Thermal aware energy efficient Bengaliunicode reader in Text analysis.", International Conference on. IEEE Optimization, Reliabilty, and Information Technology (ICROIT), 2014.
10. A.Kaur, et al, "Capacitance Scaling Based GurmukhiUnicode Reader Design for Natural Language Processing", ",9th INDIACom IEEE Conference , 11th - 13th March,2015.

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