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Study and Analysis of 3 -Input Logic Gates By using Quantum Dot Cellular Automata

G Surya Kranth, D Naveen Sai, R. S. Ernest Ravindran

Abstract*: Quantum dot cellular automata (QCA) is growing technology with Nano range scale in that, QCA is extremely computational and exceptionally productive than CMOS technology. QCA the parameters like area and usage of power are very less when compared to CMOS technology. In the comparative analysis of QCA and CMOS technologies, the number of quantum cells used and the number of transistors taken place to design 3 input logic gates. In this paper, it explains about the comparison between CMOS and QCA technologies for 3 input basic logic gates like AND, OR, NOT, NAND, NOR ,XOR and XNOR by utilizing the ultra -low power and the area, time taken to outline the circuit with quantum dot cells in QCA technology. From the results, area utilized to design logic gates using by QCA technology as compared to CMOS technology is reduced up to 5%.

Index Terms*: Quantum Dot Cellular Automata, QCA Wire, Majority Gate, Logic Gates.

I. INTRODUCTION

CMOS technology to design any transistor it takes more time as well as high power and area usage are required, to overcome a problem QCA is the alternative technology to reduce the parameters like area and ultra-low power is used to outline the logic or any design. It is the upcoming strategy with Nano range scale to help for the different quantum circuits. QCA is the alternative method to design any circuits. It is proposed by the change on alternate methods of computer-based design, which has been conceived in similarity to different methods of cells automata presented by Von Neumann. QCA it has four quantum dots and it is arranged in the square pattern, so it is considered as one quantum cell .In QCA there are four dot cells in that the two dot cells are electrons and holes and they are placed diagonally to each other because of the Columbic repulsion to each other of dot cells [9].In QCA there are two different polarizations. In that polarization if P= +1 it is represented as binary 1 and if p= -1 then it is represented as binary 0 as represented in Fig. 1 (b). By setting the polarization tunnel effect occurs at adjacent cells to propagate the signal from one to another location. For the different quantum dot of cell, there are different binary digits for polarization and to get the polarization value in QCA there is a mathematical expression, which is represented below [1-3].

$$P = \frac{(P_1+P_3)-(P_2+P_4)}{P_1+P_2+P_3+P_4} \quad (1)$$

From the above equation where p stands for polarization in QCA, whereas p1 is polarization of 1st dot , p2 is polarization of 2nd dot , p3 is polarization of 3rd dot and p4 is polarization of 4th dot in QCA to get the accurate result of the circuit and as well as waveform to the circuit[7].

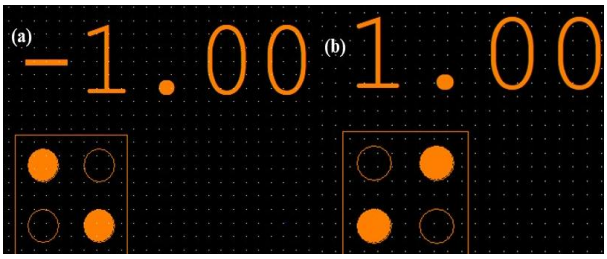

Fig. 1(a) P= -1 (Binary 0), (b) P= +1 (Binary 1)

In the individual technology, it comprises of four distinct clocks and three unique styles of dot cells. QCA there are three different styles they are normal dot cell, crossover dot cell, and vertical dot cell and there are four different colors for dot cells as shown in Fig 2 as they are present in designing of large circuits in QCA [5].

II. EXISTING METHOD OF CMOS LOGIC GATES

CMOS technology to outline any circuit utilizing the transistor to play out the capacity. To plan any application like full adders, different decoders and mux by utilizing the logic gates and transistors for outline any circuit. In this innovation, it is involving the substantial zone and more power utilization to plan the logic gate and different applications. Here actualized for the three information CMOS outlined for AND, OR, NAND, NOR by utilizing more region and more power [8].

A) NOT Gate

The inverter or NOT gate can be actualized in CMOS by symbol. It is the fundamental gate, yet this configuration require high power and region. Furthermore, the operation is y=y'.

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***** Correspondence Author
G. Surya kranth*, Electronics and communication, Koneru Lakshmaiah Education Foundation, Khammam, India.
D. Naveen Sai, Electronics and communication, Koneru Lakshmaiah Education Foundation, Guntur, India.
Dr.R.S. Ernest Ravindran Electronics and communication, Koneru Lakshmaiah Education Foundation, Vijayawada, India.

B) 3 -Input AND Gate

The articulation for the three info AND gate is Y=A.B.C. at the point when three input sources are having same input 1 then the output is 1 and the rest of the cases it represents as 0. According to the logic diagram and expression of the AND Gate when the two inputs are having the value 1 then output will be 1 and remaining cases it will act as 0.

C) 3 -Input OR Gate

In the 3 input OR gate when one of the input is having value 1 at that point output will be as 1. When one of the input sources are 0 at that point output will be zero Y=A+B+C. According to the logic diagram and expression of the OR Gate when the two inputs are having the value 0 then output will be 0 and remaining cases it will act as 1.

D) 3- Input NAND Gate

In the outline of NAND gate about the information as A, B, C, and output as Y. In NAND gate, the operation is the reverse of AND gate and the articulation is given below. According to the logic, diagram and expression of the NAND Gate when the two inputs are having the value 1 then output will be 0 and remaining cases it will act as 1.

E) 3 -Input NOR Gate

In the outline of NOR gate is about the information values as A, B, C, and output as Y. In NOR gate, the operation is reverse of the OR gate and hence the articulation is given as below. According to the logic, diagram and expression of the OR Gate when the two inputs are having the value 0 then output will be 01and remaining cases it will act as 0.

F) 2 -Input XOR Gate

The XOR logic gate (occasionally EOR, or EXOR and articulated as Exclusive OR) is a digital logic gate that gives an exact (1 or HIGH) output when the number of input odd. A XOR gate actualizes an obstructive or; that is, a genuine output results in the event that one, and just a single, of the contributions to the logic gate is valid. In the event that the two sources of info are false (0/LOW) or both are valid, a false output results. XOR tells to the imbalance work, i.e., the yield is valid if the information sources are not alike generally the output is false. An approach to recall XOR is "either yet not both".

When A = 0, B=1 Switch is open &when g=1, B=0 Switch is shut. So at the point when g=1 : whenever input is '0' at that point output will be powerless '0' and whenever input is '1' at that point output will be solid '1'.

G) 2 -Input XNOR Gate

A XNOR gate (once in a name, Selective NOR gate) is an advanced logic gate with at least two sources of input and one output that performs coherent correspondence. The output of a XNOR gate is genuine when the majority of its information sources are valid or when the majority of its data sources are false. In the event that a portion of its sources of input are valid and others are false, at that point the output of the XNOR gate is false.

When A = 0, B=0 Switch is open &when g=1, B=1 Switch is shut. So at the point when g=1: whenever input is '0' at that point output will be powerless '1' and whenever input is " at that point output will be solid '0'.

III. PROPOSED METHOD OF QCA

Wire crossing QCA

Array of QCA cells can be arranged to perform wire and all logic functions. Instead of the normal metal wire, the QCA wire is utilized to develop an advanced logic circuit. In a QCA wire, the paired signals stimulate from contribution to output in light of the electrostatic collaborations between the cells. There are two types of QCA wires as shown in Fig 3 (a) and Fig 3(b). One is a binary wire executed with cells of 90º and the other is a reverse chain executed with the cells of 45º [6].QCA circuit can be efficiently built by using the majority gate and inverters. The simplest structure of the inverter is usually formed by placing the cells only with their corners touching. In this 45 º, displacement in the two lines of merging cells produces the complement of the input signals. In coplanar wire crossing, cells situated at 90º and 45 are utilized. In any case, producing Nano-scale cells with two unique introductions is a testing mission. Moreover, over the top wire-crossing structures may influence the capacity of the circuit. In this way, it is imperative to limit the number of wire-intersections. QCA crossing is executed by one layer utilized both 45-degree and 90-degree QCA cells, every one dedicated to the other side of an intersection. These unique cells can pass the intersection without any impact on each other [10].

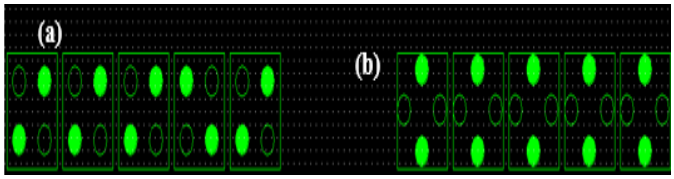


Fig.2 (a) 90º QCA wire, (b) 45º QCA wire

Majority gate QCA

In QCA, majority gate is the key part to outline any circuit and go about as central cell to any circuit configuration as appeared in Fig 11(b). Dominant QCA center as normal cell. The dot cell goes about a halfway from contribution to output to exchange distinctive qualities to get their particular waveforms. In the QCA design configuration, there are different types of majority gates like 3 input and 5 input and n number of inputs and so on. At the point of 3 input majority gate, it consists of 5 cells in that there are 3 input cells and 1 output cell and there will be a central cell. The tendency of the central cell to move a ground state guarantee that it goes up against the polarization of the greater part of its neighbors. The cell will tend take after the majority gate to polarization to go as 0 and 1 as shown in Fig 11(a). As the Columbic, repulsion power of electrons of the information cells are entirely up, the center cell will be changing in accordance with the dominant part of modifying the info association cells. Finally, the output cell modifies the center cell and the after effect of other state in the majority gate can be acquired from the output cell.

Encouraging the high majority gate can be stretched out for the diverse levels and this can be useful for planning different extensive circuits for polarizing the circuits in QCA. Here, in the QCA majority gate are knows as general logic gates of QCA.

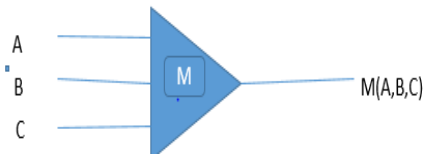


Fig. 3 Block diagram Majority gate

This majority gate frames the essential building square to execute different logic gates in QCA circuits. For instance, if the info given to greater part entryway is "001", at that point output is "0" which shows the extreme digit redundant in the information. Similarly, for input "111", output of dominant part is "1" etc. As a rule, the dominant part takes contributions to odd number, to create an output. [4] A two dimensional QCA cell, allows just three sources of input (for example, two cells for input and one cell for control) and reduces one output given that there are just four headings. Expansions to three dimensions will allow further extra data sources. In addition, for some math applications, three contributions to QCA appear to be fitting.

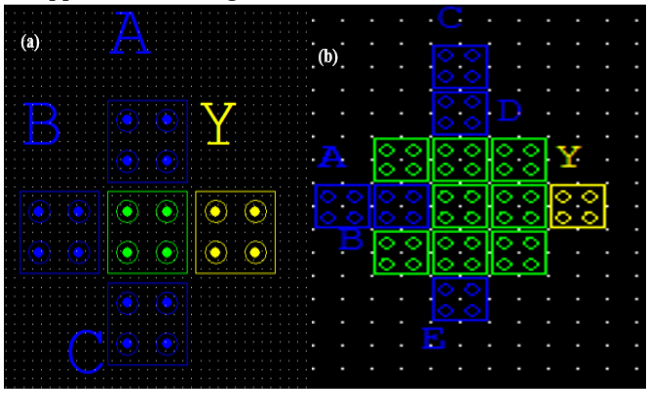


Fig .4(a) 3- input majority gate, (b) 5- input majority gate

Here there is a case of 5 input majority gate, where 13 dot cells and center cells go about as majority gate. In QCA it can actualize, distinctive composes dominant by lessening and expanding the cell estimate from default to various size according to different circuit necessities. [6]

In further, the QCA technology can be applicable to many applications like logic gates, memories, decoders, arithmetic's operations and different types of MUXs respectively. QCA to outline, any unique circuits or any applications like decoders and memories or others there will be utilization of logic gate. Here, generally the 3 input logic gate with less required dot cells occupies less region. This technology is simple to design any application in less time with less power utilizaion. For the distinctive logic gate, there will be polarized and majority gate utilized as central cell to optimize the waveforms

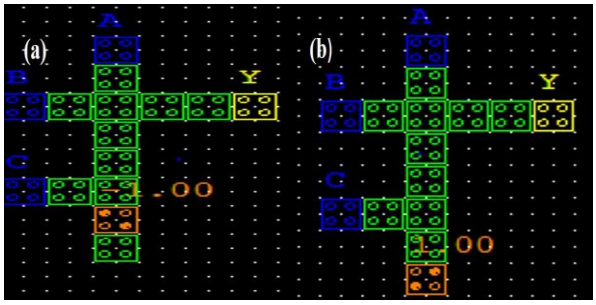
A) NOT GATE

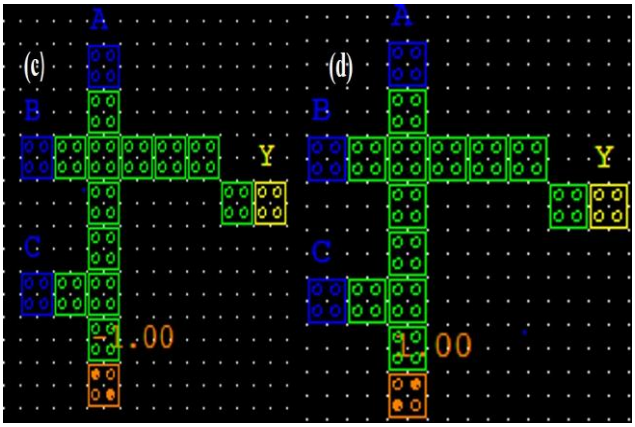
QCA inverter or NOT gate, when the information is having 1 consequently it gives the outcomes as 0. In addition, additionally when input is 0, at that point naturally output is 1. The outline is appeared in the fig (6). Here one of the input is y, which passes the incentive to central cell, and it inclines to some polarizing.

Fig.5 Not Gate

B) 3 Input Logic Gates

The expression for the three information AND gate is Y=A.B.C. at the point when three inputs are having an indistinguishable incentive from 1 then the output is 1 and the rest of the cases as it speaks to be 0. Here considering the 3 distinct information sources and each input has diverse qualities for every situation as they go from the central cell which is the dominant part of the logic gate and their qualities will be captivated to get the improved outcomes. The edge between input A and B is 90 degrees. From the input C and the polarized cell is having 90 degrees. The polarization esteem is - 1. M (A, B, C, 0) = ABC. Here in the OR gate M (A, B, C, 1) = A + B+C and NOR gate, the required polarization value is 1. This will be followed for the remaining logic gates to get the output waveforms. Here in Fig 7 (a) AND gate, (b) OR gate (c) NOR gate, (d) NAND gate.(e)XOR gate,(f)XNOR gate.





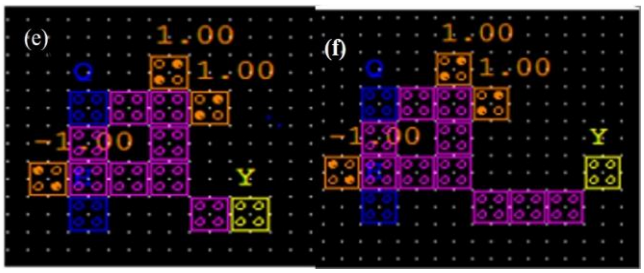
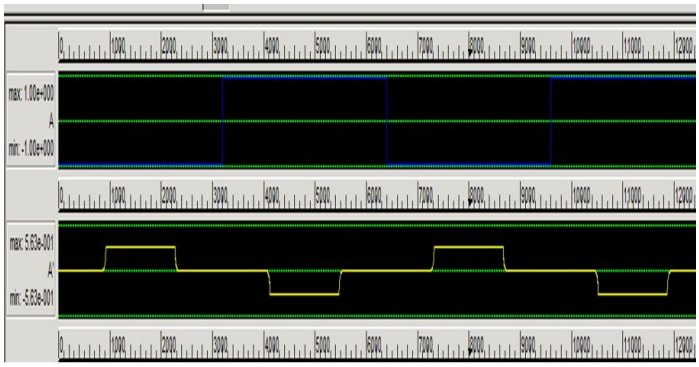


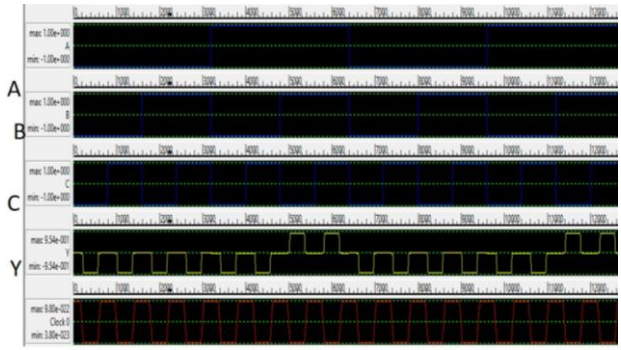
Fig. 6 3- Inputs Logic Gates

IV. RESULTS AND DISCUSSIONS

From the truth table results, the 3input logic gates waveforms are represented below accordingly. Here in the waveform (a) NOT gate, (b) AND gate, (c) OR gate (d) NOR gate, (e) NAND gate (e) XOR GATE (f) XNOR GATE



(a)



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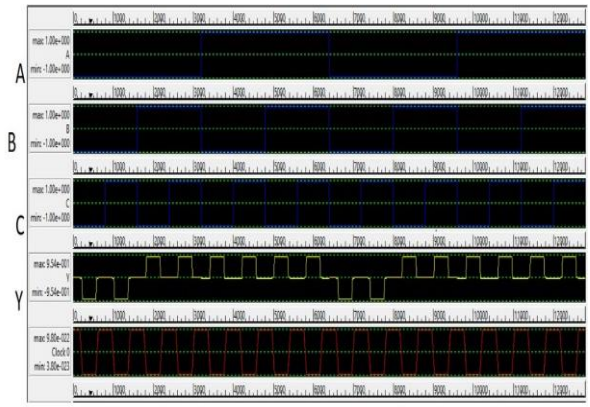

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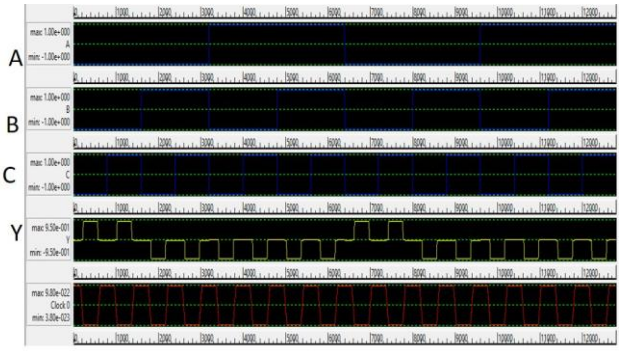

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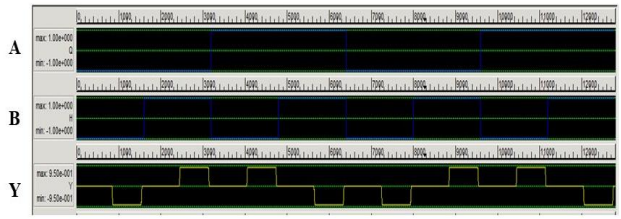

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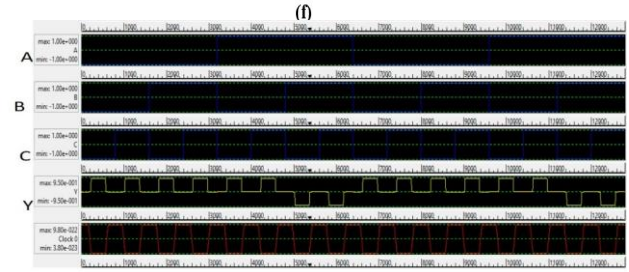
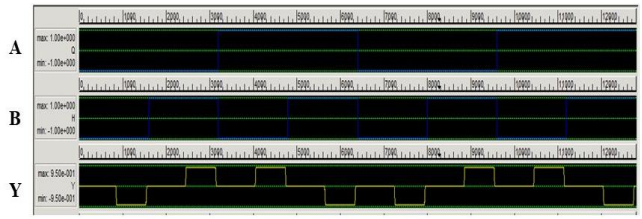


(e)



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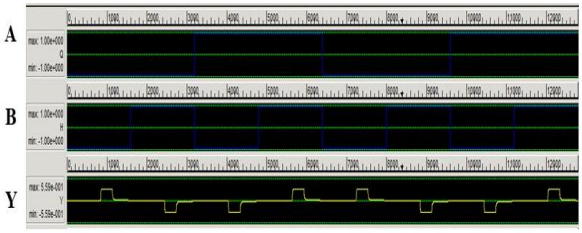

(g)

Fig.7 waveform representation of logic gates

From the above waveforms, QCA additionally designs the logic gates of three inputs getting the output as contrast with the CMOS and DSCH programming. By considering the three input truth table the logic gates are outlined in the QCA designer.

Below table demonstrates the comparison between the CMOS and QCA technology about the area, number of transistors and dot cells utilized in the technology. Here in the CMOS the taking of transistor is less but, the area to design the circuit is large, power utilization is high, and is time taking to outline fundamental logic gates. In QCA, it can execute any outline within less area and less number of required dot cells in the Nano range.

Table 1 Comparison table between CMOS AND QCA

x	Name of the gate	Proposed Method	Existed Method
1	NOT	0.00 μm^2	1.74 μm^2
2	AND	0.02 μm^2	8.125 μm^2
3	OR	0.02 μm^2	8.125 μm^2
4	NAND	0.03 μm^2	8μm^2
5	NOR	0.03 μm^2	8μm^2
6	XOR	0.02 μm^2	6μm^2
7	XNOR	0.02 μm^2	6μm^2

IV. CONCLUSION

Quantum-dot cell automata (QCA) is the new technology at Nano scale circuit configuration level and can be appropriate for various circuits. As the logic gates are more computerized, circuits are fast and less unpredictable with less region to outline. The execution for the QCA utilizing less number of quantum dot cells and limited region. This paper clarifies the change of different logic gates utilizing QCA originator with output execution of different parameters. The significant point of paper is to basic 3 input QCA based with correlation of CMOS technology with parameters like region and number of cells utilized in the QCA. The outcomes are checked with relating truth tables.

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AUTHORS PROFILE

Mr. G. Surya Kranth currently pursuing his master’s degree in VLSI design at klef deemed to be university. He obtained his bachelor’s degree in electronics & communication engineering at Lingayas University. His working area of interest includes digital VLSI design and Nano electronics.

Mr. D. Naveen Sai currently pursuing his master’s degree in VLSI design at klef deemed to be university. He obtained his bachelor’s degree in electronics & communication engineering at RVR&JC. His working area of interest includes digital VLSI design and Nano electronics.

Dr. R.S. Ernest Ravindran received his PhD in 2016 from Anna University, Chennai, India. He is currently working as assistant professor at K L University Vaddeswaram, Guntur, India. He did his Masters in Nanoscience and Technology from Anna University, Trichy, India where he established surface coated CdS quantum dots as a luminescent probe for silver ion detection. His field of research involves nanocomposites (ceramic-polymer) for high-energy storage application, green synthesis of metal nanoparticles in biomedicine applications.