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Modeling and Analysis of Deadbeat Controller Based Split Capacitor Dstatcom for Dc Voltage Regulation

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Abstract*: The Power quality is effected when three phase diode bridge rectifier and star connected load is connected in distribution side. Due to the presence of three phase diode bridge rectifier there are various effects in distribution side such as harmonics, voltage sag, voltage swell, and excessive neutral current. In conventional split capacitor DSTATCOM D.C voltage is fixed and is selected based on its reactive power. Under light loaded conditions reference D.C voltage can't vary as per load requirement so D.C voltage is high. In order to make D.C voltage as constant large number of switches are required because of that switching losses are more due to which power quality is reduced. As switching losses are more an adaptive split capacitor faces a disadvantage i.e., current harmonics. To reduce all above power quality issues a deadbeat controller is used in adaptive split capacitor DSTATCOM is proposed in this paper. It consists of Zero Crossing Detector (ZCD), Unit vector Generation, Terminal Voltage, Deadbeat Voltage control. The MATLAB SIMULINK tool is used for analyzing the performance of deadbeat controller based adaptive split capacitor DSTATCOM control scheme which is used for unbalanced loads to improve power quality.

Index Terms: Adaptive Split Capacitor, Deadbeat controller, Total Harmonic Distortion (THD), unbalanced loads, Voltage stress.

NOMENCLATURE

I_l – Load Current
P_{lavg}- Average Load Power
P_{loss} – Power Loss
V_{pcc} – Voltage across point of common coupling
V_{p0} – Average phase voltage
I_f – Filter current
I_f^* -Reference filter current
V_{inv} – Inverter voltage
X_f – Filter reactance
P_f – Real power of filter
Q_f- Reactive power of filter
I_{fmax} – Maximum filter current
V_{dc} – D.C Voltage
V_{dc}^* - Reference D.C Voltage
m- modulation index
e_{vdc} – D.C voltage error

δ – delta
K_p – Proportional gain
K_i – Integral gain
u- Unit Vector Generation
V_t- Terminal voltage
V_s – Source voltage
L- inductor
R_s – Source resistance
i_{st}- Source current
I_{a1}^+- Possitive sequence current
X_s – Source reactance
T_d – Sampling time
$U^*(K)$ – Deadbeat voltage
G_{11}
G_{12}
H_{11}} - Deadbeat voltage parameters
H_{12}

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I. INTRODUCTION

In the distribution side, Power quality gets effected due to the presence of three phase diode bridge rectifier and unbalanced star connected loads system experience issues like voltage sag, voltage swell, current harmonics, and excessive neutral current [1]-[3]. Among the various issues, current harmonics are the major concerned problem. In order to solve the above power quality issues some Flexible A.C Transmission (FACT) devices are used like Static VAR Compensator (SVC), Static Compensator (STATCOM), DSTATCOM and Unified Power Flow Control (UPFC). A DSTATCOM is one of the best solutions to compensate for the above distribution system problems. In[4]-[6] proposes a three single phase DSTATCOM in order to mitigate current harmonics but in three single phase DSTATCOMS having a disadvantage that in system configuration there are 12 Insulated gate bipolar transistor (IGBT) switches because of which switching losses and cost are high and therefore power quality is low. In[7]-[9] proposes a four leg inverter based DSTATCOM in order to eliminate harmonics, load unbalancing but four leg DSTATCOM faces a disadvantage that the system having 8 IGBT switches due to which switching losses are high and therefore power quality is reduced. In [10]-[15] proposes a split capacitor DSTATCOM to eliminate harmonics, excessive neutral current Split capacitor DSTATCOM system having 6 IGBT switches due to which switching losses are compared to above topologies but this also having a disadvantage i.e., D.C voltage unbalancing .

By using spilt capacitor DSTATCOM cannot vary reference D.C voltage as per load requirement. In conventional split capacitor DSTATCOM reference D.C voltage is constant which is two times voltage across point of common coupling because of that D.C voltage is high. As switching losses are directly proportional to D.C voltage power quality gets reduced. In [16]-[18] proposes a filters in order to mitigate harmonics, voltage sag, voltage swell. Filter having different types of controllers in which PI controller, Fuzzy controller. In [19]-[21] proposes adaptive split capacitor DSTATCOM in order to mitigate harmonics, load unbalancing, poor voltage regulation, excessive neutral current but adaptive split capacitor DSTATCOM faces a disadvantage i.e., current harmonics. By using adaptive split capacitor DSTATCOM reference D.C voltage can be varied as per load requirement using lookup table dynamically .So D.C voltage and switching losses are reduced then power quality is improved. To reduce all above power quality issues a deadbeat controller based adaptive split capacitor DSTATCOM is proposed in this paper. Deadbeat controller calculates the reference value of a signal which is varied by using lookup table to reach the desired value of a signal. Then hysteresis controller is used to compare the original signal and reference signal. If that error is within the limits only hysteresis controller sends the gating pulses to the VSI.

II. CONFIGURATION OF A PROPOSED SYSTEM

The proposed block diagram consists of a three phase diode bridge rectifier, star connected load and split capacitor DSTATCOM as shown in Fig.1. The Gate pulses to the IGBT is provided by shunt active power filter Control scheme.

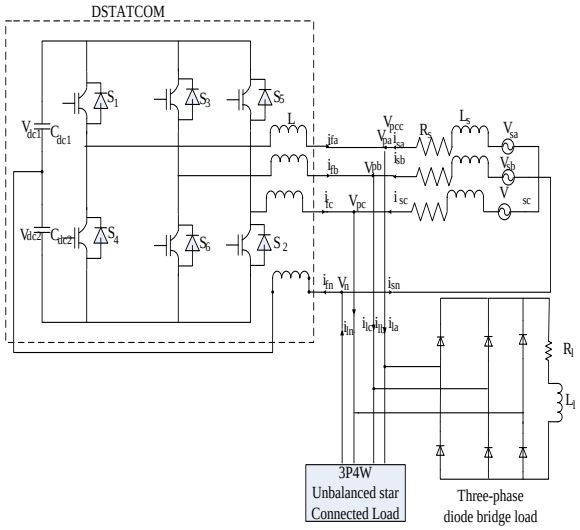

Fig. 1 *Block diagram of split capacitor DSTATCOM*

Fig.2 shows the single line diagram of split capacitor DSTATCOM .From split capacitor DSTATCOM D.C voltage is tracked and reference D.C voltage is varied dynamically by using lookup table and the error is calculated between D.C voltage and reference D.C voltage and that error is given to deadbeat controller. The calculated error is given as an input to the Deadbeat controller and it produces a modulated signal which is applied to hysteresis current controller. If the calculated error is within the limits then it sends the gating pulses to switch IGBT which is present in split capacitor DSTATCOM.

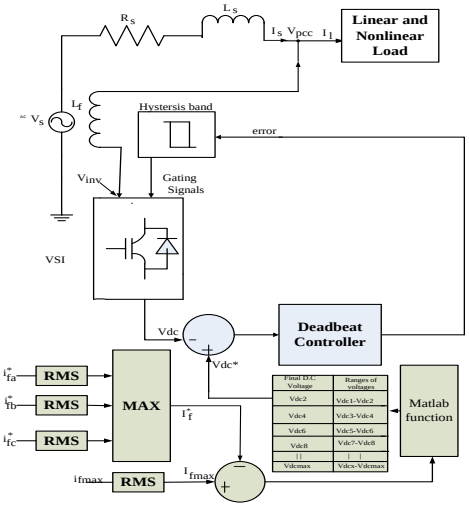

Fig.2 Single line diagram of proposed split capacitor DSTATCOM

2.1 Mathematical modelling

The equations (1)-(4) shows the load currents for each phase (i_{la},i_{lb},i_{lc}) and avg voltage (V_{p0}).

$$i_{la}-\frac{v_{pa}-v_{p0}}{\sum j=a,b,c v_{pj}^2-3v_{p0}^2}\left(p_{lavg}+p_{loss}\right)=i_{fa}^* \quad (1)$$

$$i_{lb}-\frac{v_{pb}-v_{p0}}{\sum j=a,b,c v_{pj}^2-3v_{p0}^2}\left(p_{lavg}+p_{loss}\right)=i_{fb}^* \quad (2)$$

$$i_{lc}-\frac{v_{pc}-v_{p0}}{\sum j=a,b,c v_{pj}^2-3v_{p0}^2}\left(p_{lavg}+p_{loss}\right)=i_{fc}^* \quad (3)$$

$$V_{po}=\frac{1}{3}\left(V_{pa}+V_{pb}+V_{pc}\right) \quad (4)$$

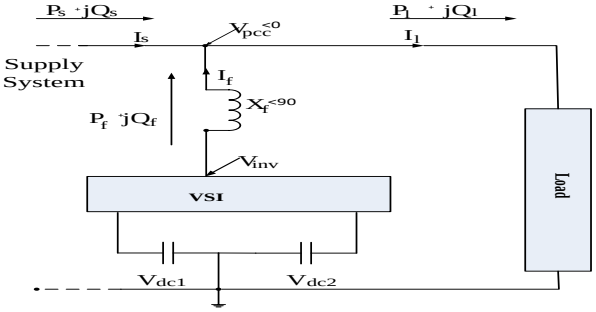

Fig. 3 *Power flow diagram*

From the power flow diagram power and current injected is derived by the DSTATCOM

$$\frac{v_{inv<\theta}-v_{pcc<0}}{x_{f<90}}=I_f \quad (5)$$

$$p_f+Q_f=v_{pcc}I_f^* \quad (6)$$

By substituting equation (5) and (6)

$$P_f+jQ_f=\frac{V_{pcc}V_{inv}}{X_f}\sin\theta+j[\frac{V_{pcc}V_{inv}}{X_f}\cos\theta-\frac{V_{pcc}^2}{X_f}] \quad (7)$$

From equation (7)

$$P_f=\frac{V_{pcc}V_{inv}}{X_f}\sin\theta \quad (8)$$

$$Q_f=\frac{V_{pcc}V_{inv}}{X_f}\cos\theta-\frac{V_{pcc}^2}{X_f} \quad (9)$$

In this D.C Voltage is obtained based on the reactive power. As in this there is no real power so power factor is zero when θ=0

$$Q_f = \frac{V_{pcc}V_{inv}}{X_f}\cos 0° - \frac{V_{pcc}^2}{X_f}$$

$$Q_f = \frac{V_{pcc}V_{inv}}{X_f} - \frac{V_{pcc}^2}{X_f} \quad (10)$$

$$\frac{V_{inv}}{V_{pcc}} = m$$

$$V_{inv} = mV_{pcc}$$

$$Q_f = \frac{V_{pcc}(mV_{dc})}{X_f} - \frac{V_{pcc}^2}{X_f}$$

$$Q_f = \frac{V_{pcc}}{X_f}(mV_{dc} - V_{pcc}) \quad (11)$$

When $mv_{dc} > v_{pcc}$ only DSTATCOM will inject reactive power. During reactive power injection, voltage across point of common coupling will vary.

$$\frac{dQ_f}{dV_{pcc}} = \frac{mV_{dc}}{X_f} - \frac{2V_{pcc}}{X_f} \quad (12)$$

$$\frac{dQ_f}{dV_{pcc}} = 0$$

$$\frac{mV_{dc}}{X_f} - \frac{2V_{pcc}}{X_f} = 0$$

$$mV_{dc} = 2V_{pcc}$$

$$V_{pcc} = (\frac{m}{2})V_{dc}$$

For DSTATCOM, m=1

$$V_{dc} = 2V_{pcc} \quad (13)$$

The maximum reactive power compensation by DSTATCOM.

As the D.C voltage is two times the voltage across point of common coupling then maximum reactive power is

$$Q_f = \frac{V_{pcc}}{X_f}(mV_{dc} - V_{pcc})$$

$$Q_f = \frac{V_{pcc}}{X_f}(V_{dc} - V_{pcc})$$

As $V_{dc} = 2V_{pcc}$

$$Q_f = \frac{V_{pcc}}{X_f}(2V_{pcc} - V_{pcc})$$

$$Q_f = \frac{V_{pcc}}{X_f}(V_{pcc})$$

$$Q_f = V_{pcc}I_{fmax} \quad (14)$$

$I_f = \frac{v_{pcc}}{x_f}$Maximum filter current corresponding to Q_{fmax}

Every time load does not require maximum reactive power

As Reactive power injection is directly proportional to the D.C voltage by DSTATCOM is observed from

$$Q_f = \frac{V_{pcc}}{X_f}(mV_{dc} - V_{pcc})$$

$$= V_{pcc}I_f^*$$

$$I_f^* = \frac{1}{X_f}(mV_{dc} - V_{pcc})$$

$$I_f^* = \frac{I_{fmax}}{V_{pcc}}(mV_{dc} - V_{pcc}) \quad (15)$$

By rearranging all the equations v_{dc}^* is expressed as

$$I_f^* = \frac{I_{fmax}}{V_{pcc}}(mV_{dc} - V_{pcc})$$

$$V_{pcc}I_f^* = mV_{dc}I_{fmax} - V_{pcc}I_{fmax}$$

$$mV_{dc}I_{fmax} = V_{pcc}I_f^* + V_{pcc}I_{fmax}$$

$$mV_{dc}I_{fmax} = V_{pcc}(I_f^* + I_{fmax})$$

$$mV_{dc} = \frac{V_{pcc}(I_f^* + I_{fmax})}{I_{fmax}}$$

$$V_{dc}^* = \frac{V_{pcc}}{m}(\frac{I_f^* + I_{fmax}}{I_{fmax}}) \quad (16)$$

As v_{dc}^* is obtained from (I_f^*). As the load changes frequently reference D.C voltage changes frequently. So it effects the DSTATCOM performance. To eliminate this problem Lookup table is selected in this D.C voltage values are given. Those D.C voltages are taken when load changes from full load to no load step by step in ranges. If the reference D.C voltage falls in the limit then the limit higher value is taken as a reference D.C voltage.

III. DEADBEAT CONTROLLER USED IN DSTATCOM

A Deadbeat controller which is proposed uses a state space of a system to calculate reference voltage in order to set error with in sampling time. Next, the reference voltage vector is sensed by a modulator. This method is used for getting dynamic response.

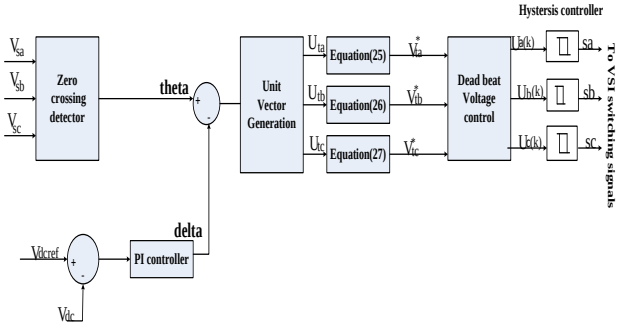

Fig. 4 *Single line diagram of deadbeat controller*

The Fig.4 shows the block diagram of a Deadbeat controller. It consists of the ZCD, unit vector generation, terminal voltage, deadbeat voltage control. The source voltages of each phase are sensed and given to ZCD which is used to detect how many times the waveform crosses zero. The reference D.C voltage is compared with D.C voltage and error is calculated and given to PI controller. The output of PI controller and ZCD is compared and given to unit vector generation it converts output to unit magnitude (u_a,u_b,u_c). The unit vector generation is given to equation (26, 27, 28) to get terminal voltages (v_{ta}^*,v_{tb}^*,v_{tc}^*) the terminal voltage signals are given to deadbeat voltage . It compares the obtained terminal voltages with reference voltages and the error is given to the hysteresis controller. If the error is within the limits of hysteresis controller then it send the gating signals to the voltage source inverter. The mathematical modelling of proposed controller as follows.

The average of load voltage (V_m) is

$$V_m = \frac{1}{3}(V_a^2 + V_b^2 + V_c^2) \quad (17)$$

$$u_a = \frac{V_a}{V_m} \quad (18)$$

$$u_b = \frac{V_b}{V_m} \quad (19)$$

$$u_c = \frac{V_c}{V_m} \quad (20)$$

The equations (18)-(20) shows the unit vector voltages. The terminal voltages ($V_{ta}^*(t)$), ($V_{tb}^*(t)$), ($V_{tc}^*(t)$) given as an input to the deadbeat controller are obtained as follows:

$$V_{tj}(t) = V_{sj}(t) - \frac{Ldi_{st}^*}{dt} - R_s i_{sj}^* \quad (21)$$

$$V\cos\delta_0 = V_t^* + RI_{a1}^+ \quad (22)$$

$$V\sin\delta_0 = X_s I_{a1}^+ \quad (23)$$

Squaring on both sides of equation 22 and 23 we get

$$V_t^* = \sqrt{V^2 - (x_s Ia_1)^2} - RI_{a1}^+ \quad (24)$$

$$V_{ta}^*(t) = \sqrt{2}V_t^* \sin(\omega t - \delta) \quad (25)$$

$$V_{tb}^*(t) = \sqrt{2}V_t^* \sin\left(\omega t - \frac{2\pi}{3} - \delta\right) \quad (26)$$

$$V_{tc}^*(t) = \sqrt{2}V_t^* \sin\left(\omega t + \frac{2\pi}{3} - \delta\right) \quad (27)$$

The equation (31) is used in deadbeat voltage controller to get the required terminal voltage load current and filter current and Table 1 shows the system parameters used for test system.

$$G_{11} = 1 - \frac{Td^2}{2L_f} \quad (28)$$

$$G_{12} = Td - \frac{Td^2}{2L_f} \quad (29)$$

$$H_{11} = \frac{Td^2 V_{dc}}{2L_f} \quad (30)$$

$$U^*(K) = \frac{V_t^*(k+1) - G_{12} i_{fi}(k) - H_{12} i_{ft}(k)}{H_{11}} \quad (31)$$

By using all these equations the error is calculated and that error is given to the hysteresis controller if that error is within the limits only hysteresis controller send signal to voltage source inverter to mitigate current harmonics. In this also reference D.C voltage is varied step by step dynamically.

Table 1 Test parameters

System Parameters	Value
Supply Voltage	440V
Source Impedance and Resistance	0.2Ω, 1mH
Filter Inductance	12mH
D.C Link Capacitance	1600μF
PI Controller	10, 0.01
Hysteresis Band	+0.1, -0.1
Unbalanced Linear Load	a-ph. 20Ω,32mH b-ph 16Ω, 42mH c-ph 10Ω, 60mH
Three Phase Diode bridge Load	36Ω, 128mH
Rated D.C Voltage	1200V
Deadbeat voltage parameters G11 G12 H11 H12	 -14 -14.4 18000 -0.6

IV. Results and Discussion

A. Source voltage without compensator

Deadbeat controller based adaptive split capacitor DSTATCOM is connected to three phase diode bridge rectifier and unbalanced star connected load is simulated by using MATLAB SIMULINK. Fig. 5 shows a source voltage waveform of a system having three phase diode bridge rectifier and unbalanced star connected load. Due to the presence of three phase diode bridge rectifier waveform is having distortions operated from 0.3-0.6 sec.

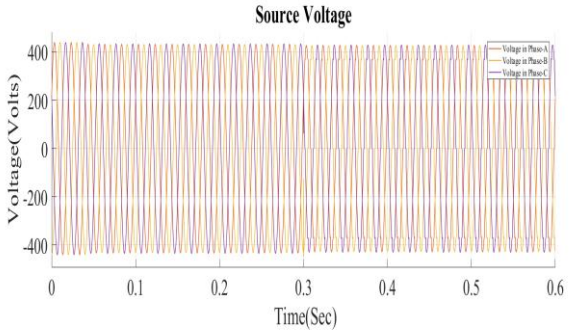

Fig.5 *Source Voltage waveform*

B. Source current without compensator

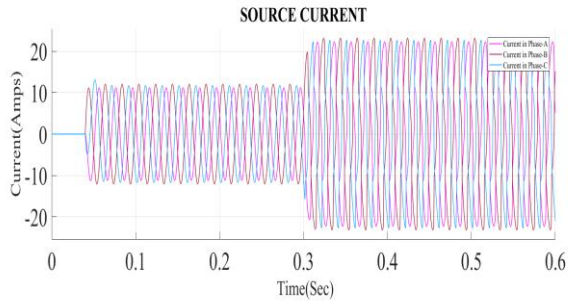

Fig.6 *Source current waveform*

Fig. 6 shows that source current waveform having unbalanced star connected load and three phase diode bridge rectifier. Due to nonlinear is operated from 0.3-0.6 sec system shows distortions in source current waveform.

C. Load current without compensator

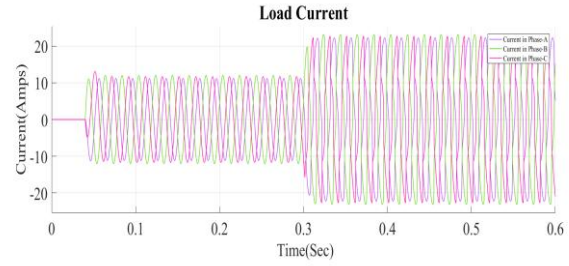

Fig.7 *Load current waveform*

Fig.7 shows load current waveform having unbalanced star connected load and three phase diode bridge rectifier. In current waveform due to the presence of nonlinear load distortions are very high from 0.3-0.6 sec is observed.

D. THD without compensator

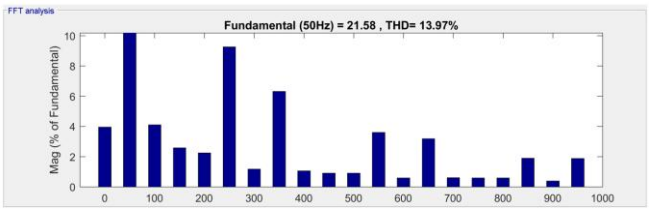

Fig.8 *THD of load current waveform*

E. Conventional split-capacitor DSTATCOM

To reduce THD of load current a conventional split capacitor DSTATCOM is used. Traditional split capacitor DSTATCOM is connected at point of common coupling by using this THD is reduced then power quality gets improved.

1. D.C voltage waveform

Fig. 9 shows D.C Voltage across conventional Split Capacitor DSTATCOM. As reference D.C voltage is fixed and it cannot vary as per load requirement .so the D.C voltage is high actually that reference D.C Voltage is two times the voltage across point of common coupling voltage. So, in Conventional Split Capacitor DSTATCOM, the D.C Voltage is high.

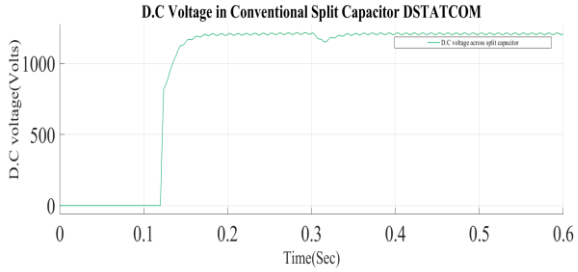

Fig. 9 *D.C voltage of a conventional split capacitor DSTATCOM*

2. Voltage across switches

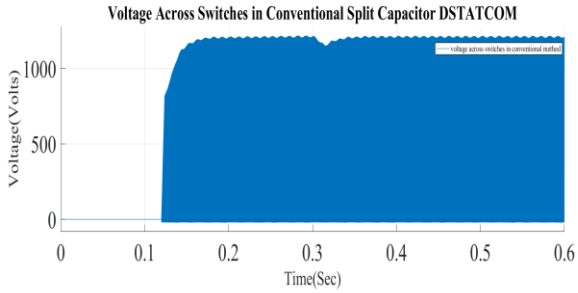

Fig.10 *Voltage across switches in conventional split capacitor DSTATCOM*

Fig. 10 shows voltage across Switches in the circuit. From Fig.10 it is observed that D.C voltage is directly proportional to voltage across switches. As D.C voltage is high voltage across switches also high because of that switching losses will be more so power quality is reduced

3. THD

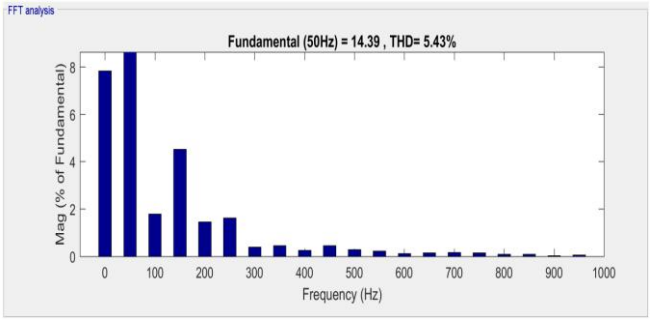

Fig.11 *THD of Load current in conventional split capacitor DSTATCOM*

Fig.11 shows the THD of load current using conventional split capacitor DSTATCOM. THD of load current is reduced to 5.43% from 13.97% when THD is compared between system using conventional split capacitor DSTATCOM and system without using compensator

F. Adaptive split capacitor DSTATCOM

To reduce D.C voltage an adaptive split capacitor DSTATCOM is used because of which switching losses are also reduced.

1. D.C voltage

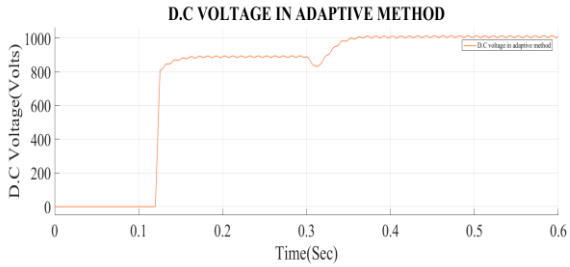

Fig.12 *D.C voltage of adaptive split capacitor DSTATCOM*

Fig. 12 shows the D.C voltage of an adaptive split capacitor DSTATCOM. So by using adaptive split capacitor DSTATCOM reference D.C voltage is varied as per load requirement by using lookup table. By varying reference D.C voltage D.C voltage is reduced from 1200 to 1000.

2. Voltage across switches

Fig. 13 shows Voltage across Switches using adaptive split capacitor DSTATCOM. As D.C voltage is reduced from 1200 to 1000 voltage across switches also reduced from 1200 to 1000. From this power quality gets improved

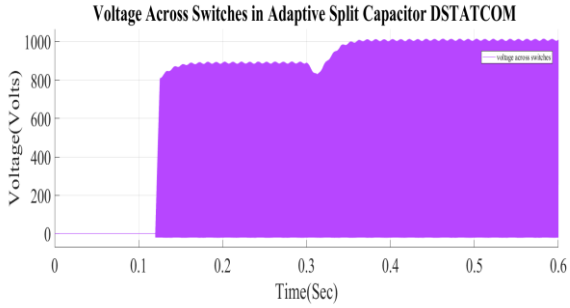

Fig.13 *Voltage across switches in adaptive split capacitor DSTATCOM*

3. THD for load currents

Fig.14 shows THD of a load current using adaptive split capacitor DSTATCOM. By using adaptive split capacitor DSTATCOM the THD is increased compared to traditional Split Capacitor DSTATCOM from 5.43% to 19.42%.

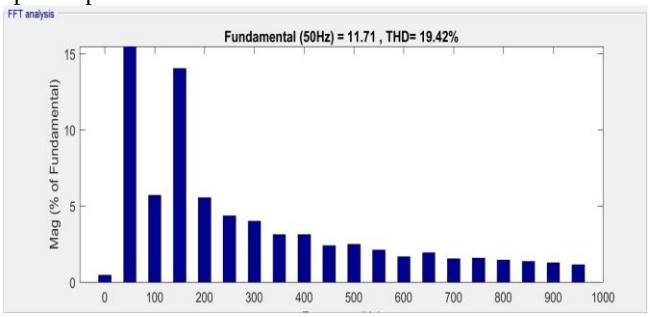

Fig.14 *THD of Load current in adaptive split capacitor DSTATCOM*

G. Deadbeat controller for adaptive split capacitor DSTATCOM

So to reduce THD of load currents using a deadbeat controller based adaptive split capacitor DSTATCOM .If PI controller is used instead of deadbeat controller keeping Kp value as constant and Ki value is increased then current harmonics are increased. If Ki value is decreased then system becomes slow

1. D.C voltage

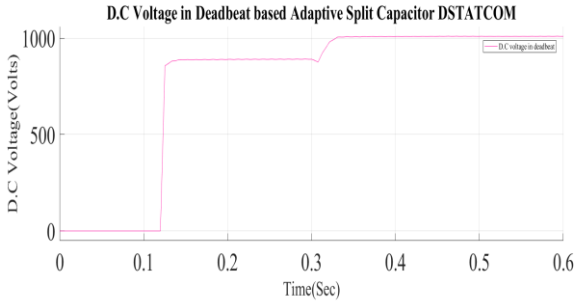

Fig.15 *D.C voltage of deadbeat controller for adaptive split capacitor DSTATCOM*

Fig. 15 shows the D.C Voltage waveform of a Deadbeat Controller for Adaptive Split Capacitor DSTATCOM. By using a Deadbeat controller for Adaptive Split Capacitor DSTATCOM the D.C Voltage is as same as Adaptive Split Capacitor DSTATCOM

2. THD for load currents

Fig.16 shows the THD of load current a deadbeat controller based adaptive split capacitor DSTATCOM. THD is reduced from 19.47% to 6.43% when compared between adaptive split capacitor DSTATCOM and deadbeat controller based adaptive split capacitor DSTATCOM

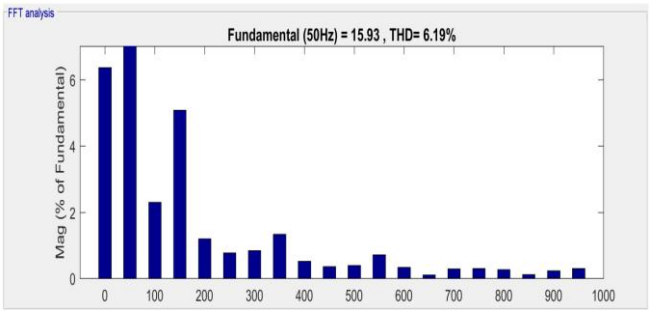

Fig.16 *THD of Load current of a deadbeat controller for adaptive split capacitor DSTATCOM*

Table 2 Comparative Results

Parameters	**D.C Voltage**	**% TH D**
Without DSTATCOM	-	13.97
With conventional split capacitor DSTATCOM	1200	5.43
Adaptive split capacitor DSTATCOM	1000	19.42
With using of deadbeat controller based Adaptive split capacitor DSTATCOM	1000	6.74

Table 2 shows the comparative results of D.C voltage and THD without using any FACT devices THD is 13.97% to reduce the THD of load current a split capacitor DSTATCOM is used. By using conventional split capacitor DSTATCOM D.C voltage is 1200 and THD of load current is 5.43%. So to reduce D.C voltage from 1200 to 1000 an adaptive split capacitor DSTATCOM but THD of load current is 19.47%. To reduce THD of load current from 19.47%to 6.74% a deadbeat controller based adaptive split capacitor DSTATCOM.

V. CONCLUSION

This study presents the usage of nonlinear load and unbalanced star connected loads due to which power quality issues arises in the distribution system. In order to mitigate harmonics a conventional split capacitor DSTATCOM is used. But by using a conventional split capacitor DSTATCOM there is a disadvantage i.e., D.C voltage is high due to which switching losses are more. So to reduce D.C voltage an adaptive split capacitor DSTATCOM is used in this reference D.C voltage is varied in step by step dynamically by using a lookup table. However by using an Sadaptive split capacitor DSTATCOM also there is a disadvantage i.e., current harmonics. To reduce current harmonics in the system instead of using a PI controller a deadbeat controller is used because of which power quality is improved. So deadbeat controller is much better than PI controller in adaptive split capacitor DSTATCOM.

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