

# An Improved Pso Algorithm for Floor Planning in Asic Design

R. Dheebiga, R. Manikandan

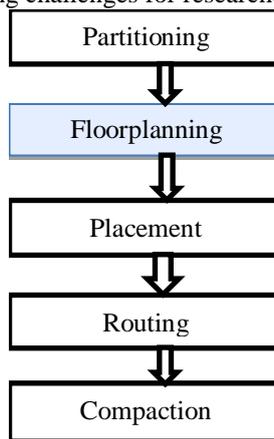
**Abstract:** Floorplanning is a life of any Very Large Scale Integration physical design flow. Floor planning is the method of assembling blocks in a chip and identifying structures which are closely organized and assigning space for them. One of the main responsibilities of floorplan in physical design is to reduce the area requirements and improving its performance. Floor plan in general is a Non-deterministic polynomial time hard problem and such problems can be resolved using numerous heuristics algorithm which can also be used for different representation. The key intention of this paper is to gain knowledge about different algorithms and to know how those algorithms can be used for solving a floorplan problem with constraints satisfying an optimal area and smaller run time thus increasing its performance. In existing method algorithms such as genetic algorithm, simulated annealing and ant colony optimization algorithm had been used and from those algorithms, genetic algorithm had given a better or promising result by its cost functions evaluation, when compared to other methods using ASIC Design implemented with MATLAB. But the Computation time of genetic algorithm was the major issue in existing system. Hence, the proposed method is dealt with improved particle swarm optimization algorithm based on inertia weight parameter because of its better computational efficiency and its high speed. A comparative study of four different algorithms based on its computation time has been made and shown that Particle Swarm Optimization algorithm takes less time for computation when compared with existing algorithms by their best cost function.

**Keywords:** Area optimization, Floorplanning, Heuristics algorithm, Physical design, VLSI

## I. INTRODUCTION

In today’s industrialized domain, there is a continually growing demand for speed, features and performance. The extant market has been becoming more and more demand, forcing difficult architecture and reduced time to market [1]. In such cases floor plan not only captures designer’s intent, but also presents the prospects and challenges that shake the entire design flow starting from implementation to chip assembly. Floor plan technique plays a vigorous role in physical design and it is the first stage in designing the layout of the chip [2]. Floorplanning is the method of arranging blocks or macros in a chip region and thereby determining its routing area.

The constraints which are to be followed for good floor planning are that, the total area of the chip should be minimized as much as possible and making the routing phase easier, also improving its performance. The major purpose of designing VLSI floorplanning circuit is to generate a circuit with rectangular module and also with an objective of minimum area [3]. Fig1 represents that CAD Floorplanning is the most needed step next to partitioning, because if the output of floorplanning is poor, it has the possibility of affecting all the consequent steps, such as placement, routing and compaction. Floor plan in VLSI is basically characterized into two structures such as slicing and non-slicing. The floor plan is known to be a slicing floor plan, if its floor plan arrangement is repeatedly cut into horizontal or vertical structure, whereas it is not apparent in non-slicing[4, 5]. Floor plan in VLSI is generally a non-deterministic polynomial time hard problem and so its solution space rises with respect to its circuit size [6]. Therefore, finding an appropriate solution is the prevailing challenges for researchers.



**Fig: 1 Physical Design Cycle**

Even though, researchers have found various heuristics algorithm for solving such problems [7]. This paper provides a comparative results between genetic, ant colony optimization, simulated annealing and particle swarm optimization and shown that PSO algorithm provides a good computational efficacy. The following sections are as follows: Section 2 represents existing methodology, Section 3 represents the proposed method of floorplans, Section 4 represents Results and discussions of present method and section 5 concludes the paper.

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## II. EXISTING METHODOLGY

Floor planning steps are responsible for determining the position or locations of a module for obtaining minimum wire length and hence the area will be minimized [8]. For such a floor planning process, different heuristics or meta-heuristics algorithms can be used for representation. In an existing approach an algorithms viz. simulated annealing, ant colony, genetic algorithm had been used up for execution and comparison [9].

Each algorithm is based on similar functions such as finding shortest distance between a source and destination to achieve a minimum area. In each algorithm, a block is chosen as

random and the process for finding shortest distance is carried out and hence the finest solution for each block is obtained [10]. These algorithms are compared based on its cost function parameter. The below experimental results had being carried out with 500 iterations using MATLAB language. From those algorithms genetic algorithm had given a best result during its iteration [1] and shown in table 2 with its comparison. The main problem in the GA is its computation time which is greater than other algorithm. Fig: 2,3,4 shows the existent's cost function comparison results.

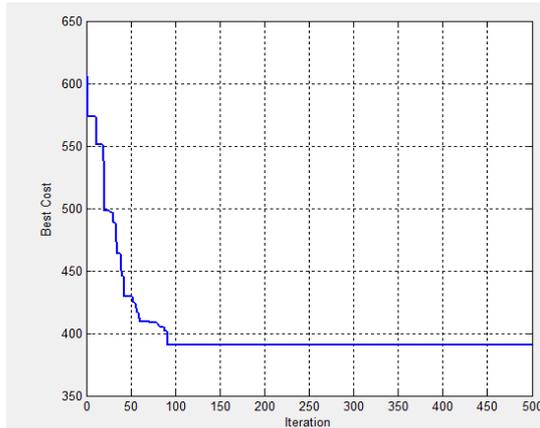


Fig: 2 Cost function of SA

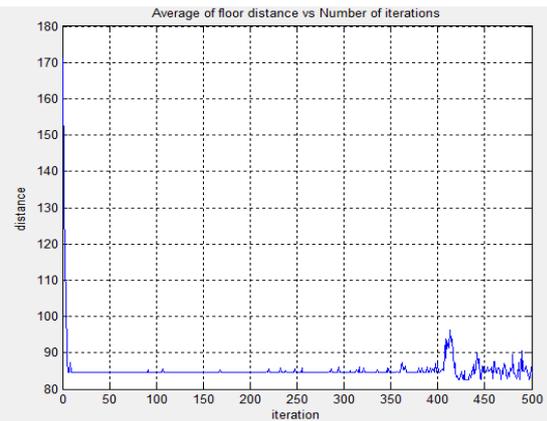


Fig: 3 Cost function of ACO

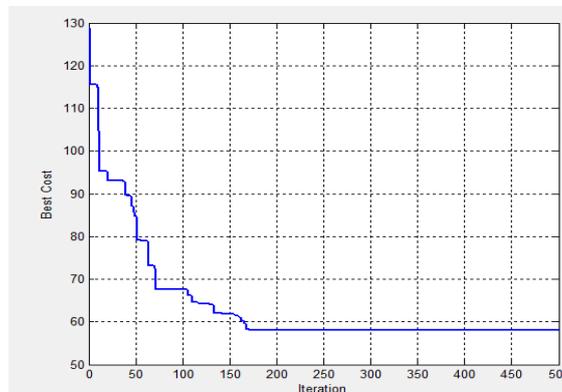


Fig: 4 Cost function of GA

## III. PROPOSED METHODOLGY

### A. Particle Swarm Optimization

To overcome the limitations of existing method, PSO algorithm with improved block parameter information is chosen for proposed method. The simple PSO algorithm is random search techniques which are based on bird's behavior [11]. Apart from other algorithms PSO algorithm has the best characteristics such as; it remembers the multiple previous successes of itself and its neighbors during its search. PSO algorithm is led by its personal understanding (p best) and the overall understanding (g best) [12, 13]. The algorithm starts by choosing the blocks at random and moves in random direction in search of optimum area and for next iteration it moves to a new block for finding optimum solution than its

previous iteration [14]. In improved PSO algorithm inertia weight is the major parameter selected, which is used to control the velocity associated while moving in search of optimum solution. Initially, the inertia weight is high and further it is reduced. Inertia weight has an ability of providing firmness between exploration and exploitation process. Inertia weight helps in determining the rate of particles previous velocity with its current velocity at each time interval of steps [15]. The resulting block diagram demonstrates the implementation process for attaining the required

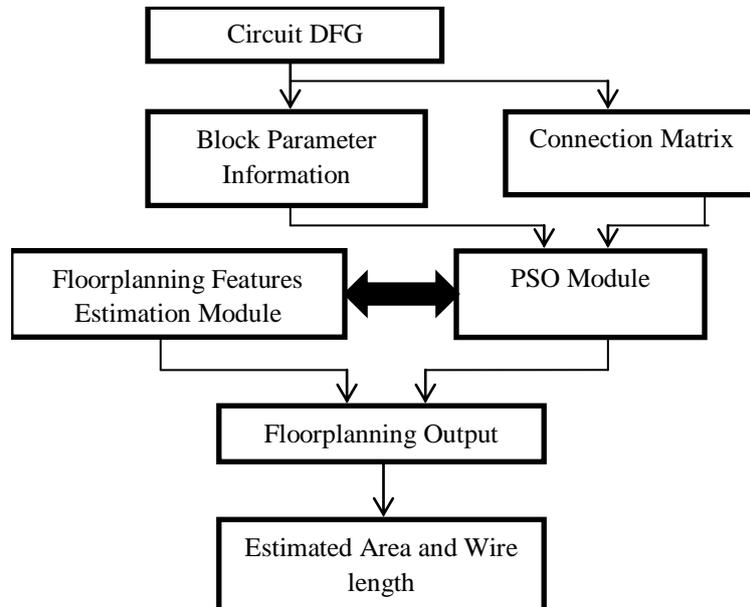


Fig: 5 PSO block diagram

The DFG circuit is used because of its retiming concepts, the retiming reduces the critical path time and also the circuit speed will be increased. Then, block parameter information together with its connection matrix is given to the PSO unit. After estimating the floor planning features along with PSO module result, the result for floor planning with estimated wire length and area is obtained.

The improved PSO algorithm is realized using MATLAB version 8.3 and the output is obtained by reducing the inertia weight. Generally, inertia weight will be ranging between 0.9-0.4 but as the researchers proved that decreasing the inertia weight will produce good results, the experimentation is done by reducing it below 0.4 and the result is obtained. The below output is executed using different inertia weight 0.3, 0.2 with 500 iterations.

IV. RESULTS AND DISCUSSIONS

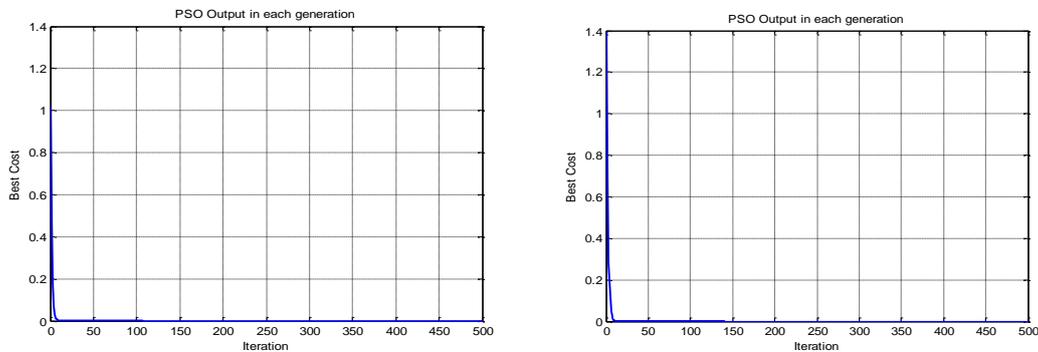


Fig: 6 Cost function of PSO algorithm with different inertia weight

Table: 1 Inertia weight table calculated using MATLAB

ITERATIONS	INERTIA WEIGHT	VALUES
500	0.9	5.194e-029
500	0.8	1.1677e-039
500	0.7	3.1611e-026
500	0.6	3.0291e-036
500	0.5	3.0158e-043

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500	0.4	3.791e-058
500	0.3	2.8399e-037
500	0.2	1.2903e-020
500	0.1	1.9882e-031

**Table: 2 Comparison table for specified algorithms**

Optimization Methods	Iterations	Best cost
Simulated Annealing	500	390.6841
Ant Colony Optimization	500	87.6888
<b>Genetic Algorithm</b>	<b>500</b>	<b>67.9512</b>
<b>Particle Swarm Optimization</b>	<b>500</b>	<b>5.9158e-038</b>

An experimental result shows that from the above algorithm Particle Swarm Optimization (PSO) algorithm has a reduced computation time with respect to its cost function and provides a better solution for floor planning process.

### V. CONCLUSION

From VLSI design perspective, area is also the significant factor which is always expected to occupy a minimum area. The idea behind this study is to achieve minimum area and wire length while placing the modules in the chip design under floor planning process and thereby increasing its performance. In this paper, a comparative work of four different algorithms based on its computation time with respect to its cost function is done which is implemented using MATLAB. From those algorithms, improved PSO algorithm has given a favorable result with low computational complexity and hence shown that PSO algorithm has taken less time for computation when compared with existing algorithms. PSO overcomes the limitations of existing method and has an ability of finding realistic solution for soft and hard modules instead when matched with other algorithms. Future emphasis is on improvement in particles neighborhood in an improved PSO method.

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**R. Dheebiga** is currently pursuing her Master of Technology in VLSI Design from SASTRA Deemed University, India. She received her Bachelor of Engineering from University College of Engineering panruti, Anna University. She is interested in the field of VLSI physical design and Digital CMOS VLSI Design.



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