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Optimized VLSI Design of 2-Bit Magnitude Comparator using GDI Technique

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Abstract: ***In the modern VLSI, the need for optimizing design constraints has become a major concern both at schematic level as well as layout level. Mux based approach has been extensively used due to the efficient implementation of Mux using Gate Diffusion Input (GDI). Several designs have been studied and finally a Mux based Magnitude Comparator is proposed with optimized VLSI design constraints. All the possibilities of design using mux with wide variety of primary inputs as selection inputs of mux have been studied and the best design which has lead to minimal transistor count was proposed.In this paper, GDI technique has been implemented in 250 nm process technology using TANNER S-EDIT. There is 70%, 33% and 9% reduction in transistor count in comparison with existing GDI comparators respectively***

Index Terms**:** ***Magnitude Comparator; Gate Diffusion Input Technique; Mux Based Logic design***

I. INTRODUCTION

Logic minimization is the prime concern for Digital logic circuits as it will lead to optimized design constraints of VLSI. This logic minimization can happen if Boolean expressions are minimized. Comparator is one of the important blocks used in digital logic design. It does have many applications in DSP. Comparator compares two words and decides whether A>B or A<B or A=B.

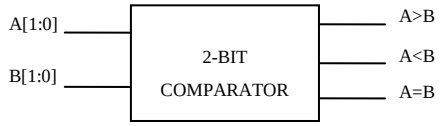

Fig. 1 Symbol of 2-bit Magnitude Comparator

Fig.1 is the Block Diagram for 2- Bit magnitude comparator it compares two numbers A and B and gives output A>B as 1 when A is having more magnitude then B and A<B as 1 when B is having more magnitude then A and A=B as 1 when B is having same magnitude of A.

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"Comparator has been designed with only 22 Number of transistors in GDI.[1]" "Comparator in GDI has been designed by using Full-Adder with 30 Number of transistors.[2]" "Comparator has been designed for high performance by using parallel MSB checking method but by sacrificing Area.[4]"

"Comparator was designed with further high performance by going for MUX based structure but by even more sacrificing with area.[5]" "Pseudo logic implementation of comparator has taken 100 transistors, PTL implementation has taken 54 Number of transistors and Hybrid logic has taken 38 Number of transistors[6]" "Comparator has been designed with 74 Number of transistors. by using TGL.[7]" The Section 2 describes about Conventional MOS Comparator, existing GDI Comparators. Section 3 describes about the Proposed Comparator. Section 4 covers the simulation results of proposed comparator with existing Comparators in terms of transistor count. Section 5 gives the conclusion.

II. LITERATURE SURVEY

A. *Conventional cmos magnitude comparator*

"[2]The logic function of the magnitude comparator can be realized conventionally using 66 Transistors." As it uses more number of transistors, power consumption will be more but with full output voltage swing.

B. *Existing gdi magnitude comparator[2]*

Gate Diffusion Input(GDI) is a Technique in which lengthy expressions can be realized using less amount of hardware as PMOS and NMOS source/drain can be either Power rails or primary inputs or intermediate inputs or any constants with logic0 or logic1. "Basic Cell of GDI looks like a basic CMOS inverter as shown in figure 2.1[8]" G, P and N are considered as inputs to the GDI Cell.

- G activates at a time either PMOS or NMOS based upon the logical value applied.
- N input is applied to source/Drain of NMOS
- P input is applied to the source/drain of PMOS.

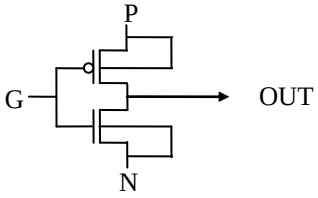

Fig .2.1 Basic GDI Cell

"Based upon the logical values applied to the GDI cell inputs functions will vary accordingly[1]". Despite having many advantages with GDI its performance declines when technology is scaled down and in which we can expect voltage scaling and logic 0 and logic 1 regions get minimized such that noise margins become reduced.
To overcome this Modified GDI is preferred. "In Modified GDI, bulk/body
terminals of PMOS and NMOS are connected to VDD and GND respectively as shown in Fig.2.2.[3]"

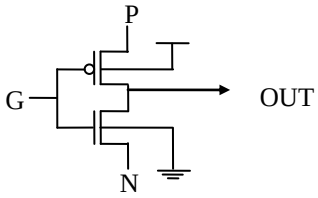

Fig .2.2 Basic Modified GDI Cell

"Existing 2-Bit GDI magnitude comparator using 30 transistors is based on full adder.[2]" The functions required are XOR, NOT, AND, MUX 2 TO 1 and NOR. so in total 5 cells are required. Below Table shows Total number of cells required and the Transistor count

Table 1. Cells and Transistor count for [2].

Function required	Number of cells	Total number of Transistors
XOR	4	30
AND	2	
NOT	2	
MUX 2 TO 1	2	
NOR	1	

C. *Existing 2-bit gdi magnitude comparator*[1]

Above proposed Comparator used 22 number of Transistors. Functions required are XNOR, A<B, NOT, MUX 2 TO 1, OR and AND. so in total 6 cells are required.Below Table shows the Total number of cells required and their Transistor count.

Table 2. Cells and Transistor count for [1].

Function required	Number of cells	Total number of Transistors
XNOR	2	22
A<B	2	
NOT	1	
MUX 2 TO 1	1	
OR	1	
AND	2	

III. PROPOSED COMPARATOR

A. *Mux based design*

1.) Any combinational logic circuit can be designed using mux and chosing the size of mux is the concern and it will be based on the number of inputs of a circuit. Depending upon the mux size chosen the resultant hardware will vary.

2.) The resultant hardware not only vary based on chosing the size of mux but also on chosing the inputs for selection lines of a circuit.

B. *Design for A>B*

Two conditions will be there for A>B to become true so we can expect two
number of product terms in which each product term represents one condition.

AGB = A1B'1 + A0B'0 (A1 +B'1)……(1)
We have chosen mux size of 4 to 1 because chosing mux size of 2 to 1 is leading to very lengthy expressions and mux size of 8 to 1 by default lead to more hardware.We have chosen inputs a1 and b1 as selection lines and it is leading to minimum hardware out of 12 possible cases.
Case1: A1A0
Case2: A1B1
Case3: A1B0
Case4: A0A1
Case5: A0B1
Case6: A0B0
Case7: B1A1
Case8: B1A0
Case9: B1B0
Case10: B0A1
Case11: B0A0
Case12: B0B1

Case(1,4), case(2,7), case(3,10), case(5,8), case(6,11), case(9,12) will lead to same hardware except with at the data input side hardware changing its position. All possible cases were investigated and with choice of a1b1 has lead to minimum hardware.

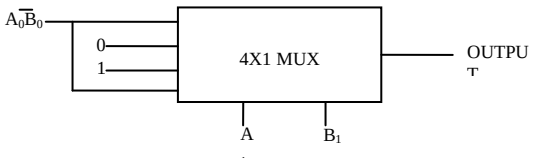

Fig .3.1 Design for A>B.

Above figure has 4 possible cases

Case1:when A1B1=00 then substituting these values in expression 1 leaves us with A0B'0. So this evaluated expression should be passed on the top data input line.
Case2:when A1B1=01 then substituting these values in expression 1 leaves us with 0. So this value should be passed on the second data input line.
Case3:when A1B1=10 then substituting these values in expression 1 leaves us with 1. So this value should be passed on the third data input line.
Case4:when A1B1=11 then substituting these values in expression 1 leaves us with A0B'0. So this value should be passed on the bottom data input line.

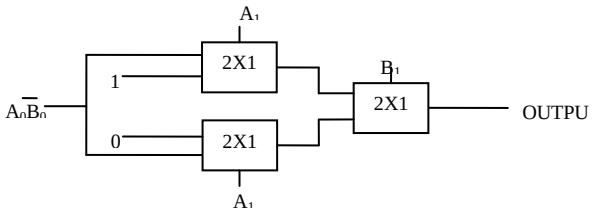

Fig .3.2 Further decomposition for A>B.

Above figure shows the decomposition of mux 4 to 1 which requires three mux 2 to 1 and the top most path is for a1b1(00), second path is fora1b1(10), third path is for a1b1(01) and bottom most path is for a1b1(11).

C. ***Design for A<B***

Two conditions will be there for a<b to become true so we can expect two number of product terms in which each product term represents one condition.

ALB = A'1 B1 + A'0 B0 (A'1 + B1)…… (2)

We have chosen mux size of 4 to 1 because chosing mux size of 2 to 1 is leading to very lengthy expressions and mux size of 8 to 1 by default lead to more hardware.
We have chosen inputs a1 and b1 as selection lines and it is leading to minimum hardware out of 12 possible cases
Case1: A1A0
Case2: A1B1
Case3: A1B0
Case4: A0A1
Case5: A0B1
Case6: A0B0
Case7: B1A1
Case8: B1A0
Case9: B1B0
Case10: B0A1
Case11: B0A0
Case12: B0B1
Case(1,4), case(2,7), case(3,10), case(5,8), case(6,11), case(9,12) will lead to same hardware except with at the data input side hardware changing its position. All possible cases were investigated and with choice of a1b1 has lead to minimum hardware.

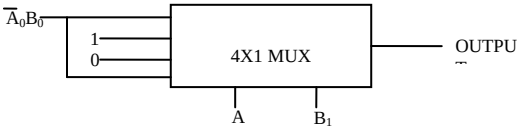

Fig .3.3 Design for A<B.

Above figure have 4 possible cases

Case1:when A1B1=00 then substituting these values in expression 2 leaves us with A'0 B0. So this evaluated expression should be passed on the top data input line.
Case2:when A1B1=01 then substituting these values in expression 2 leaves us with 1. So this value should be passed on the second data input line.
Case3:when A1B1=10 then substituting these values in expression 2 leaves us with 0. So this value should be passed on the third data input line.

Case4:when A1B1=11 then substituting these values in expression 2 leaves us with A'0 B0. So this value should be passed on the bottom data input line.

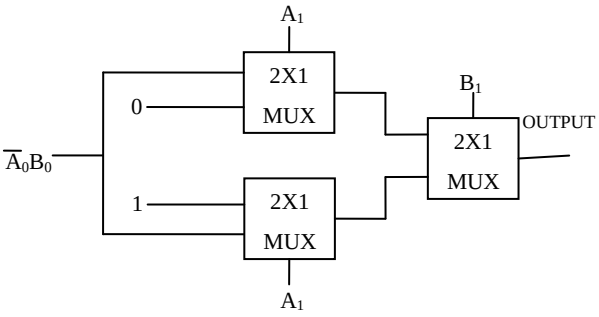

Fig .3.4 Further decomposition for A<B.

Above figure shows the decomposition of mux 4 to 1 which requires three mux 2 to 1 and the top most path is for a1b1(00), second path is fora1b1(10), third path is for a1b1(01) and bottom most path is for a1b1(11)

D . ***Required functions***

Total of 4 functions are required for our design which are A>B, A<B, MUX 2 TO 1 and NOR so in total 4 cells are required. Below Table shows the Total number of cells required and their Transistor count.

Table 3. Proposed Cells and Transistor count.

Function required	Number of cells	Total number of Transistors
A>B	1	20
A<B	1	
MUX 2 TO 1	6	
NOR	1	

i *Nor*

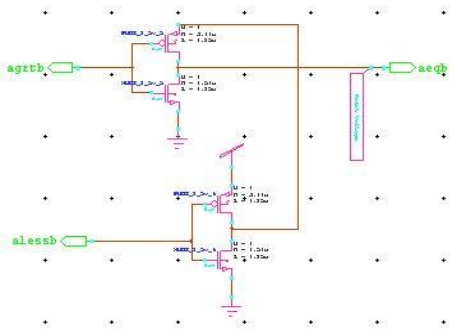

Fig .3.5 Design for NOR.

Above figure describes about NOR function which was required for designing A=B, since if A>B is true or A<B is true A=B is false.

ii *Logic for A>B*

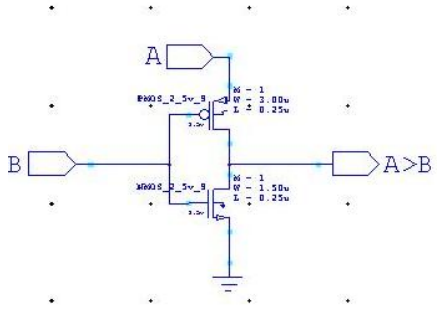

Fig .3.6 Design for A>B.

Above figure describes about A>B function and it is the careful selection of where A and B has to be given.

iii *Logic for A<B*

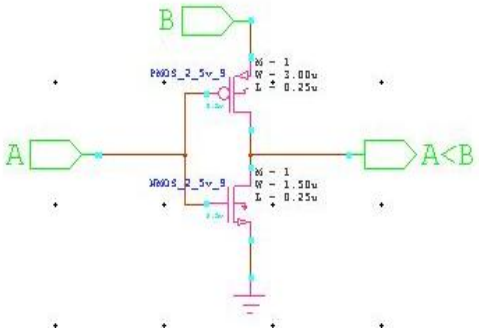

Fig .3.7 Design for A<B.

Above figure describes about A<B function and it is the carefull selection of where A and B has to be given.

iv *mux*

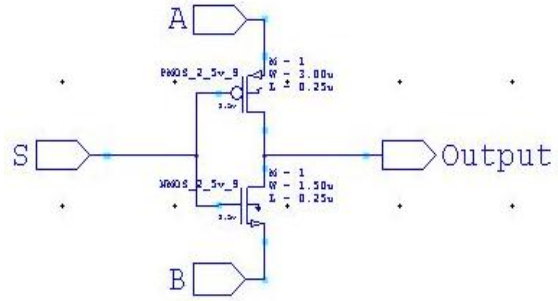

Fig .3.8 Design for Mux 2 to 1.

Above figure describes about Mux 2 to 1 function and it is the careful selection of where A, B and S has to be given.

E. *Proposed 2-bit magnitude comparator*

A new Optimized Architecture for magnitude comparator is proposed with 20 transistors. Block Diagram of Proposed Modified GDI Magnitude Comparator is shown in Fig.3.9.

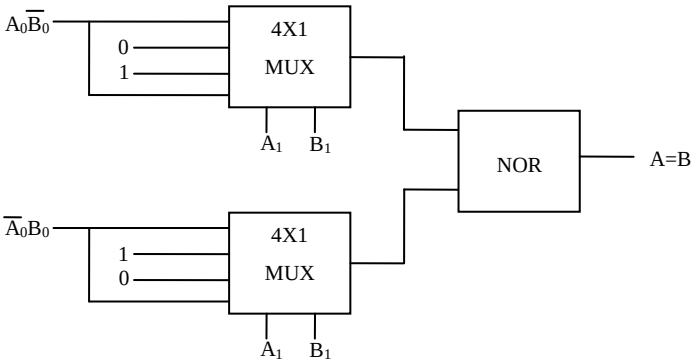

Fig . 3.9 Block Diagram of proposed 2-Bit Magnitude Comparator

Above figure shows the Mux based implementation of 2-bit Comparator in which very less hardware is needed at the data inputs of the Mux. The approach was to first realize circuit in parallel for A>B and A<B. Nor gate was needed to obtain A=B.

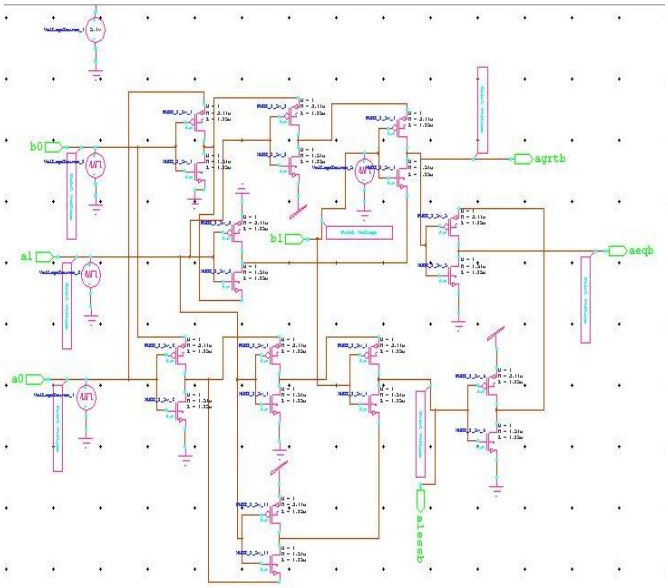

Fig . 3.10 Schematic of proposed 2-Bit Magnitude Comparator

The Function (A>B) can be realized usingModified GDI with three Mux 2 to 1(6 transistors) and one A>B cell(2 transistors) making it a total of 8 transistors.The Function (A<B) can be realized with three Mux 2 to 1(6 transistors) and one A>B cell(2 transistors) making it a total of 8 transistors.The Function (A=B) can be realized using GDI with 4 transistors using NOR. The proposed 2-Bit Magnitude Comparator using modified GDI is implemented and simulated in TANNER S-EDIT in 250nm Technology. Schematic is shown in Fig. 3.10.

IV. RESULTS

Simulation results for the all the 16 Combinations of 2-bit magnitude comparator are shown below at 5V supply voltage in Fig.4.1.

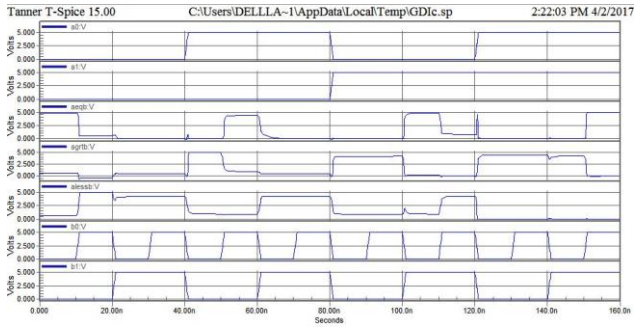

Fig . 4.1 Simulation results of proposed 2-Bit Magnitude Comparator

Table 4. Power consumption at varying Input Voltages for proposed design

Average power consumption(proposed design)	4v	3v	2v
Uw	70.669	33.678	10.696

Table5 shows the difference in Transistor count and it is only for 2-bit Comparator we are able to reduce the Transistor count and for N-Bit Comparator reduction might be greater than or in equal proportion

Table 5. Transistor count comparison for existing and proposed.

Area	Design in reference2	Design in reference1	Proposed
Number of transistors	30	22	20

Proposed Comparator requires only 20 number of transistors where as the conventional implementation and existing GDI comparators requires 66, 30 and 22 transistors respectively.

V. CONCLUSION

Designing a maximum optimized VLSI circuit is never end research area. As a logic designer we need to go for many number of design iterations such that we might finally end up with a quality of design. Mux based approach is very powerful especially when designing circuits in GDI. Logic minimization has also been done and choosing the Mux size as well as selecting which inputs should be given for select lines is also a concern for maximum optimization. A innovative proposal is made for the design and implementation of 2-bit Magnitude comparator using an Enhanced GDI technique in terms of VLSI Design constraints. The proposed design using Modified GDI technique compared with Conventional design has 33% of reduction in transistor count in which equal probability of PMOS and NMOS transistors were minimized. With Existing GDI comparators design which we proposed offers a 9% considerable reduction in Transistor count at the schematic level.

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