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Design Optimization Of Triple Material Gate Stacked Oxide TFET

A Maria Jossy , Swati Sajee Kumar, Ananya Chakraborty, Namrata Lahiri

Abstract— In this paper, we propose the design and purpose for devising a Triple Material Gate Stacked Oxide (TMGSO) Tunnel Field Effect Transistor (TFET) to simultaneously optimize the On current (I_{ON}), Off current (I_{OFF}) and the threshold voltage. Moreover, the design also improves the sub-threshold slope, the I_{ON}-I_{OFF} ratio and also provides immunity from the Short Channel Effects (SCEs). We also compare the transfer characteristics of our structure with the previously developed structures and justify the reasons behind the variations. Furthermore, the relationship between the work function of the metal and the electric field has also been studied by comparing the simulation results of Single Metal Gate (SMG) TFET with the TMGSO TFET. The design and simulation of TFET is done on Technology Computer Aided Design (TCAD Sentaurus) Simulator

Index Terms—On current, Off current, threshold voltage, sub-threshold slope, Short Channel Effects, work function

I. INTRODUCTION

Following the observations by Gordon Moore, the size of transistors on an integrated circuit have been scaled down throughout the years, to meet the requirements for speed, complexity and circuit density. However, with the rise in the number of MOSFETs per unit area the total power consumption also increases. Therefore, an alternative for MOSFET has been demanded for an ultra-low-power consumption. Tunnel Field Effect Transistor (TFET) has been proved as one of the suitable alternative for MOSFET [6]. TFET has a major advantage of a lower Sub-threshold Swing (SS) below 60mV/decade and a significantly less Off current (I_{OFF}) compared to that of MOSFET [7-8]. Moreover, TFET follows the principle of Band to Band tunneling (BTBT) which is responsible in suppressing the undesirable Short Channel Effects (SCE) whereas in MOSFET thermionic emission is responsible for the source-drain current (I_{ds}). However, the On current (I_{ON}) in TFET is comparatively lower to that of MOSFET.

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* Correspondence Author
Namrata Lahiri*, Department of ECE, SRM Institute of Science and Technology, Chennai, India
A Maria Jossy[1] , Department of ECE, SRM Institute of Science and Technology, Chennai, India
Swati Sajee Kumar, Department of ECE, SRM Institute of Science and Technology, Chennai, India
Ananya Chakraborty, Department of ECE, SRM Institute of Science and Technology, Chennai, India

Throughout the years different approaches have been done in order to get a higher On current by varying the engineering of gate and channel with the help of novel techniques like Dual Gate (DG), Dual Material Double Gate (DMDG), Gate-all-around (GAA structures. Furthermore, the length, width and the doping concentration in channel can also be varied. One of the best discoveries have been the relation between the work function of the gate material and the On current. Studies have shown that, significant improvement in On current and suppression in SCE can be witnessed by using a GAA TFET with proper work function [4].

After analyzing the various results obtained from the previous research works we have concatenated some of the optimum characteristics for TFET to obtain the most efficient structure, such as - (i) Gate-All-Around (GAA) TFET [4] (ii) 2-D Triple Material Gate (TMG) TFET with optimum work function [1] (iii) Stacked oxide 2-D TFET with SiO_2 and High-k Dielectric[2][5].

In this paper Section II illustrates the design of Triple Material Gate (TMG) Stacked Oxide TFET in detail, along with the reasons behind its engineering. Section III presents the band diagram of TFET in Off state and On statealong with the graphs of Doping concentration, Electric Field, Electrostatic Potential and Electron Mobility. Furthermore, the improvement in I_{ds}-V_{gs}curve in TMGSO TFET is compared to TMG Single Oxide TFET and Single Metal Gate (SMG) TFET.

II. DESIGN AND SIMULATION OF TMG STACKED OXIDE TFET

For the design of Triple Material Gate Stacked Oxide (TMGSO) TFET, a 3-D Gate-All-Around (GAA) cylindrical structure is chosen which shows an improvement in electric field intensity at source-channel interface. Also, it shows an excellent immunity against the undesirable SCEs [9]. Furthermore, three materials with different work functions are used for the construction of the gate. Sneh Saurabh et al. have proposed an analytical model for Dual Material Double Gate 2-D structure with an experimental proof for the range of values needed to be chosen for the gate work functions [1]. In our structure we have taken 4.6eV as work function for Gate 1, 4.3eV for Gate 2 and 4.2 eV for Gate 3. It is noticed that the work function of the metal gate has direct impact on the lateral electric field and potential over the channel.We have used a low band gap material Ge and SiGe for source and drain respectively with Si as channel.

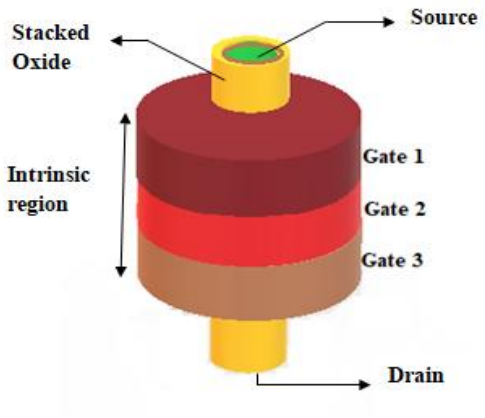

Fig. 1 3-D Structure of TMG Stacked Oxide TFET

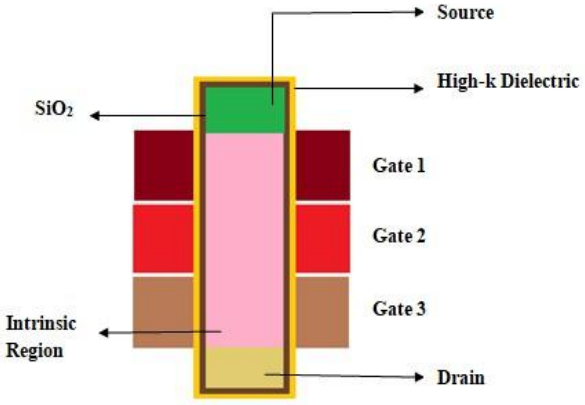

Fig. 2 Cross-sectional view of TMG Stacked Oxide TFET

While scaling down the dimensions of TFET the oxide layer thickness also needs to be decreased, however decreasing thickness of SiO_2 leads to THE increase in leakage current. Therefore, high-k dielectric with minimum thickness can be used as an alternative. But using a high-k dielectric at source-channel interface can lead to fringing effect, thus a stacked oxide comprising of both SiO_2 and high-k dielectric is used. Furthermore, the source and the drain are doped with p-type and n-type materials respectively. The doping concentration in source is 1x 10^{20} cm^{-3} and that in drain is 5x10^{18} cm^{-3}. Note that the doping concentration in source is higher than that in drain.

The TMGSO TFET is devised on Sentaurus Device Editor (SDE) and the simulation results for the designed structure is obtained on Sentaurus Visual (S-Visual) as shown in Fig. 3.

TABLE I
DESIGN PARAMETERS FOR TMG STACKED OXIDE TFET

Region	Material	Doping/Work Function	Length/Thickness
Source	Germanium	1x 10^{20} cm^{-3}	7nm
Drain	Silicon Germanium	5x10^{18} cm^{-3}	7nm
Intrinsic	Silicon	1x$10^{17}$$cm^{-3}$	28nm
Gate 1	Metal 1	4.6 eV	7nm
Gate 2	Metal 2	4.3 eV	13nm
Gate 3	Metal 3	4.2 eV	7nm
Oxide	SiO_2		0.6nm
	High-k Dielectric		

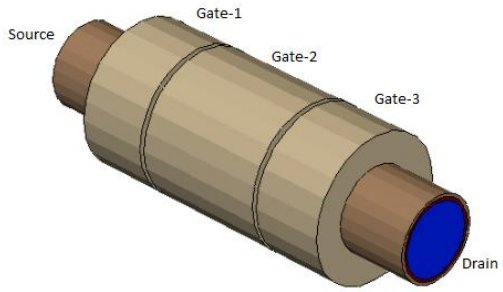

Fig. 3 Simulation result obtained on S-Visual , after designing structure on SDE

III. RESULTS AND DISCUSSION

All the simulations are done on 3-D TCAD device simulator, which uses various models such as Shockley–Read–Hall model, BTBT model, Kane's and Keldysh's models [3]. In Fig. 4 shows the band to band tunneling diagram for TMG Stacked Oxide TFET at an On state with V_{gs} as 0.3 V and at an Off state with V_{gs} as 0V, and V_{ds} kept constant as 1V. Moreover, as TFET follows BTBT principle, the electron in valence band of the source cannot be tunneled to the conduction band of the channel at Off state due to the voltage barrier. However, when a gate voltage of 0.3 V is applied, the valence and the conduction band overlap each other thereby increasing the tunneling probability.

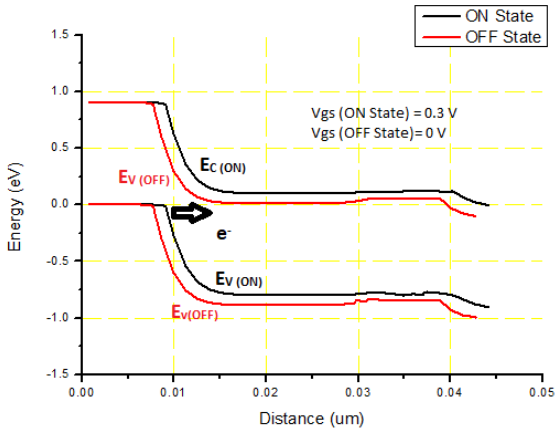

Fig. 4 Shows the Band-to-Band tunnelling of electrons in ON State (Vgs=0.3V), also it shows the band gap between the valence band of source and conduction band of channel at OFF State (Vgs=0V)

Fig. 5 shows the doping concentration provided in the source, drain and intrinsic region of TMGSO TFET. The need for providing a higher doping concentration of 1x 10^{20} cm^{-3} at source and a lower doping concentration of 5x10^{18} cm^{-3} at drain is because of the asymmetry in TFET and as a measure to suppress the drain-induced barrier lowering.

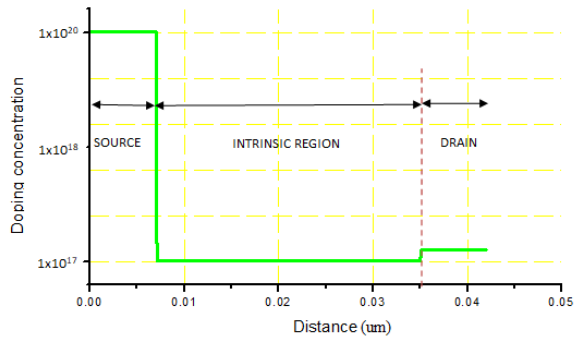

Fig. 5 Doping concentration in TMG Stacked Oxide TFET, with 1x 10^{20} cm^{-3} of p-type material in source and 5x10^{18} cm^{-3} of n-type material in drain

The accuracy of TMG Stacked Oxide TFET is compared with the TMG Single Oxide TFET and SMG TFET. Fig. 6 shows the comparison between the simulated values for the lateral electric fields of TMG Stacked Oxide TFET, TMG Single Oxide TFET and Single Material Gate (SMG) TFET. The lateral electric field for both the TMG structures show similar properties due to the same work function used for the gate materials. However, in SMG GAA TFET work function of the metal is kept as 4.6eV. It can be noted that the source-channel interface experiences the highest electric field intensity, and the drain-channel interface experiences the least, except in SMG GAA TFET.

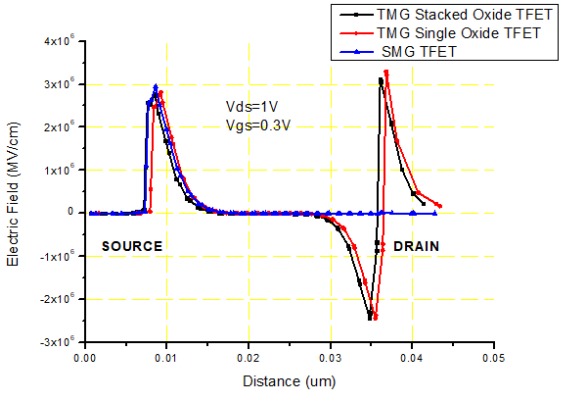

Fig. 6 Variation oflateral electric field for TMG Stacked Oxide, TMG Single Oxide and SMG TFET along the channel at Vds =1V and Vgs=0.3V

Fig. 7 shows the comparison between the electrostatic potential of different TFETs. The potential varies near the junction of metal gates, but it is constant in the middle of the Silicon body. There are two step changes in the potential values of TMG Stacked Oxide and TMG Single Oxide TFET along the channel at the interface of Gate 1-Gate 2 and Gate 2 -Gate 3. This implies that there is a reduction in drain current over the channel. The SCEs are also suppressed significantly when compared to that of SMG TFET due to the change in work function.

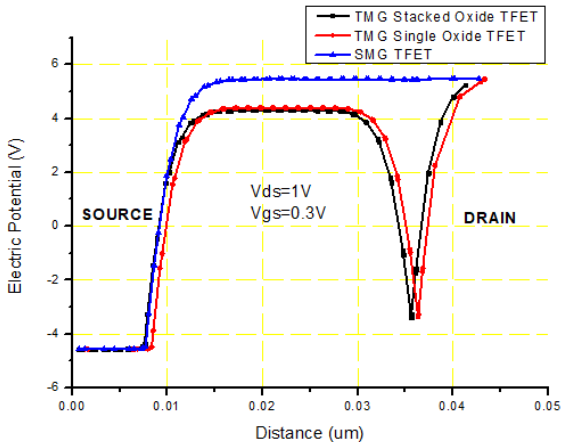

Fig. 7 Variation of electrostatic potential along the channel region at Vds=1V and Vgs=0.3V for TMG Stacked Oxide, TMG Single Oxide and SMG TFET.

Fig. 8 shows the electron mobility in TMG and SMG TFET along the channel. With a high electric field and electron mobility in the source region, the drift velocity of electrons becomes significantly higher when compared to that in drain.

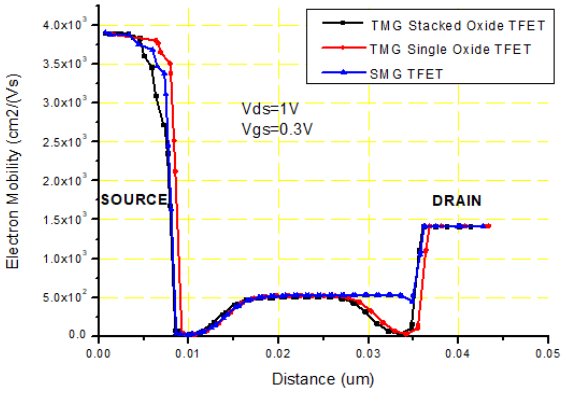

Fig. 8 Variation of electrostatic potential along the channel region at Vds=1V and Vgs=0.3V for TMG Stacked Oxide, TMG Single Oxide and SMG TFET.

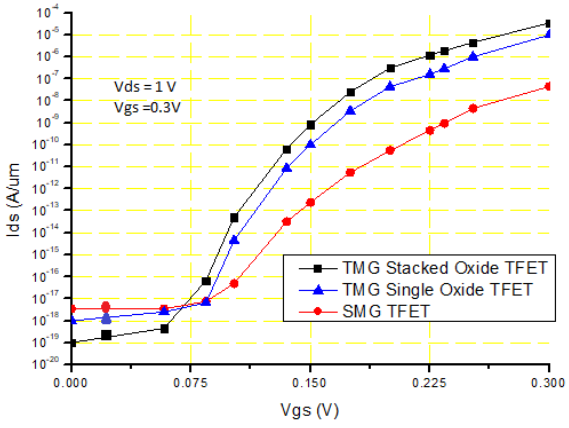

Fig. 10 Ids-Vgs curves for TMG Stacked Oxide TFET, TMG Single Oxide TFET and SMG TFET at Vds=1V and Vgs=0.3V.

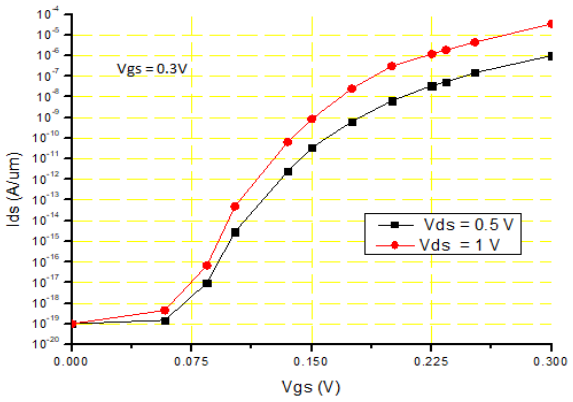

Fig.10 The Ids-Vgs Curve for Vds = 1V and Vds=0.5 V, for Vgs=0.3V

Fig. 9 shows the comparison in I_{ds}-V_{gs} curve of TMG Stacked Oxide, TMG Single Oxide and SMG TFET. The simulation is done for V_d = 1V and V_{gs}=0.3 V. For TMG Single Oxide and SMG TFET the oxidelayer thickness is 8nm and the work function in SMG is 4.6eV .All the other physical parameters are equivalent to that of TMGSO TFET, as shown in parameter table-1. The improvement in Off current in TMGSO TFET is due to the careful choice of gate di-electric and its dimensions. There is a considerable increase in On current in TMG compared to that in SMG TFET. The threshold voltage obtained in TMG TFET is around 0.058 V and in SMG TFET is 0.083 V. Fig. 10 depicts the change in sub-threshold slope for various values of V_{ds} with V_{gs} as 0.3V.

IV. CONCLUSION

Design and Simulation of Triple Metal Stacked Oxide TFET is done using TCAD Sentaurus Simulator. The benefits of including a stacked oxide layer of high-k dielectric and SiO_2 has been studied by comparing the I_{ds}-V_{gs} curves of TMGSO TFET with TMG Single Oxide TFET, it can be observed that there is an improvement in I_{ON}-I_{OFF} ratio in TMGSO TFET. Furthermore, the benefits of using triple material gate can also be observed by comparing the electric field and electrostatic potential characteristics of SMG and TMG TFET. In conclusion,TMGSO TFET was able to provide a better On current and also a suppressed threshold voltage and Off current. In future, the research can be done on decreasing the complexity of the design and alsoapproaches can be made for making it cost effective.

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